Document Title

256Kx72-Bit Pipelined N*t*RAM^{TM}

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial document.	April. 21. 2001	Preliminary
0.1	1. Add JTAG Scan Order	May. 10. 2001	Preliminary
0.2	1. Upate DC characteristics(icc,isb)	Aug. 30. 2001	Preliminary
0.3	1. Speed bin merge. From K7N167249A to K7N167245A. 2. AC parameter change. tOH(min)/tLZC(min) from 0.8 to 1.5 at -25 tOH(min)/tLZC(min) from 1.0 to 1.5 at -22 tOH(min)/tLZC(min) from 1.0 to 1.5 at -20	Dec. 26. 2001	Preliminary

16Mb NtRAM(Flow Through / Pipelined) , Double Late Write RAM x72 Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7M161825A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns	Q : 100TQFP H : 119BGA F : 165FBGA	C (Commercial Temperature Range) I (Industrial Temperature Range)
	K7N161801A-Q(H/F)C(I)25/22/20/16/13	Pipelined	3.3	250/225/200/167/133MHz		
	K7N161845A-Q(H/F)C(I)25/22/20/16/13	Pipelined	2.5	250/225/200/167/133MHz		
512Kx32	K7M163225A-QC(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163201A-QC(I)25/22/20/16/13	Pipelined	3.3	250/225/200/167/133MHz		
	K7N163245A-QC(I)25/22/20/16/13	Pipelined	2.5	250/225/200/167/133MHz		
512Kx36	K7M163625A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163601A-Q(H/F)C(I)25/22/20/16/13	Pipelined	3.3	250/225/200/167/133MHz		
	K7N163645A-Q(H/F)C(I)25/22/20/16/13	Pipelined	2.5	250/225/200/167/133MHz		
256Kx72	K7N167245A-HC25/22/20/16/13	Pipelined (Normal	2.5	250/225/200/167/133MHz	H : 209BGA	
	K7Z167285A-HC30/27/25	Pipelined (Sigma Type)	1.8	300/275/250MHz		

256Kx72-Bit Pipelined N*t*RAM™

FEATURES

- 2.5V ±5% Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention .
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 209BGA(11x19 Ball Grid Array Package).

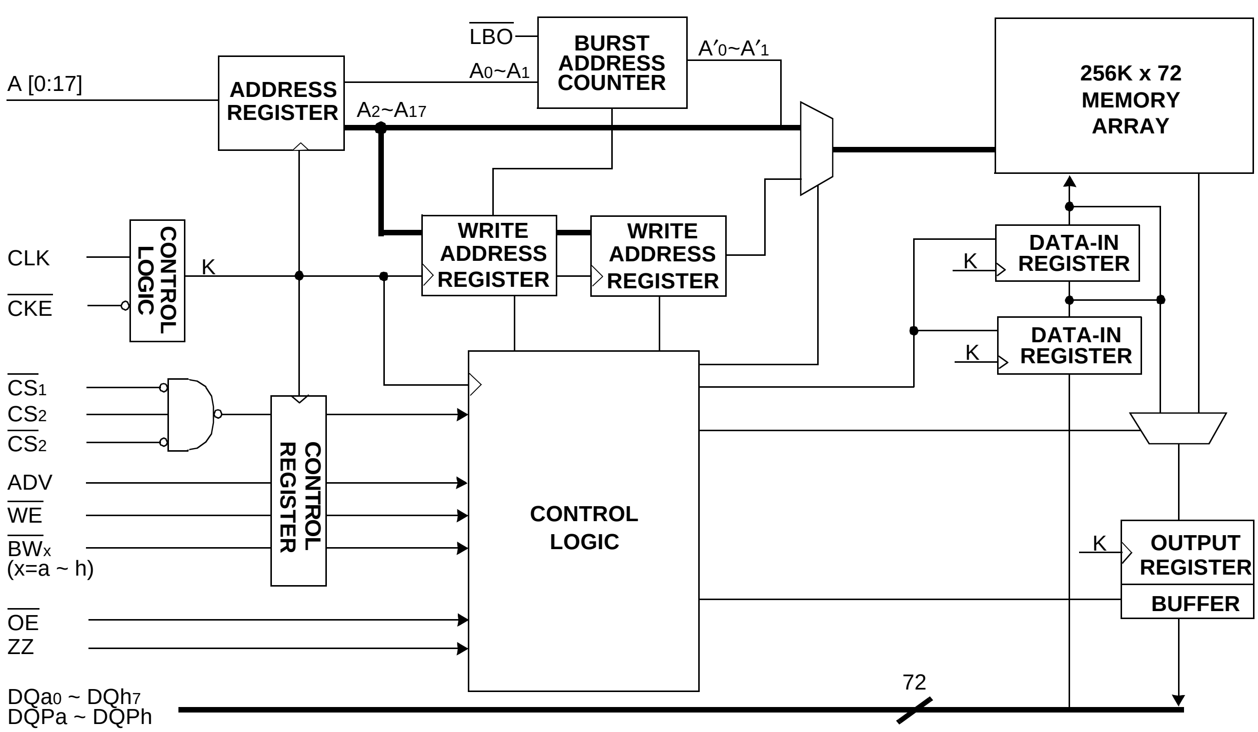
FAST ACCESS TIMES

PARAMETER	Symbol	-25	-22	-20	-16	-13	Unit
Cycle Time	tCYC	4.0	4.4	5.0	6.0	7.5	ns
Clock Access Time	tCD	2.6	2.8	3.2	3.5	4.2	ns
Output Enable Access Time	tOE	2.6	2.8	3.2	3.5	4.2	ns

GENERAL DESCRIPTION

The K7N167245A is 18,874,368-bits Synchronous Static SRAMs. The N*t*RAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles.
Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock.
Burst order control must be tied "High or Low".
Asynchronous inputs include the sleep mode enable(ZZ).
Output Enable controls the outputs at any given time.
Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation
and provides increased timing flexibility for incoming signals.
For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.
The K7N167245A are implemented with SAMSUNG′s high performance CMOS technology and is available in 209BGA packages. Multiple power and ground pins minimize ground bounce.

LOGIC BLOCK DIAGRAM



209BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7N167245A(256K x 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	CS2	A	ADV	A	CS2	A	DQb	DQb
B	DQg	DQg	BWc	BWg	NC	WE	A	BWb	BWf	DQb	DQb
C	DQg	DQg	BWh	BWd	NC	CS1	NC	BWe	BWa	DQb	DQb
D	DQg	DQg	VSS	NC	NC	OE	NC	NC	VSS	DQb	DQb
E	DQPg	DQPc	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQPf	DQPb
F	DQc	DQc	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQf	DQf
G	DQc	DQc	VDDQ	VDDQ	VDD	NC	VDD	VDDQ	VDDQ	DQf	DQf
H	DQc	DQc	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQf	DQf
J	DQc	DQc	VDDQ	VDDQ	VDD	NC	VDD	VDDQ	VDDQ	DQf	DQf
K	NC	NC	CLK	NC	VSS	CKE	VSS	NC	NC	NC	NC
L	DQh	DQh	VDDQ	VDDQ	VDD	NC	VDD	VDDQ	VDDQ	DQa	DQa
M	DQh	DQh	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQa	DQa
N	DQh	DQh	VDDQ	VDDQ	VDD	NC	VDD	VDDQ	VDDQ	DQa	DQa
P	DQh	DQh	VSS	VSS	VSS	ZZ	VSS	VSS	VSS	DQa	DQa
R	DQPd	DQPh	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQPa	DQPe
T	DQd	DQd	VSS	NC	NC	LBO	NC	NC	VSS	DQe	DQe
U	DQd	DQd	NC	A	NC(64M)	A	NC(32M)	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1**	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0**	A	TDO	TCK	DQe	DQe

Notes : 1. ** A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
		VSS	Ground
A0,A1	Burst Address Inputs		
ADV	Address Advance/Load	N.C.	No Connect
WE	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
CKE	Clock Enable	DQb	Data Inputs/Outputs
CS1	Chip Select	DQc	Data Inputs/Outputs
CS2	Chip Select	DQd	Data Inputs/Outputs
CS2	Chip Select	DQe	Data Inputs/Outputs
BWx	Byte Write Inputs	DQf	Data Inputs/Outputs
(x=a~h)		DQg	Data Inputs/Outputs
		DQh	Data Inputs/Outputs
OE	Output Enable	DQPa~Ph	Data Inputs/Outputs
ZZ	Power Sleep Mode		
LBO	Burst Mode Control	VDDQ	Output Power Supply
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7N167245A is N*t*RAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

N*t*RAM™ latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS}_1$, CS_2, $\overline{CS}_2$) are active .
Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS}_1$, CS_2, $\overline{CS}_2$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low.The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$[h:a] can be used for byte write operation. The pipelined N*t*RAM™ uses a late-late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.
The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.
And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$=High)

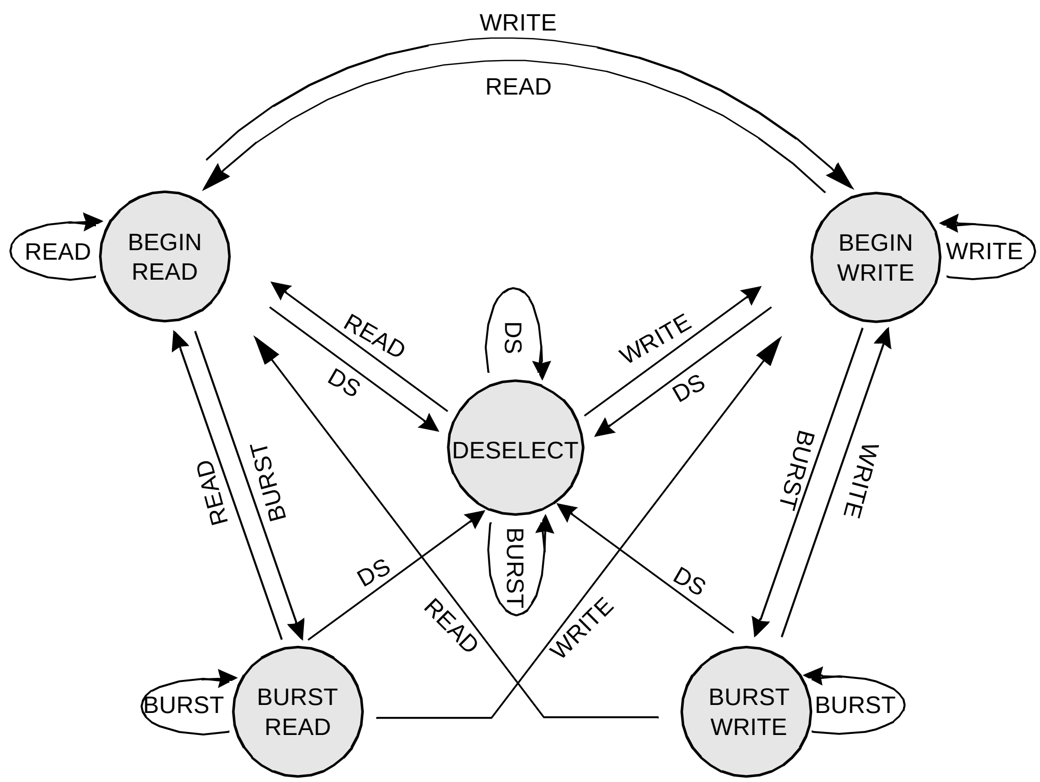
$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$=Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR N*t*RAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown is the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	ADV	$\overline{WE}$	$\overline{BW_x}$	$\overline{OE}$	$\overline{CKE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

Notes : 1. X means "Don′t Care". 2. The rising edge of clock is symbolized by (↑).
3. A continue deselect cycle can only be enterd if a deselect cycle is executed first.
4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
$\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x72)

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	$\overline{BWe}$	$\overline{BWf}$	$\overline{BWg}$	$\overline{BWh}$	OPERATION
H	X	X	X	X	X	X	X	X	READ
L	L	H	H	H	H	H	H	H	WRITE BYTE a
L	H	L	H	H	H	H	H	H	WRITE BYTE b
L	H	H	L	H	H	H	H	H	WRITE BYTE c
L	H	H	H	L	H	H	H	H	WRITE BYTE d
L	H	H	H	H	L	H	H	H	WRITE BYTE e
L	H	H	H	H	H	L	H	H	WRITE BYTE f
L	H	H	H	H	H	H	L	H	WRITE BYTE g
L	H	H	H	H	H	H	H	L	WRITE BYTE h
L	L	L	L	L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don′t Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

OPERATION	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes
1. X means "Don′t Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 3.6	V
Voltage on Any Other Pin Relative to VSS	VIN	-0.3 to VDD+0.3	V
Power Dissipation	PD	1.6	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

***Note** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS(0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	2.375	2.5	2.625	V
	VDDQ	2.375	2.5	2.625	V
Ground	VSS	0	0	0	V

***Note** : VDD and VDDQ must be supplied with identical vlotage levels.
The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(TA=25°C, f=1MHz)

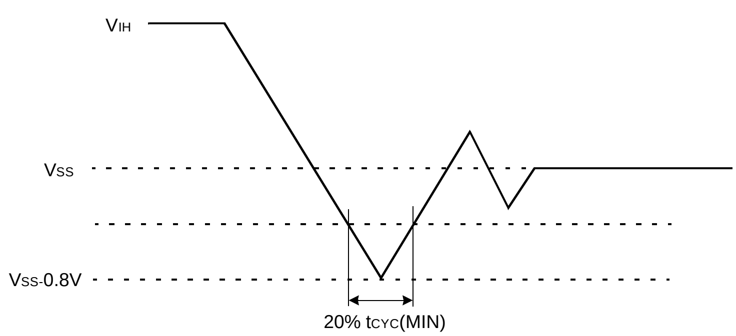
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOUT=0V	-	7	pF

***Note** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(V_{DD}=2.5V ±5%, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	µA	
Operating Current	I_{CC}	V_{DD}=Max I_{OUT}=0mA Cycle Time ≥ t_{CYC} Min	-25	-	620	mA	1,2
			-22	-	580		
			-20	-	540		
			-16	-	500		
			-13	-	450		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-25	-	150	mA	
			-22	-	140		
			-20	-	130		
			-16	-	120		
			-13	-	110		
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	70		
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	60		
Output Low Voltage	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage	V_{IL}			-0.3*	0.7	V	
Input High Voltage	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. Data states are all zero.
4. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V



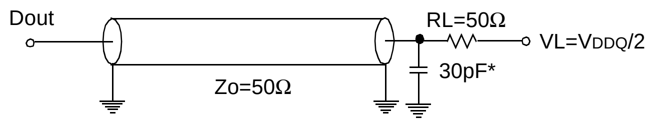
TEST CONDITIONS

(T_A=0 to 70°C, V_{DD}=2.5V ±5%, unless otherwise specified)

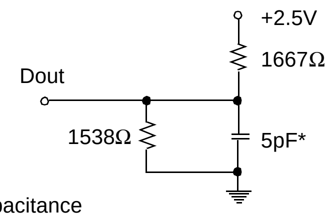
PARAMETER	VALUE
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	V_{DDQ}/2
Output Load	See Fig. 1

* The above parameters are also guaranteed at industrial temperature range.

Output Load(A)



Output Load(B),
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=2.5V ±5%, T_A=0 to 70°C)

PARAMETER	SYMBOL	-25		-22		-20		-16		-13		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CYC}	4.0	-	4.4	-	5.0	-	6.0	-	7.5	-	ns
Clock Access Time	t_{CD}	-	2.6	-	2.8	-	3.2	-	3.5	-	4.2	ns
Output Enable to Data Valid	t_{OE}	-	2.6	-	2.8	-	3.2	-	3.5	-	4.2	ns
Clock High to Output Low-Z	t_{LZC}	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Hold from Clock High	t_{OH}	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	2.6	-	2.8	-	3.0	-	3.0	-	3.5	ns
Clock High to Output High-Z	t_{HZC}	-	2.6	-	2.8	-	3.0	-	3.0	-	3.5	ns
Clock High Pulse Width	t_{CH}	1.7	-	2.0	-	2.0	-	2.2	-	3.0	-	ns
Clock Low Pulse Width	t_{CL}	1.7	-	2.0	-	2.0	-	2.2	-	3.0	-	ns
Address Setup to Clock High	t_{AS}	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	ns
$\overline{CKE}$ Setup to Clock High	t_{CES}	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	ns
Data Setup to Clock High	t_{DS}	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{WE}$, $\overline{BW_X}$)	t_{WS}	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t_{ADVS}	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t_{CSS}	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	ns
Address Hold from Clock High	t_{AH}	0.3	-	0.4	-	0.4	-	0.5	-	0.5	-	ns
$\overline{CKE}$ Hold from Clock High	t_{CEH}	0.3	-	0.4	-	0.4	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.3	-	0.4	-	0.4	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{WE}$, $\overline{BW_X}$)	t_{WH}	0.3	-	0.4	-	0.4	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.3	-	0.4	-	0.4	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.3	-	0.4	-	0.4	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	2	-	2	-	2	-	cycle

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
4. A write cycle is defined by WE low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
5. To avoid bus contention, At a given voltage and temperature t_{LZC} is more than t_{HZC}.
The specs as shown do not imply bus contention because t_{LZC} is a Min. parameter that is worst case at totally different test conditions (0°C,2.625V) than t_{HZC}, which is a Max. parameter(worst case at 70°C,2.375V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

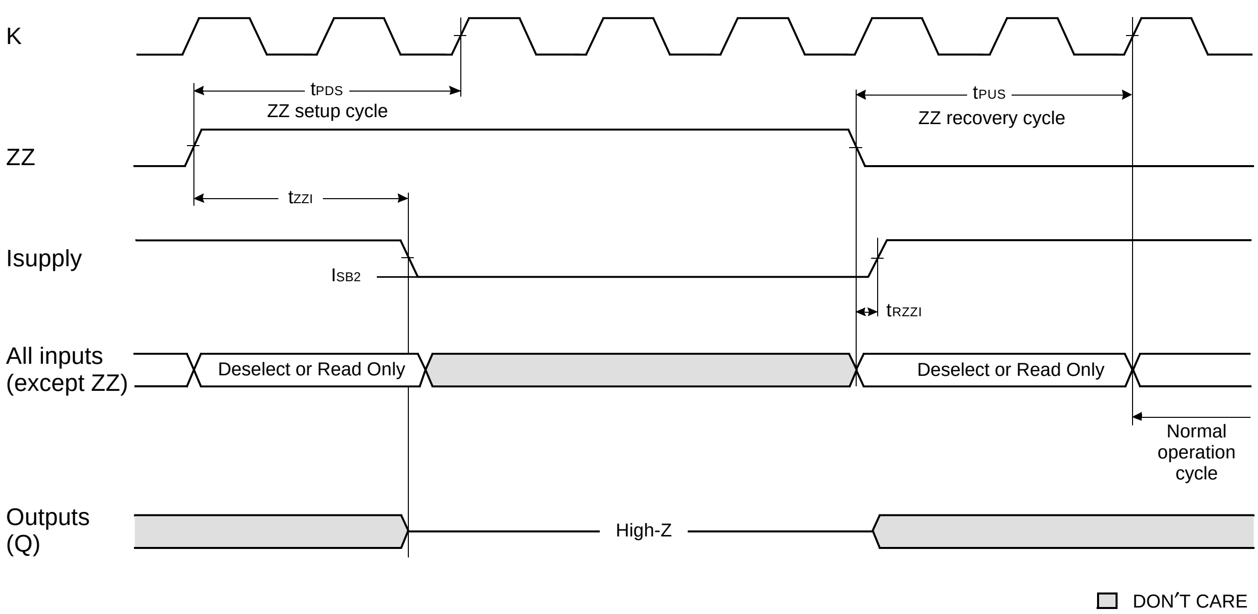
SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2}. The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.
After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.
When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. similarly, when exiting SLEEP MODE during t_{PUS}, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

SLEEP MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	ZZ ≥ V_{IH}	I_{SB2}		10	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

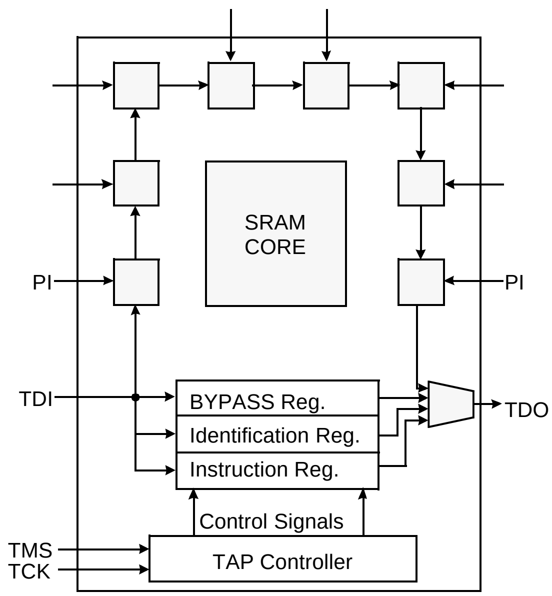
SLEEP MODE WAVEFORM



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



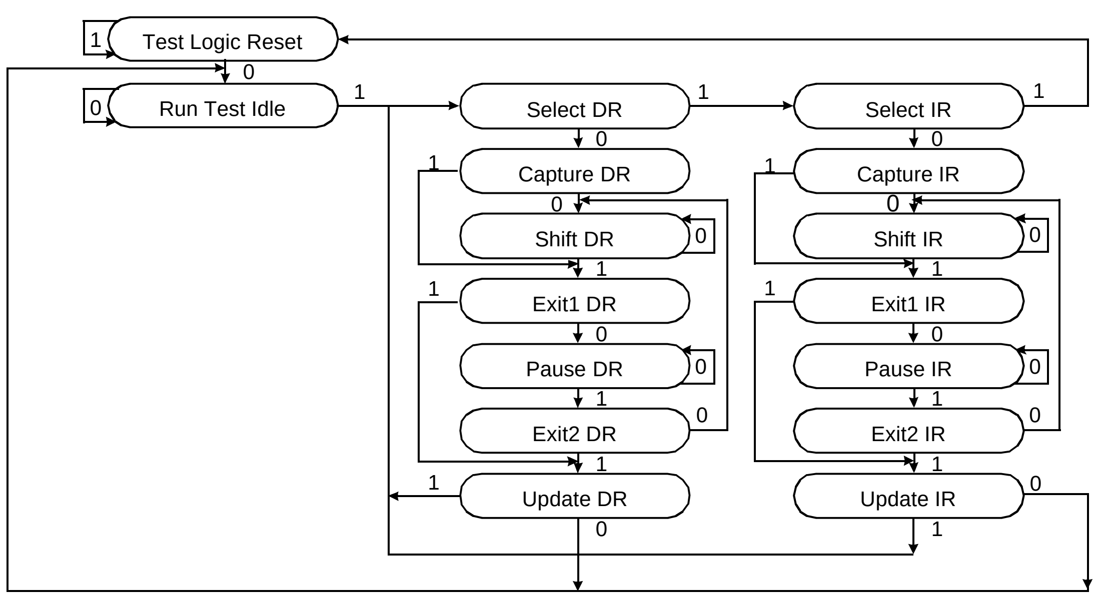
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx72	3 bits	1 bits	32 bits	122 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
256Kx72	0000	00110 00101	XXXXXX	00001001110	1

209BGA BOUNDARY SCAN EXIT ORDER(x72)

1	6W	A_0		DQf	11J	36
2	6V	A_1		DQf	11H	37
3	6U	A		DQf	10H	38
4	7V	A		DQf	10G	39
5	7U	NC		DQf	11G	40
6	7W	A		DQf	11F	41
7	8U	A		DQf	10F	42
8	8V	A		DQPf	10E	43
9	9V	A		DQPb	11E	44
10	6P	ZZ		DQb	11D	45
11	10W	DQe		DQb	10D	46
12	11W	DQe		DQb	10C	47
13	11V	DQe		DQb	11C	48
14	10V	DQe		DQb	11B	49
15	10U	DQe		DQb	10B	50
16	11U	DQe		DQb	10A	51
17	11T	DQe		DQb	11A	52
18	10T	DQe		$\overline{BWa}$	9C	53
19	11R	DQPe		$\overline{BWf}$	9B	54
20	10R	DQPa		A	9A	55
21	10P	DQa		$\overline{BWe}$	8C	56
22	11P	DQa		$\overline{BWb}$	8B	57
23	11N	DQa		$\overline{CS_2}$	8A	58
24	10N	DQa		A	7B	59
25	10M	DQa		A	7A	60
26	11M	DQa		NC	6H	61
27	11L	DQa		NC	6G	62
28	10L	DQa		$\overline{OE}$	6D	63
29	11K	NC		$\overline{CS_1}$	6C	64
30	6M	NC		$\overline{WE}$	6B	65
31	6L	NC		ADV	6A	66
32	6J	NC		NC	5C	67
33	6F	NC		A	5A	68
34	10K	NC		$\overline{BWd}$	4C	69
35	10J	DQf		$\overline{BWg}$	4B	70

71	4A	CS_2		DQPh	2R	106
72	3C	$\overline{BWh}$		DQPd	1R	107
73	3B	$\overline{BWc}$		DQd	1T	108
74	3A	A		DQd	2T	109
75	2A	DQg		DQd	2U	110
76	1A	DQg		DQd	1U	111
77	1B	DQg		DQd	1V	112
78	2B	DQg		DQd	2V	113
79	2C	DQg		DQd	2W	114
80	1C	DQg		DQd	1W	115
81	1D	DQg		$\overline{LBO}$	6T	116
82	2D	DQg		A	3V	117
83	1E	DQPg		A	4V	118
84	2E	DQPc		A	4U	119
85	2F	DQc		NC	5U	120
86	1F	DQc		A	5V	121
87	1G	DQc		A	5W	122
88	2G	DQc				
89	2H	DQc				
90	1H	DQc				
91	1J	DQc				
92	2J	DQc				
93	1K	NC				
94	3K	CLK				
95	4K	NC				
96	6K	$\overline{CKE}$				
97	2K	NC				
98	2L	DQh				
99	1L	DQh				
100	1M	DQh				
101	2M	DQh				
102	2N	DQh				
103	1N	DQh				
104	1P	DQh				
105	2P	DQh				

NOTE, NC ; Don′t Care

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	2.375	2.5	2.625	V	
Input High Level	V_{IH}	1.7	-	V_{DD}+0.3	V	1
Input Low Level	V_{IL}	-0.3	-	0.7	V	
Output High Voltage	V_{OH}	2.0	-	-	V	
Output Low Voltage	V_{OL}	-	-	0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V.

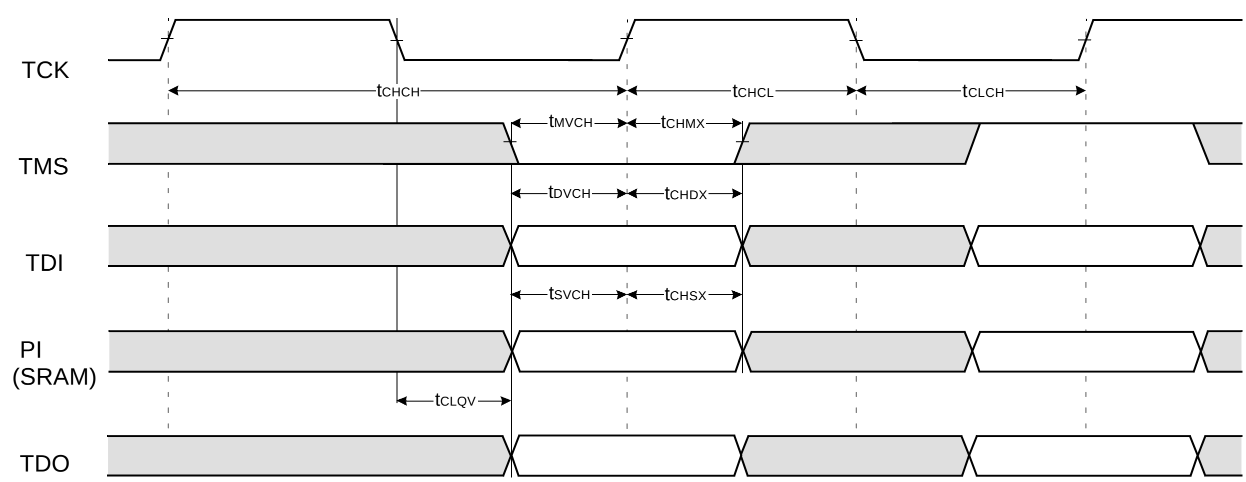
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	2.5/0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		V_{DDQ}/2	V	

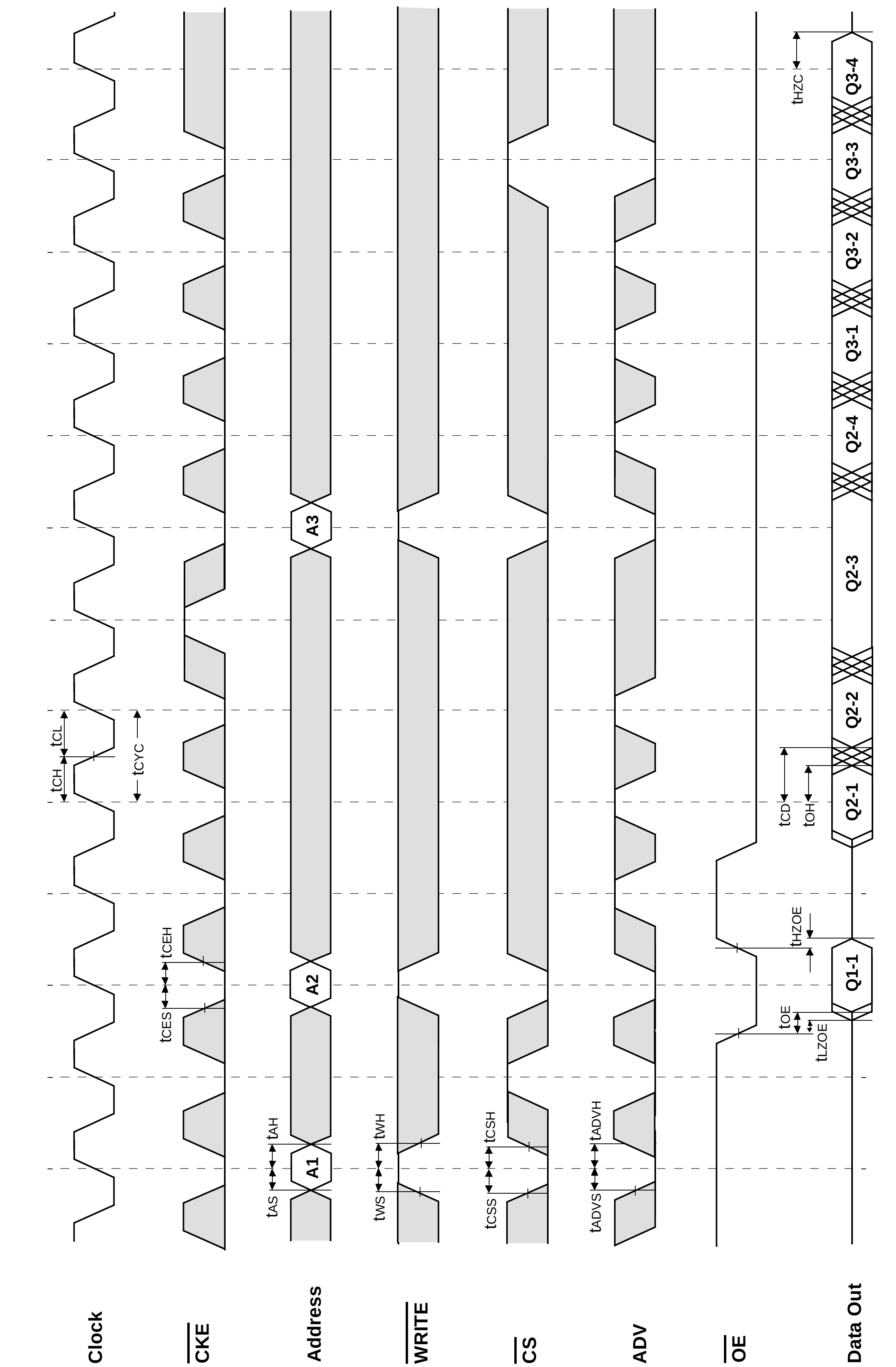
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



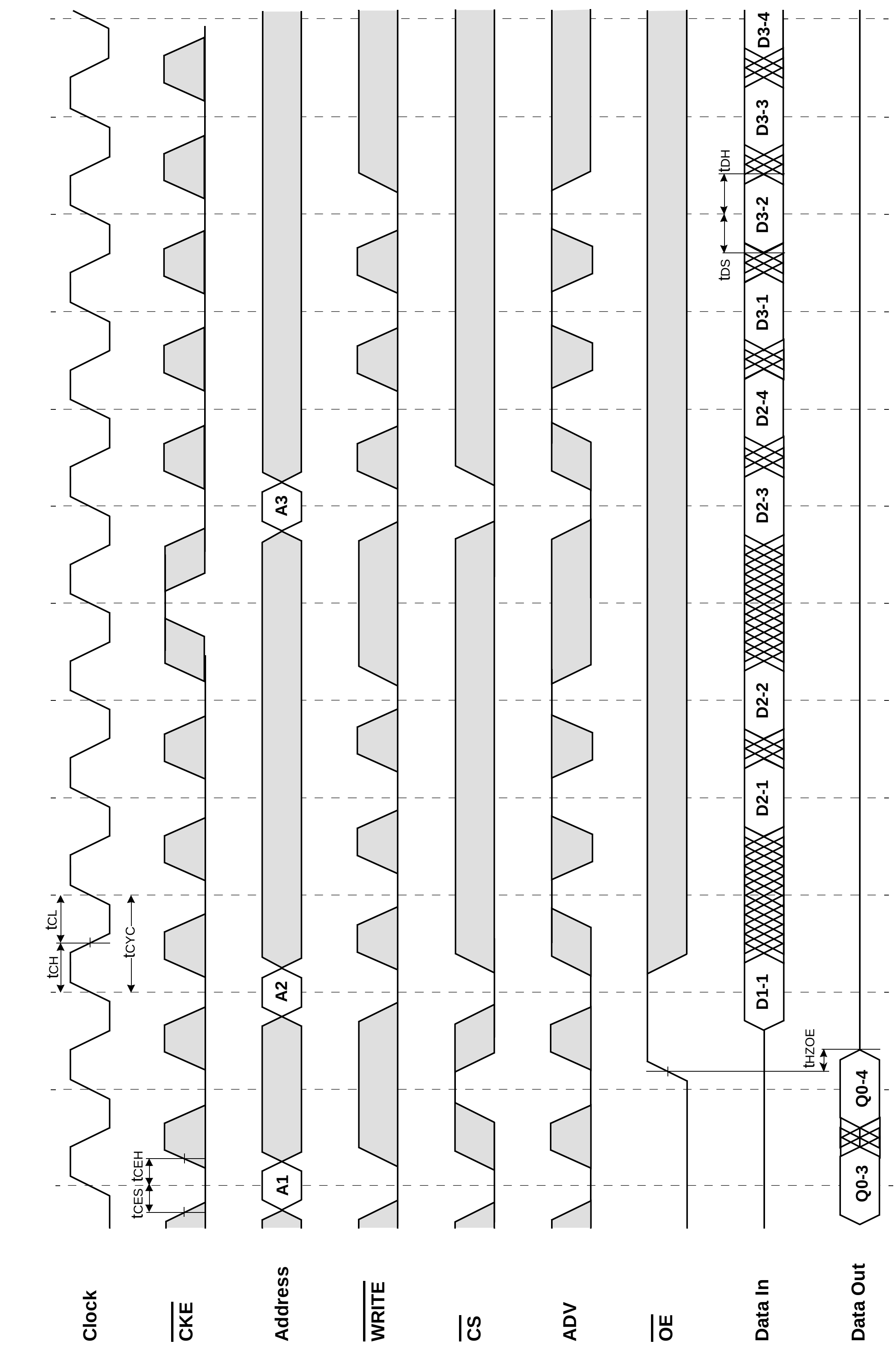
TIMING WAVEFORM OF READ CYCLE



Don't Care
Undefined

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or CS_1 = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

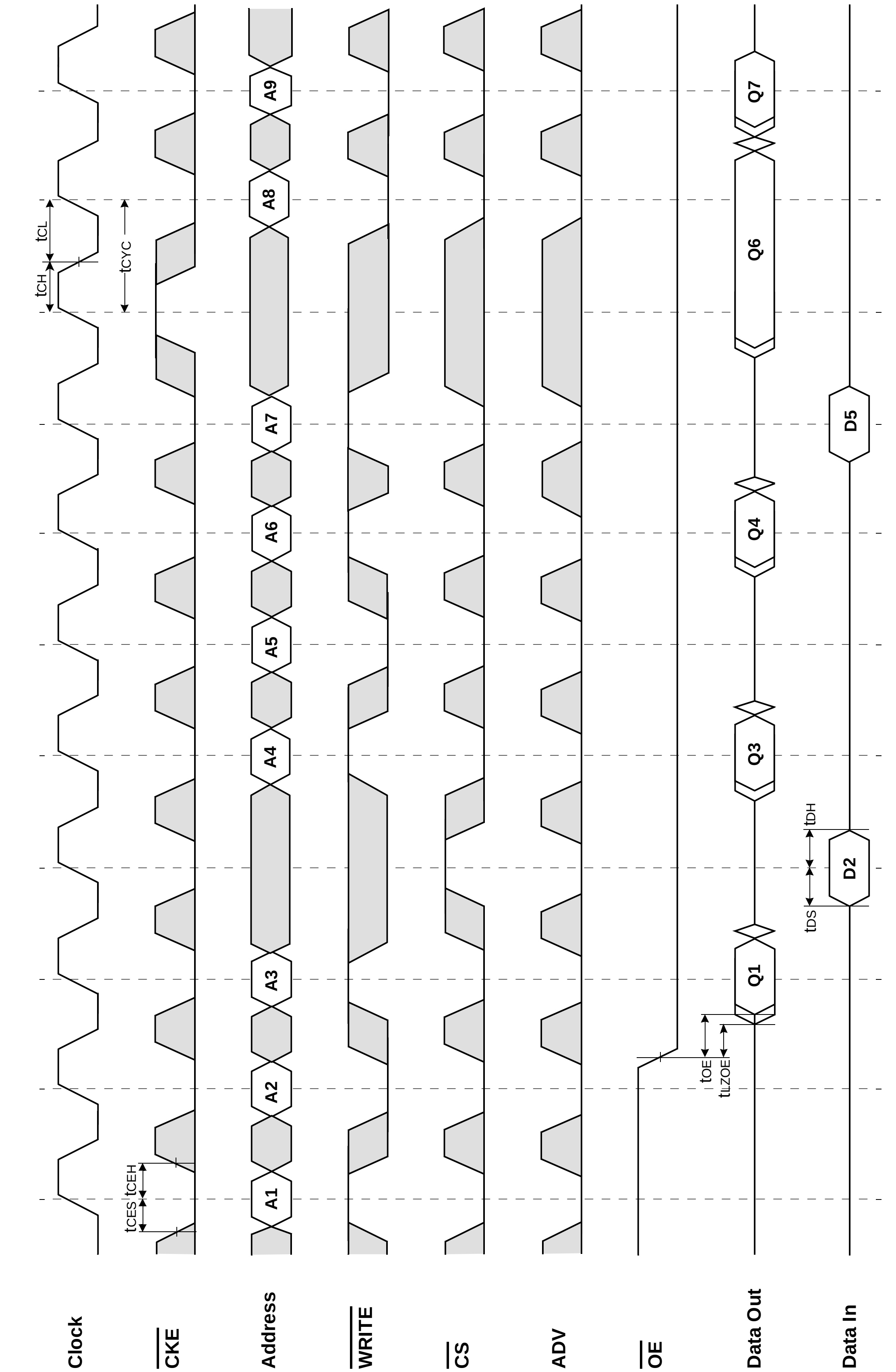
TIMING WAVEFORM OF WRTE CYCLE



Don't Care
Undefined

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BW_X}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

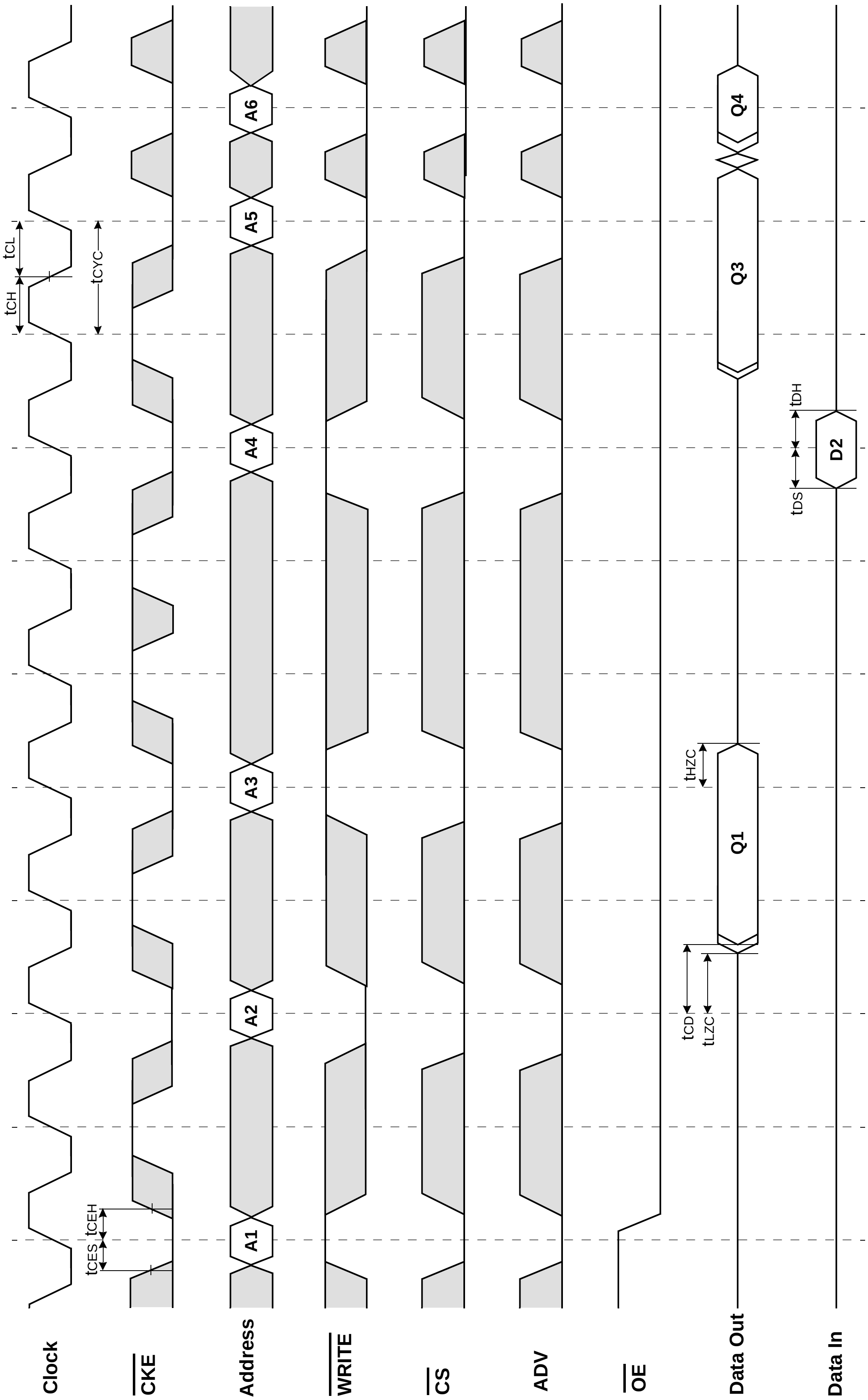
TIMING WAVEFORM OF SINGLE READ/WRITE



Don't Care
Undefined

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

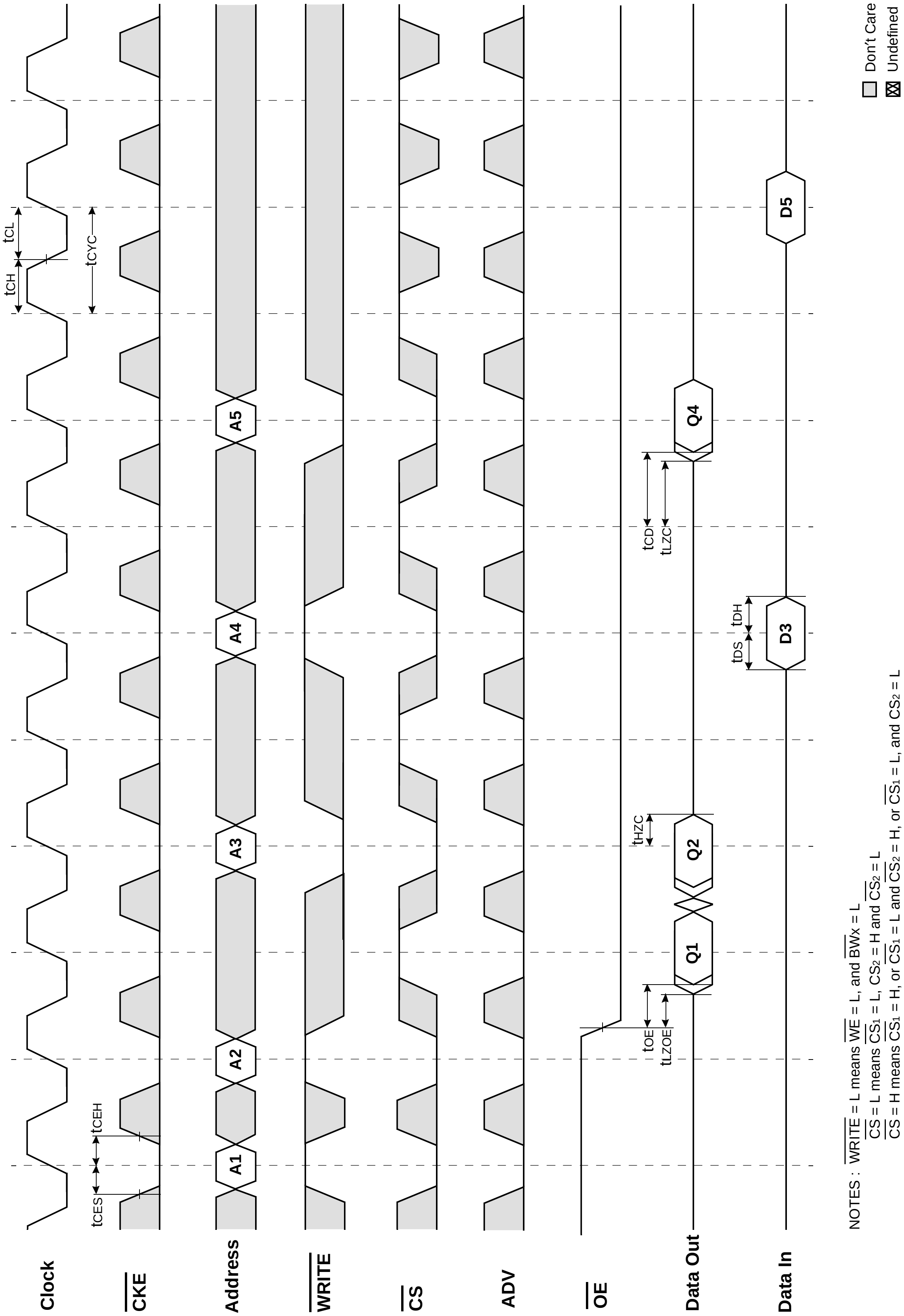
TIMING WAVEFORM OF $\overline{CKE}$ OPERATION



Don't Care
Undefined

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or CS_2 = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

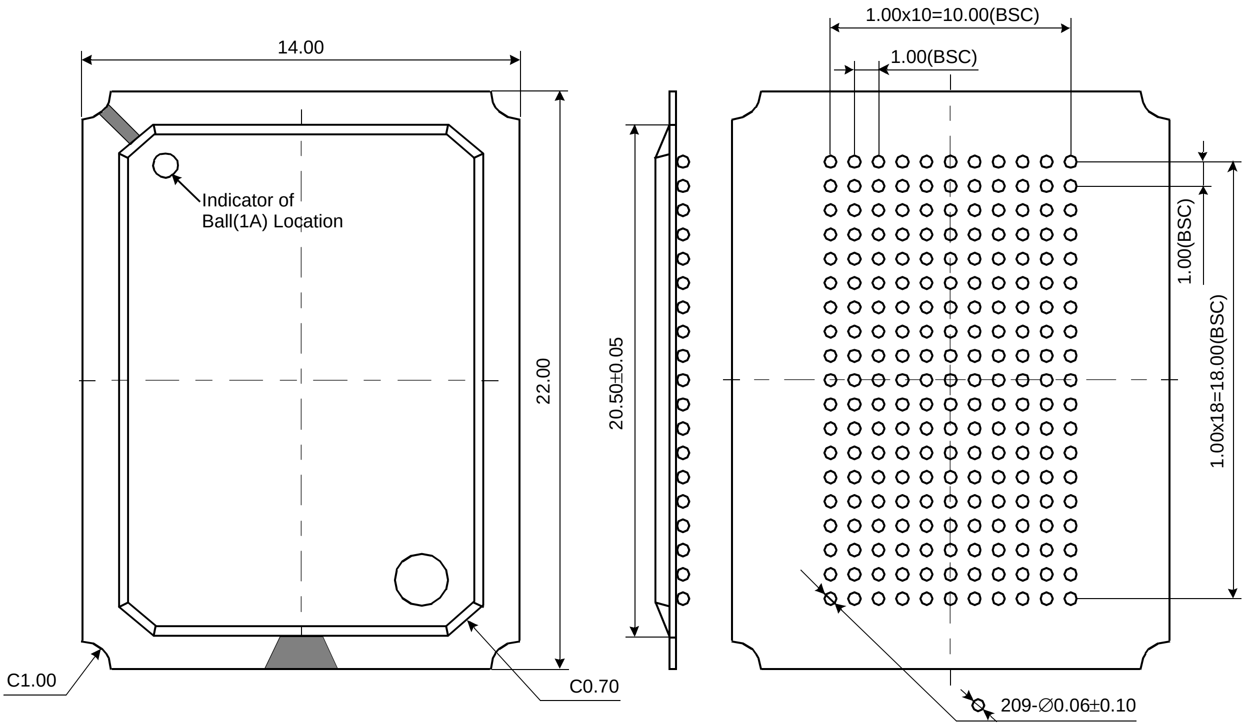
TIMING WAVEFORM OF $\overline{CS}$ OPERATION

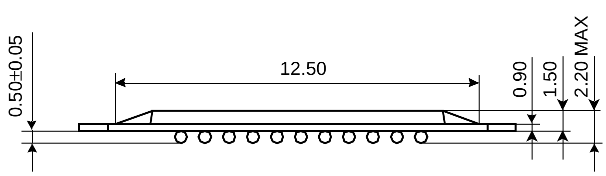


NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

209 Bump BGA PACKAGE DIMENSIONS

14mm x 22mm Body, 1.0mm Bump Pitch, 11x19 Bump Array





NOTE :
1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset: 0.10 MAX.
3. PCB to Cavity Offset: 0.10 MAX.