
Document Title

128Kx36 & 256Kx18-Bit Pipelined NtRAM™

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial document.	Jan. 20. 2000	Preliminary
0.1	1. Changed DC condition at I _{cc} and I _{sb} . I _{cc} ; from 350mA to 400mA at -16, from 340mA to 390mA at -15, from 310mA to 360mA at -13, I _{sb} ; from 130mA to 140mA at -16, from 120mA to 130mA at -15, from 120mA to 130mA at -13,	April. 03. 2000	Preliminary
1.0	1. Final spec release 2. Changed input & output capacitance. C _{IN} ; from 6pF to 5pF, C _{OUT} ; from 8pF to 7pF,	May. 15. 2000	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

128Kx36 & 256Kx18-Bit Pipelined NtRAM™

FEATURES

- $V_{DD}=3.3V+0.165V/-0.165V$ Power Supply.
- V_{DDQ} Supply Voltage $3.3V+0.165V/-0.165V$ for 3.3V I/O or $2.5V+0.4V/-0.125V$ for 2.5V I/O.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention.
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A Package.

FAST ACCESS TIMES

PARAMETER	Symbol	-16	-15	-13	Unit
Cycle Time	tCYC	6.0	6.7	7.5	ns
Clock Access Time	tCD	3.5	3.8	4.2	ns
Output Enable Access Time	tOE	3.5	3.8	4.2	ns

GENERAL DESCRIPTION

The K7N403601A and K7N401801A are 4,718,592 bits Synchronous Static SRAMs.

The NtRAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles.

Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low".

Asynchronous inputs include the sleep mode enable(ZZ).

Output Enable controls the outputs at any given time.

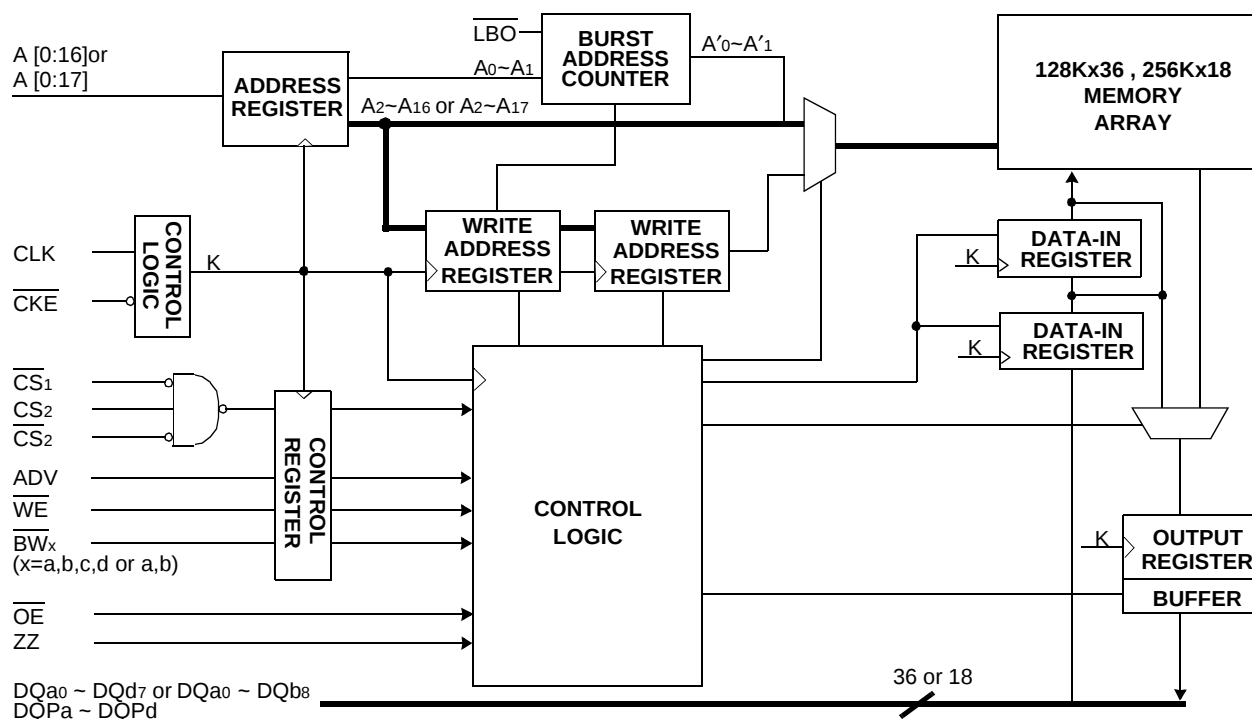
Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation

and provides increased timing flexibility for incoming signals.

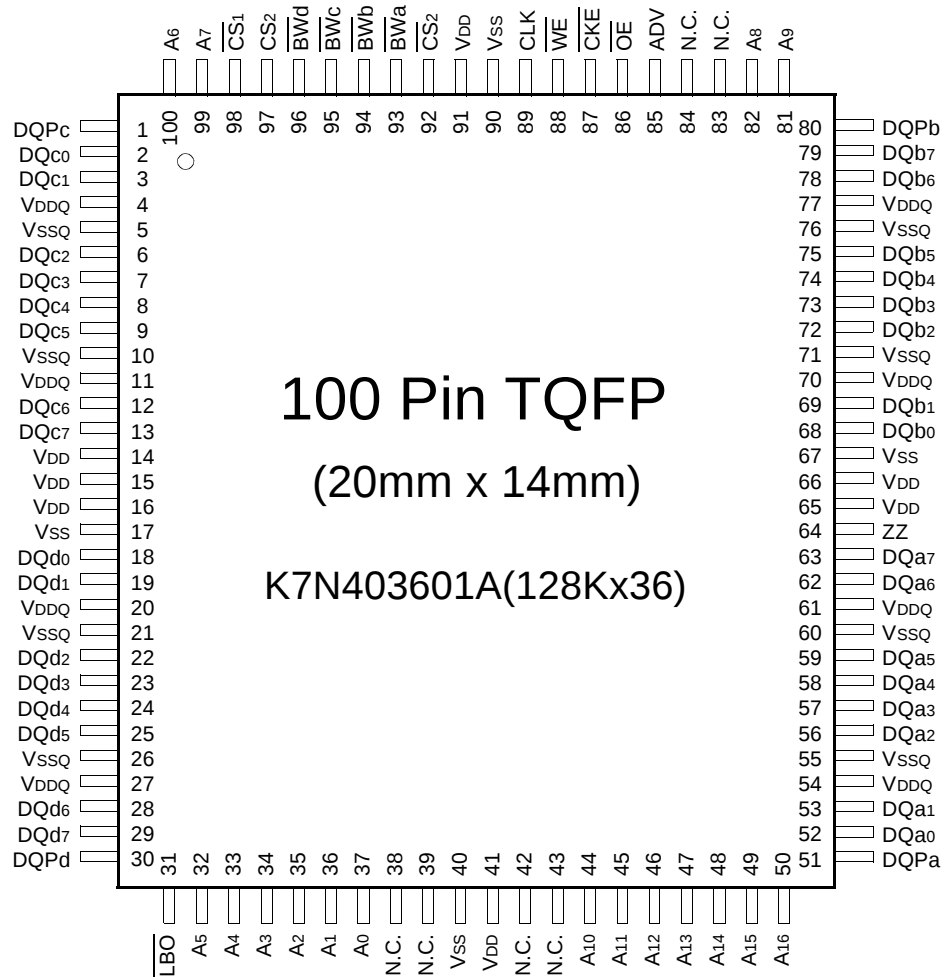
For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The K7N403601A and K7N401801A are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP packages. Multiple power and ground pins minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

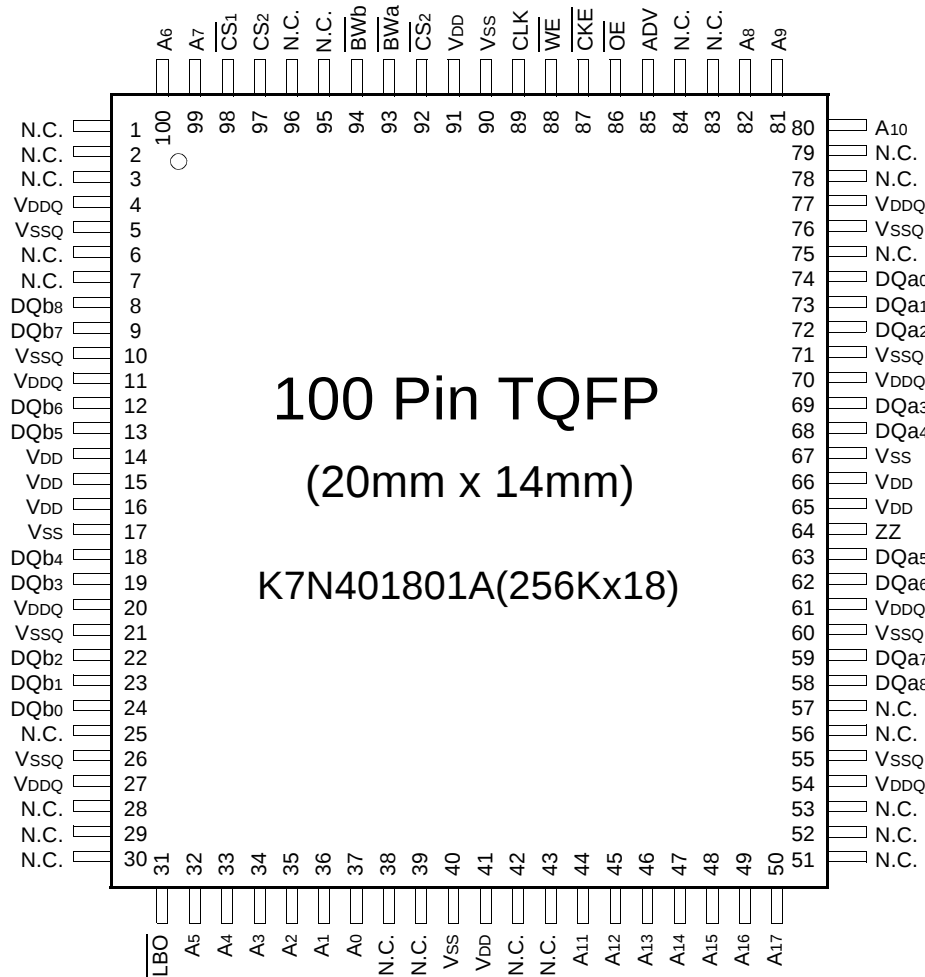


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37 44,45,46,47,48,49 50,81,82,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	38,39,42,43,83,84
ADV	Address Advance/Load	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
WE	Read/Write Control Input	88	DQb0~b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0~c7		2,3,6,7,8,9,12,13
CKE	Clock Enable	87	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQPa~Pd		51,80,1,30
CS2	Chip Select	97			
CS2	Chip Select	92			
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

Notes : 1. The pin 83 is reserved for address bit for the 8Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,80,81,82,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
ADV	Address Advance/Load	85	VSS	Ground	17,40,67,90
WE	Read/Write Control Input	88	N.C.	No Connect	1,2,3,6,7,25,28,29,30,38,39,42,43,51,52,53,56,57,75,78,79,83,84,95,96
CLK	Clock	89	DQa0~a8	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CKE	Clock Enable	87	DQb0~b8		8,9,12,13,18,19,22,23,24
CS1	Chip Select	98			
CS2	Chip Select	97			
CS2	Chip Select	92			
BWx(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
ZZ	Power Sleep Mode	64	VSSQ	Output Ground	5,10,21,26,55,60,71,76
LBO	Burst Mode Control	31			

Notes : 1. The pin 83 is reserved for address bit for the 8Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

FUNCTION DESCRIPTION

The K7N403601A and K7N401801A are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NtRAM™ latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active .

Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}[d:a]$ can be used for byte write operation. The pipelined NtRAM™ uses a late-late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation, $\overline{ZZ}$ must be driven low. When $\overline{ZZ}$ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$ =High)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
		1	1	1	0	0	1	0	0

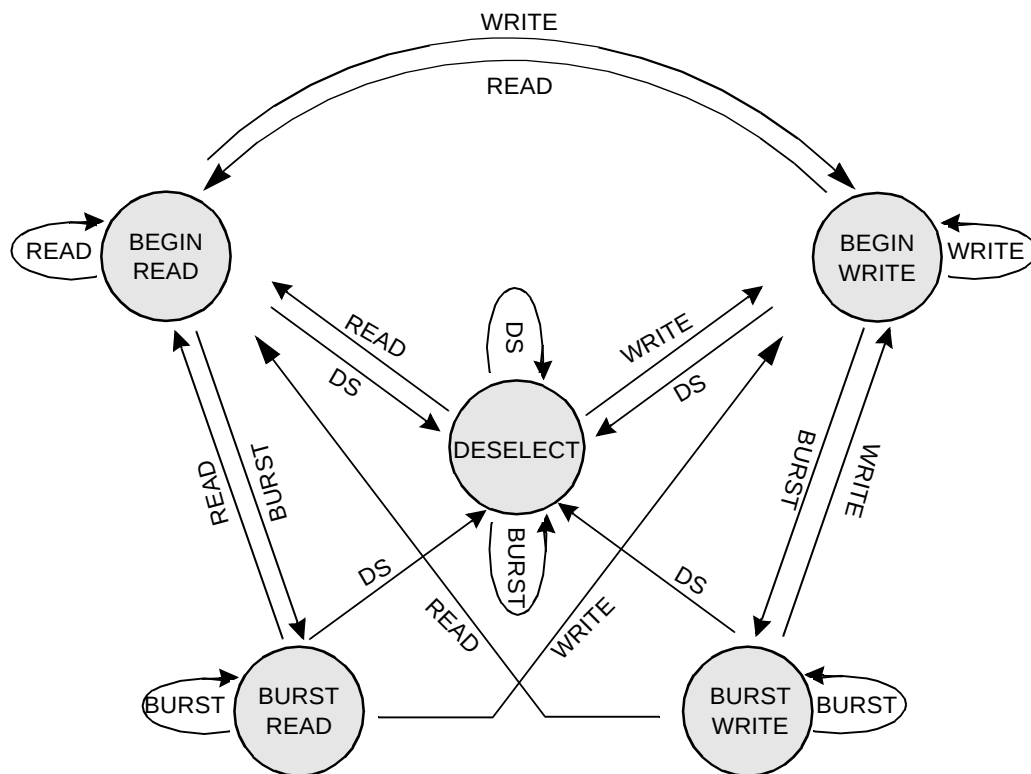
Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

(Linear Burst, $\overline{LBO}$ =Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_2$	ADV	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CKE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{WE}$	$\overline{BW}_a$	$\overline{BW}_b$	$\overline{BW}_c$	$\overline{BW}_d$	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTES
L	H	H	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{WE}$	$\overline{BW}_a$	$\overline{BW}_b$	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTES
L	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

OPERATION	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to V _{SS}	V _{IN}	-0.3 to V _{DD} +0.5	V
Power Dissipation	P _D	1.4	W
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T _{BIAS}	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	3.135	3.3	3.465	V
Ground	V _{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	2.375	2.5	2.9	V
Ground	V _{SS}	0	0	0	V

CAPACITANCE* (T_A=25°C, f=1MHz)

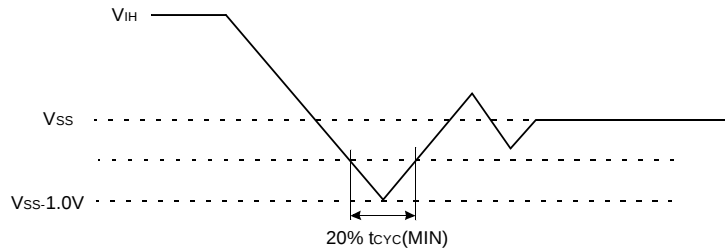
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C _{IN}	V _{IN} =0V	-	5	pF
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	7	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I _{IL}	$V_{DD}=Max$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	I _{OL}	Output Disabled,	-2	+2	μA	
Operating Current	I _{CC}	$V_{DD}=Max$ I _{OUT} =0mA Cycle Time $\geq t_{CYC}$ Min	-16	-	400	1,2
			-15	-	390	
			-13	-	360	
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ $\leq V_{IL}$, f=Max, All Inputs $\leq 0.2V$ or $\geq V_{DD}-0.2V$	-16	-	140	mA
			-15	-	130	
			-13	-	130	
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ $\leq 0.2V$, f=0, All Inputs=fixed ($V_{DD}-0.2V$ or $0.2V$)	-	100	mA	
	I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ $\geq V_{DD}-0.2V$, f=Max, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	50	mA	
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA	-	0.4	V	
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA	2.4	-	V	
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V	
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA	2.0	-	V	
Input Low Voltage(3.3V I/O)	V _{IL}		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V _{IH}		2.0	$V_{DD}+0.5^{**}$	V	3
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V _{IH}		1.7	$V_{DD}+0.5^{**}$	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.3V$



TEST CONDITIONS

($V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=3.3V+0.165V/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=2.5V+0.4V/-0.125V$, $T_A=0$ to $70^{\circ}C$)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	$V_{DDQ}/2$
Output Load	See Fig. 1

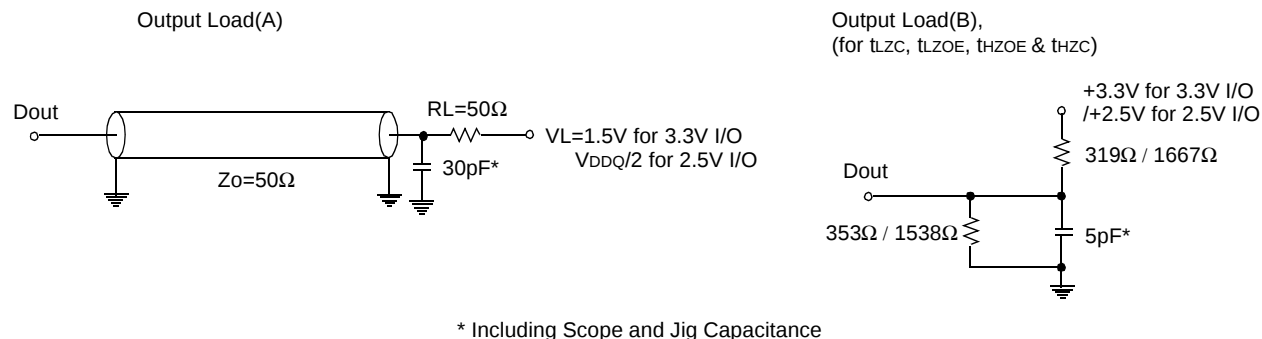


Fig. 1

AC TIMING CHARACTERISTICS(VDD=3.3V+0.165V/-0.165V, TA=0°C to +70°C)

PARAMETER	Symbol	-16		-15		-13		UNIT
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	6.0	-	6.7	-	7.5	-	ns
Clock Access Time	tCD	-	3.5	-	3.8	-	4.2	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.8	-	4.2	ns
Clock High to Output Low-Z	tLZC	1.5	-	1.5	-	1.5	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	-	3.5	-	3.8	ns
Clock High to Output High-Z	tHZC	-	3.5	-	3.5	-	3.8	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	1.5	-	1.5	-	1.5	-	ns
CKE Setup to Clock High	tCES	1.5	-	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.5	-	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{WE}$, $\overline{BWX}$)	tWS	1.5	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.5	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.5	-	1.5	-	1.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
CKE Hold from Clock High	tCEH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{WE}$, $\overline{BWEX}$)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature tLZC is more than tHZC.
The specs as shown do not imply bus contention because tLZC is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than tHZC, which is a Max. parameter(worst case at 70°C,3.135V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

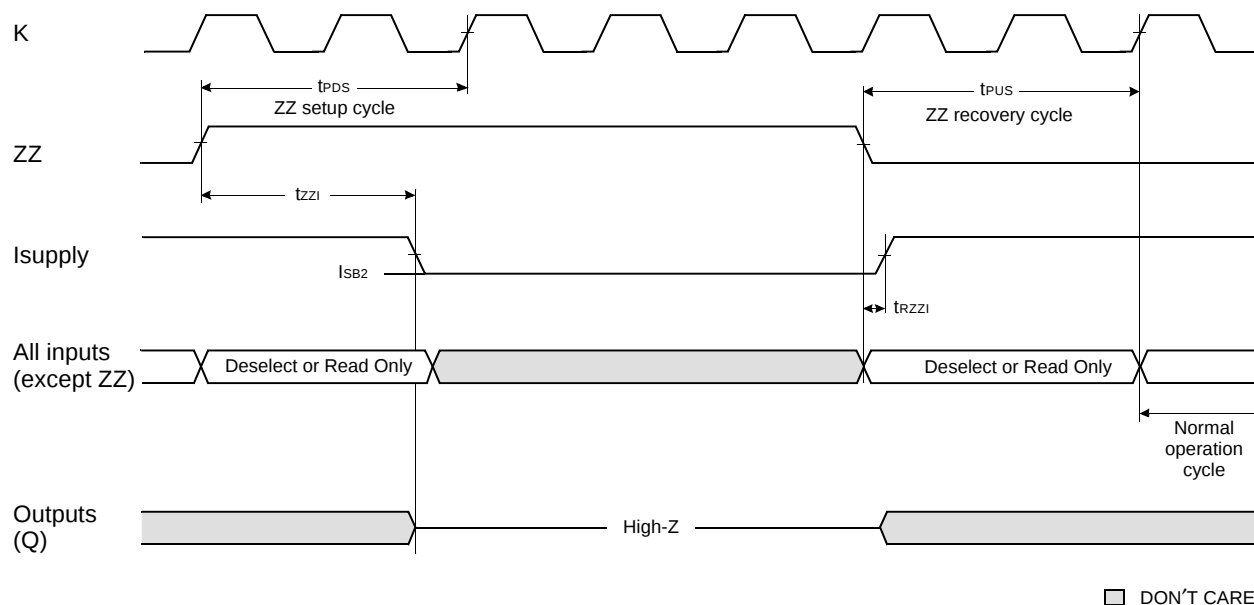
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. similarly, when exiting SLEEP MODE during t_{PUS} , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

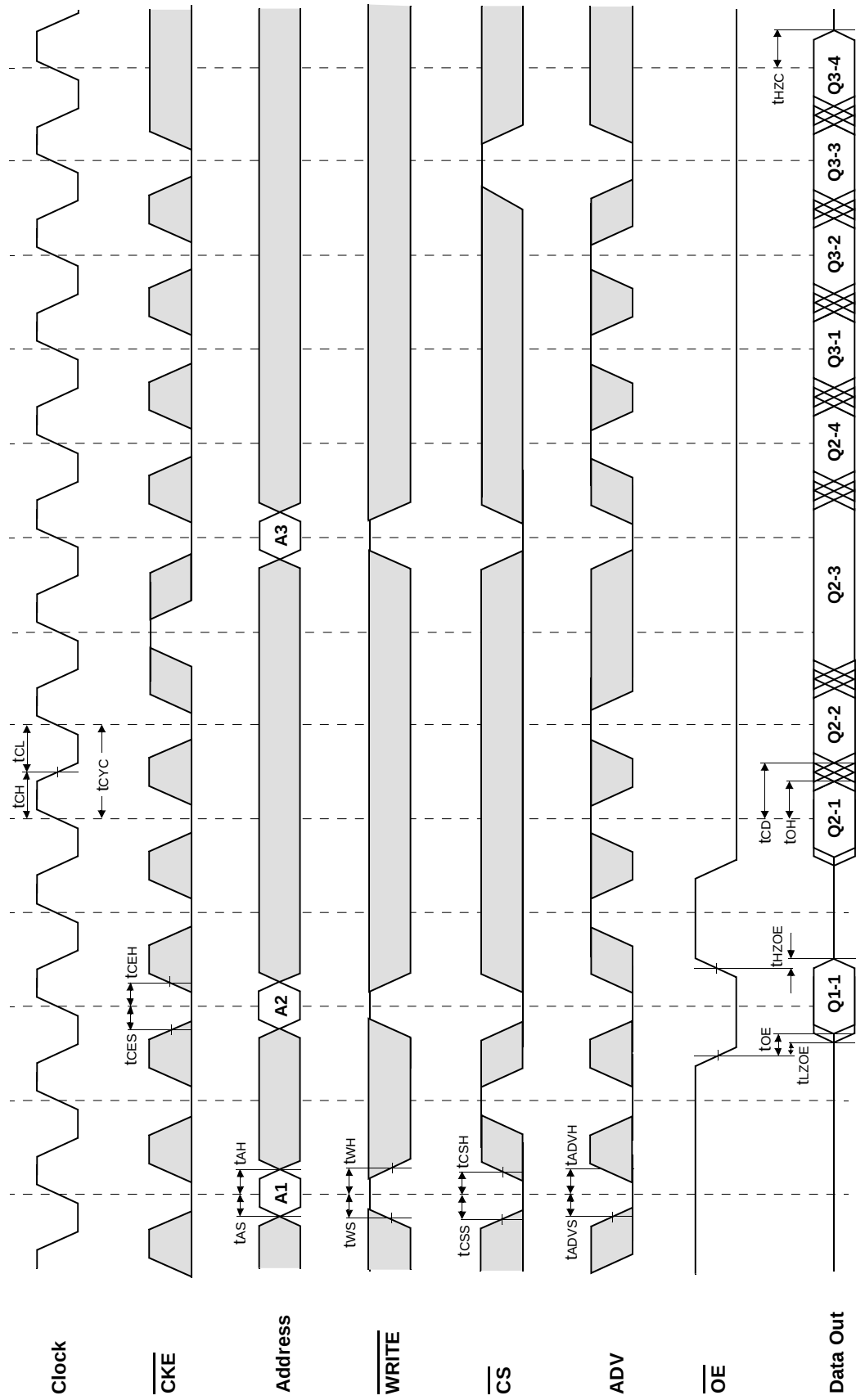
SLEEP MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		10	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

SLEEP MODE WAVEFORM



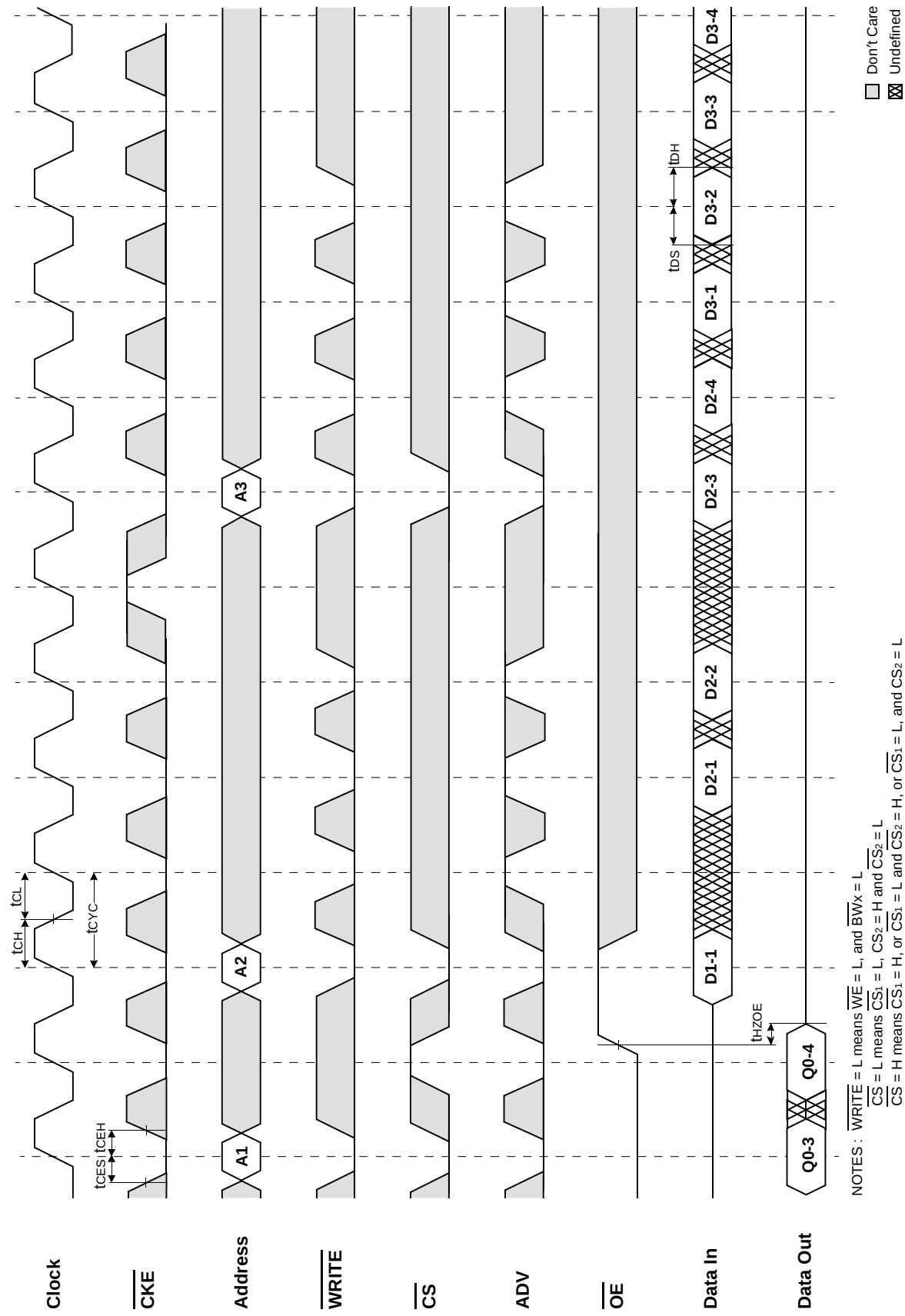
TIMING WAVEFORM OF READ CYCLE



NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS_1} = L$, $\overline{CS_2} = H$ and $\overline{CS_2} = L$
 $\overline{CS} = H$ means $\overline{CS_1} = H$, or $\overline{CS_1} = L$ and $\overline{CS_2} = H$, or $\overline{CS_1} = L$, and $\overline{CS_2} = L$

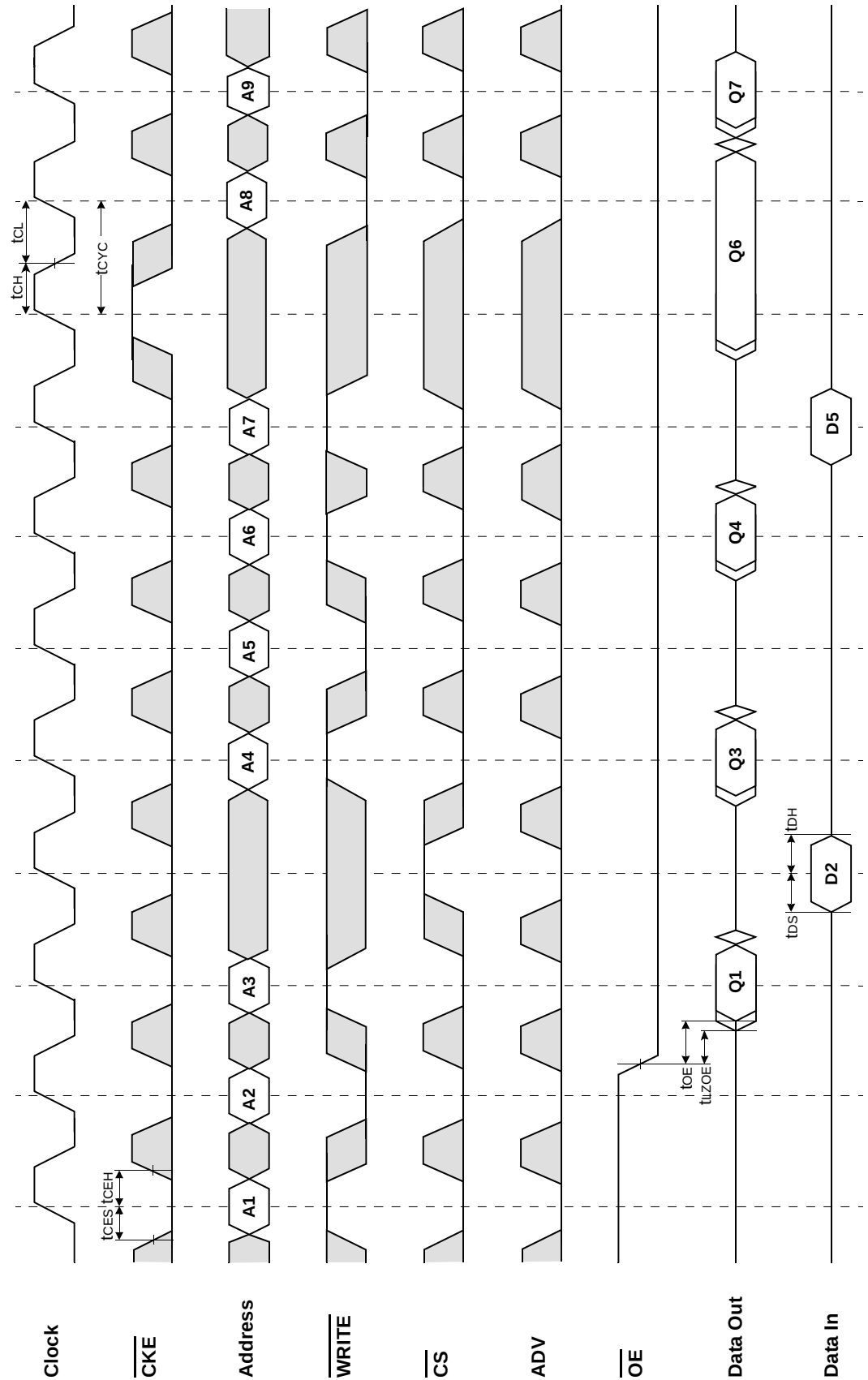
□ Don't Care
▣ Undefined

TIMING WAVEFORM OF WRTE CYCLE



NOTES : $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\overline{\text{CS}}_2 = \text{L}$

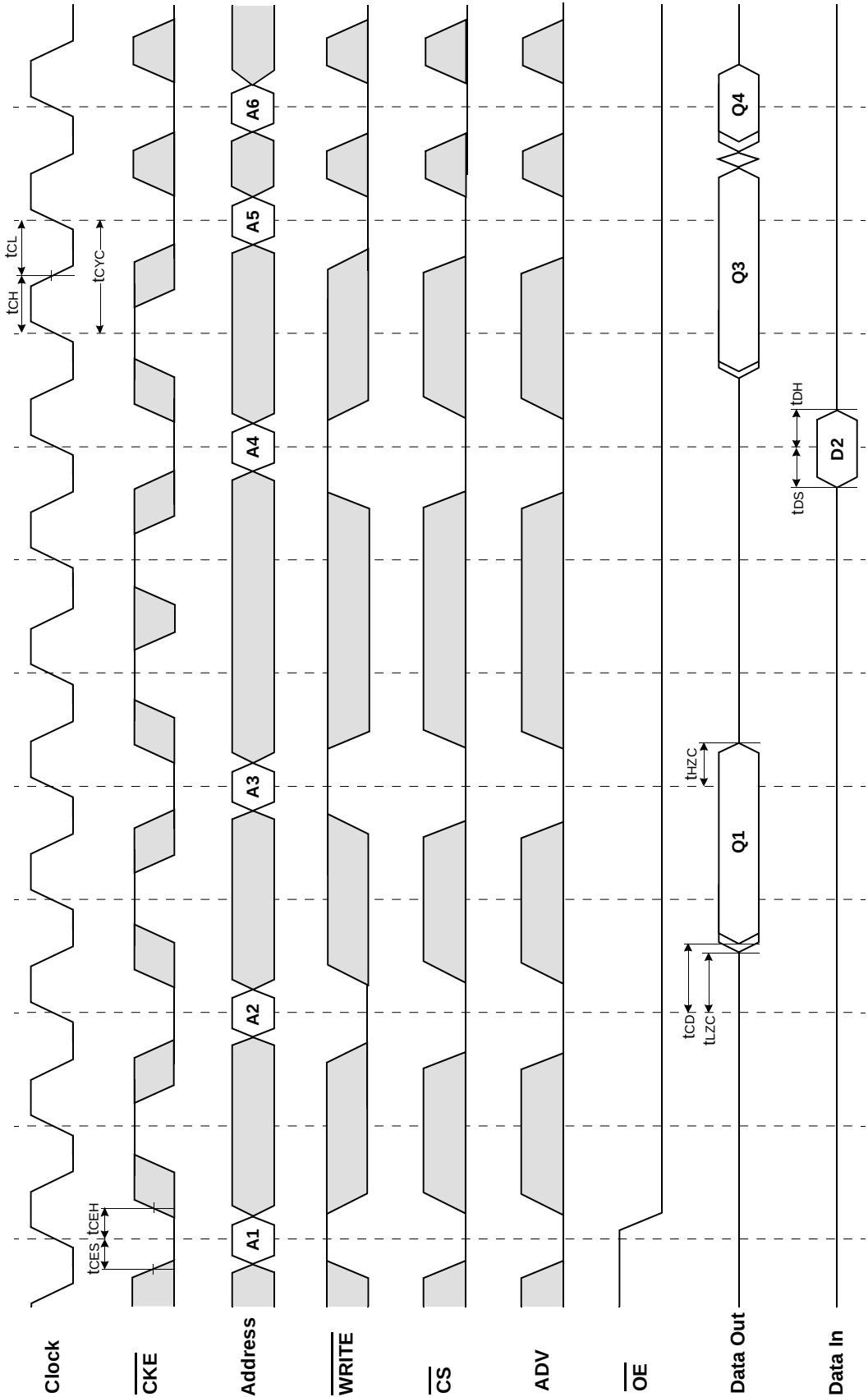
TIMING WAVEFORM OF SINGLE READWRITE



NOTES: $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BW}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\overline{\text{CS}}_2 = \text{L}$

□ Don't Care
⊗ Undefined

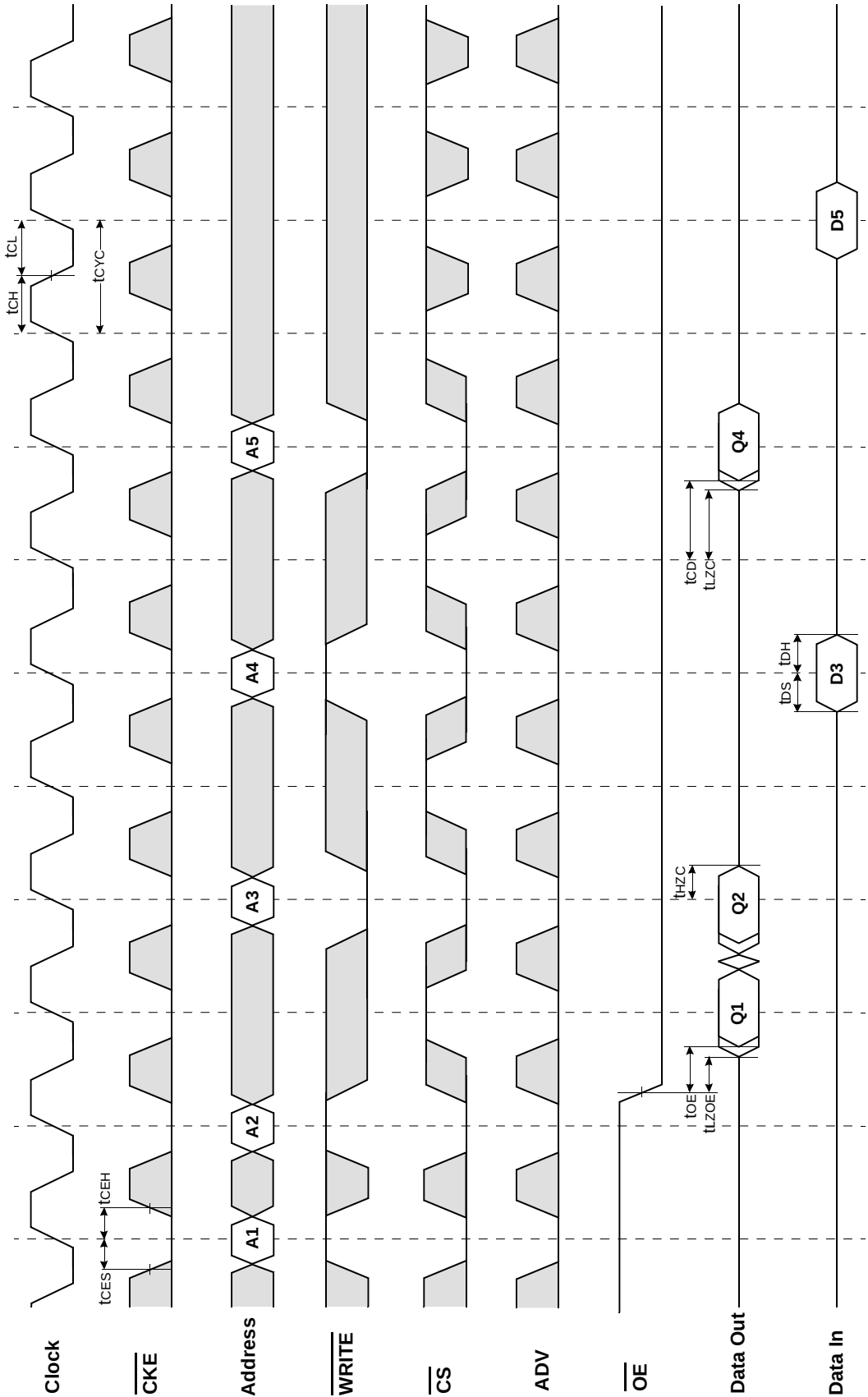
TIMING WAVEFORM OF CKE OPERATION



□ Don't Care
⊗ Undefined

NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS_1} = L$, $\overline{CS_2} = H$ and $\overline{CS_2} = L$
 $\overline{CS} = H$ means $\overline{CS_1} = H$, or $\overline{CS_1} = L$ and $\overline{CS_2} = H$, or $\overline{CS_1} = L$, and $\overline{CS_2} = L$

TIMING WAVEFORM OF CS OPERATION



NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS_1} = L$, $\overline{CS_2} = H$ and $\overline{CS_2} = L$
 $\overline{CS} = H$ means $\overline{CS_1} = H$, or $\overline{CS_1} = L$ and $\overline{CS_2} = H$, or $\overline{CS_1} = L$, and $\overline{CS_2} = L$

□ Don't Care
⊗ Undefined

PACKAGE DIMENSIONS

