TISP4070H3LM THRU TISP4095H3LM, TISP4125H3LM THRU TISP4220H3LM, TISP4240H3LM THRU TISP4400H3LM
BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

NOVEMBER 1997 - REVISED APRIL 1999

TELECOMMUNICATION SYSTEM HIGH CURRENT OVERVOLTAGE PROTECTORS

- **8 kV 10/700, 200 A 5/310 ITU-T K20/21 rating**
- **Ion-Implanted Breakdown Region**
  Precise and Stable Voltage
  Low Voltage Overshoot under Surge

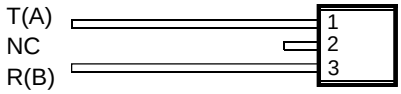
DEVICE	V_{DRM} V	$V_{(BO)}$ V
‘4070	58	70
‘4080	65	80
‘4095	75	95
‘4125	100	125
‘4145	120	145
‘4165	135	165
‘4180	145	180
‘4220	160	220
‘4240	180	240
‘4260	200	260
‘4300	230	300
‘4350	275	350
‘4400	300	400

- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	GR-1089-CORE	500
8/20 µs	IEC 61000-4-5	300
10/160 µs	FCC Part 68	250
10/700 µs	ITU-T K20/21 FCC Part 68	200
10/560 µs	FCC Part 68	160
10/1000 µs	GR-1089-CORE	100

- **Low Differential Capacitance . . . 80 pF max.**

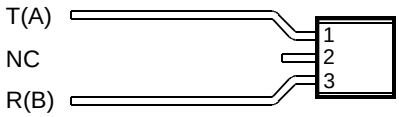
LM PACKAGE
(TOP VIEW)



MD4XAT

NC - No internal connection on pin 2

LMF PACKAGE
(LM PACKAGE WITH FORMED LEADS)
(TOP VIEW)



MD4XAKB

NC - No internal connection on pin 2

device symbol

SD4XAA

Terminals T and R correspond to the alternative line designators of A and B

- **Ordering Information**

DEVICE TYPE	PACKAGE TYPE
TISP4xxxH3LM	Straight Lead DO-92 Bulk Pack
TISP4xxxH3LMR	Straight Lead DO-92 Tape and Reeled
TISP4xxxH3LMFR	Formed Lead DO-92 Tape and Reeled

description

These devices are designed to limit overvoltages on the telephone line. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of 2-wire telecommunication equipment (e.g. between the Ring to Tip wires for telephones and modems). Combinations of devices can be used for multi-point protection (e.g. 3-point protection between Ring, Tip and Ground).

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

description (continued)

This TISP4xxxH3LM range consists of thirteen voltage variants to meet various maximum system voltage levels (58 V to 300 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These protection devices are supplied in a DO-92 (LM) cylindrical plastic package. The TISP4xxxH3LM is a straight lead DO-92 supplied in bulk pack and on tape and reeled. The TISP4xxxH3LMF is a formed lead DO-92 supplied only on tape and reeled.

absolute maximum ratings, T_A = 25°C (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, (see Note 1)	‘4070	V_{DRM}	± 58	V
	‘4080		± 65	
	‘4095		± 75	
	‘4125		±100	
	‘4145		±120	
	‘4165		±135	
	‘4180		±145	
	‘4220		±160	
	‘4240		±180	
	‘4260		±200	
	‘4300		±230	
	‘4350		±275	
	‘4400		±300	
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)				
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)		I_{TSP}	500	A
8/20 µs (IEC 61000-4-5, combination wave generator, 1.2/50 voltage, 8/20 current)			300	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)			250	
5/200 µs (VDE 0433, 10/700 µs voltage wave shape)			220	
0.2/310 µs (I 31-24, 0.5/700 µs voltage wave shape)			200	
5/310 µs (ITU-T K20/21, 10/700 µs voltage wave shape)			200	
5/310 µs (FTZ R12, 10/700 µs voltage wave shape)			200	
5/320 µs (FCC Part 68, 9/720 µs voltage wave shape)			200	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)			160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			100	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)				
20 ms (50 Hz) full sine wave		I_{TSM}	55	A
16.7 ms (60 Hz) full sine wave			60	
1000 s 50 Hz/60 Hz a.c.			2.3	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 100 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. See Applications Information and Figure 10 for voltage values at lower temperatures.
2. Initially the TISP4xxxH3LM must be in thermal equilibrium with T_J = 25°C.
3. The surge may be repeated after the TISP4xxxH3LM returns to its initial conditions.
4. See Applications Information and Figure 11 for current ratings at other temperatures.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 8 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C

electrical characteristics for the T and R terminals, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DRM}	Repetitive peak off-state current	$V_D = \pm V_{DRM}$	T_A = 25°C			±5	µA
			T_A = 85°C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'4070			±70	V
			'4080			±80	
			'4095			±95	
			'4125			±125	
			'4145			±145	
			'4165			±165	
			'4180			±180	
			'4220			±220	
			'4240			±240	
			'4260			±260	
			'4300			±300	
			'4350			±350	
			'4400			±400	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'4070			±78	V
			'4080			±88	
			'4095			±102	
			'4125			±132	
			'4145			±151	
			'4165			±171	
			'4180			±186	
			'4220			±227	
			'4240			±247	
			'4260			±267	
			'4300			±308	
			'4350			±359	
			'4400			±410	
$I_{(BO)}$	Breakover current	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.6	A
V_T	On-state voltage	I_T = ±5 A, t_W = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15		±0.6	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85°C			±10	µA
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 1 V rms, V_D = 0,	'4070 thru '4095		172	218	pF
			'4125 thru '4220		95	120	
			'4240 thru '4400		92	115	
		f = 100 kHz, V_d = 1 V rms, V_D = -1 V	'4070 thru '4095		157	200	
			'4125 thru '4220		85	110	
			'4240 thru '4400		80	100	
		f = 100 kHz, V_d = 1 V rms, V_D = -2 V	'4070 thru '4095		145	185	
			'4125 thru '4220		78	100	
			'4240 thru '4400		72	90	
		f = 100 kHz, V_d = 1 V rms, V_D = -50 V	'4070 thru '4095		70	90	
			'4125 thru '4220		33	43	
			'4240 thru '4400		28	35	
		f = 100 kHz, V_d = 1 V rms, V_D = -100 V (see Note 6)	'4125 thru '4220		25	33	
			'4240 thru '4400		22	28	

NOTE 6: To avoid possible voltage clipping, the '4125 is tested with V_D = -98 V.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 7)			105	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C		55		

NOTE 7: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

PARAMETER MEASUREMENT INFORMATION

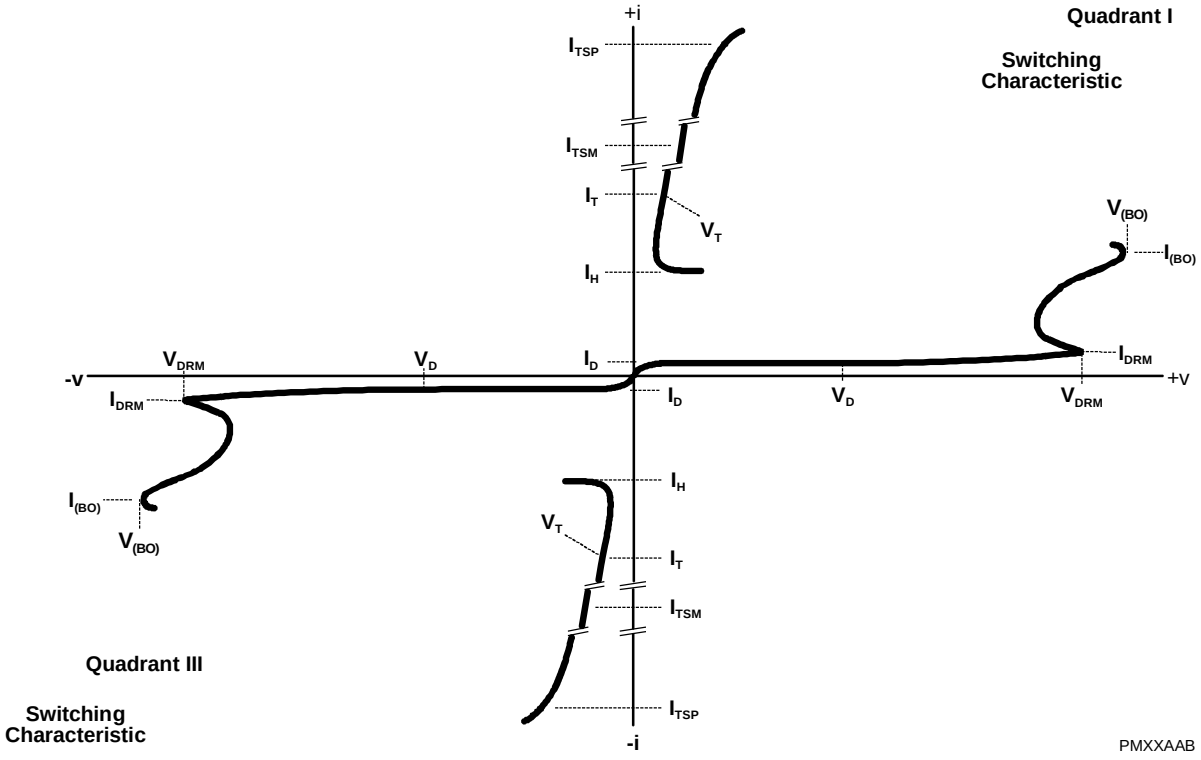


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR T AND R TERMINALS
ALL MEASUREMENTS ARE REFERENCED TO THE R TERMINAL

TYPICAL CHARACTERISTICS

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

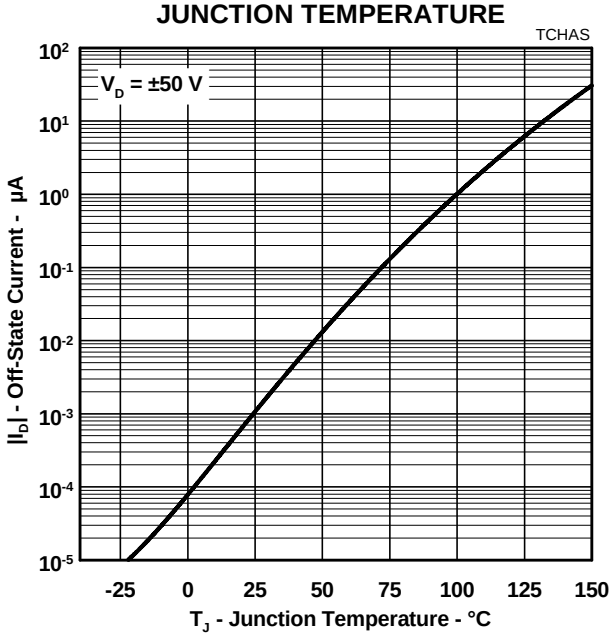


Figure 2.

NORMALISED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

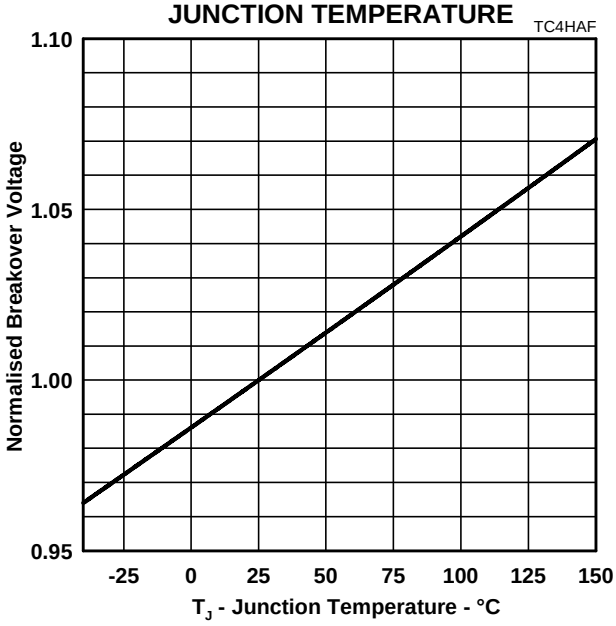


Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

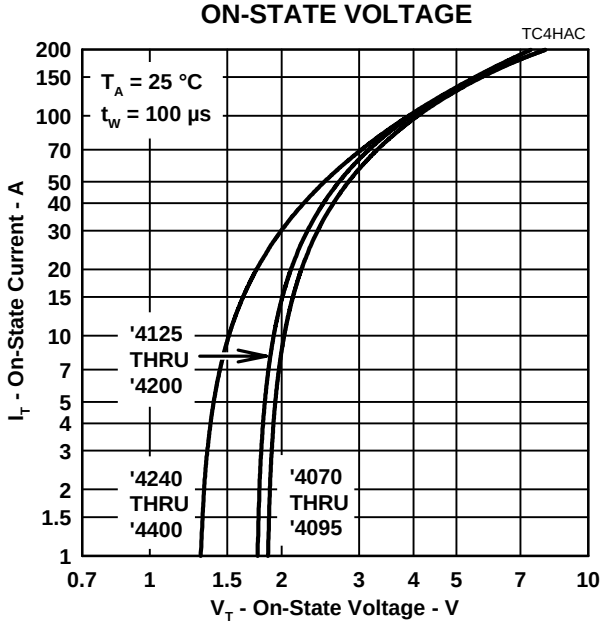


Figure 4.

NORMALISED HOLDING CURRENT vs JUNCTION TEMPERATURE

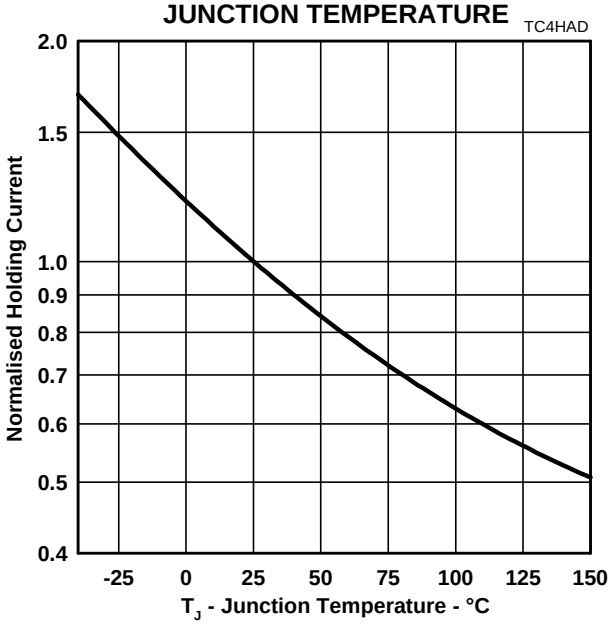


Figure 5.

TYPICAL CHARACTERISTICS

NORMALISED CAPACITANCE
vs
OFF-STATE VOLTAGE

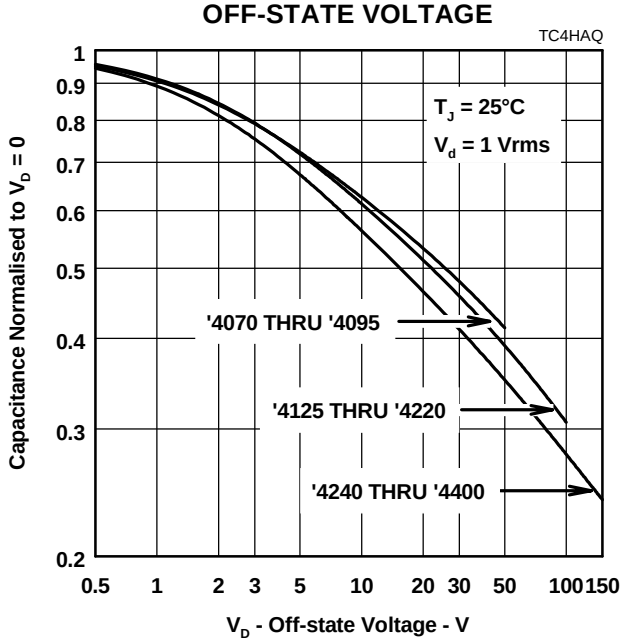


Figure 6.

DIFFERENTIAL OFF-STATE CAPACITANCE
vs
RATED REPETITIVE PEAK OFF-STATE VOLTAGE

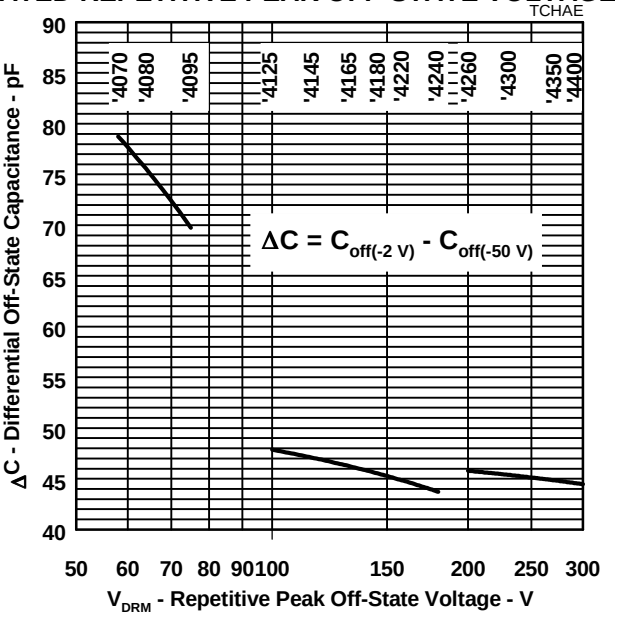


Figure 7.

RATING AND THERMAL INFORMATION

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

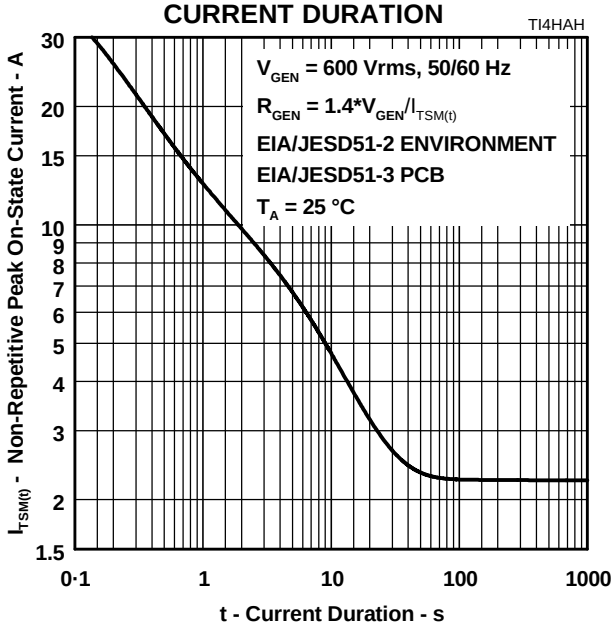


Figure 8.

THERMAL IMPEDANCE vs POWER DURATION

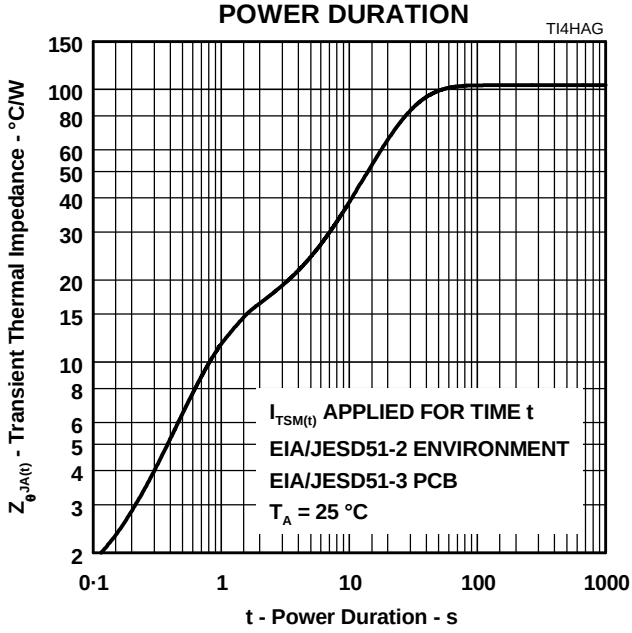


Figure 9.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

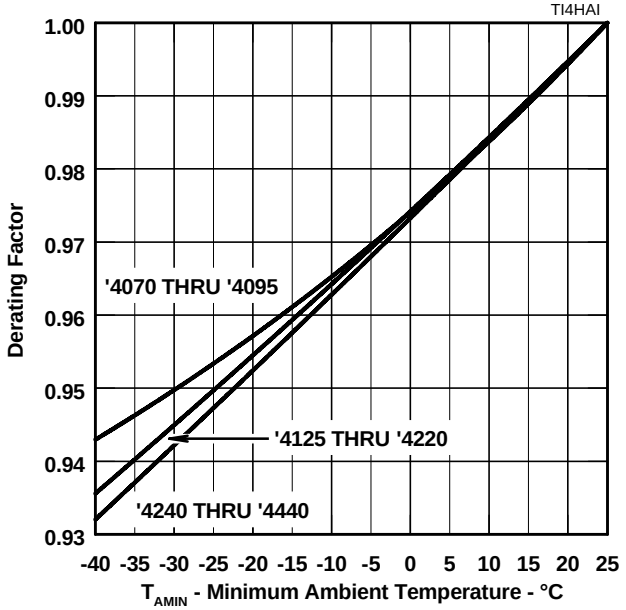


Figure 10.

IMPULSE RATING vs AMBIENT TEMPERATURE

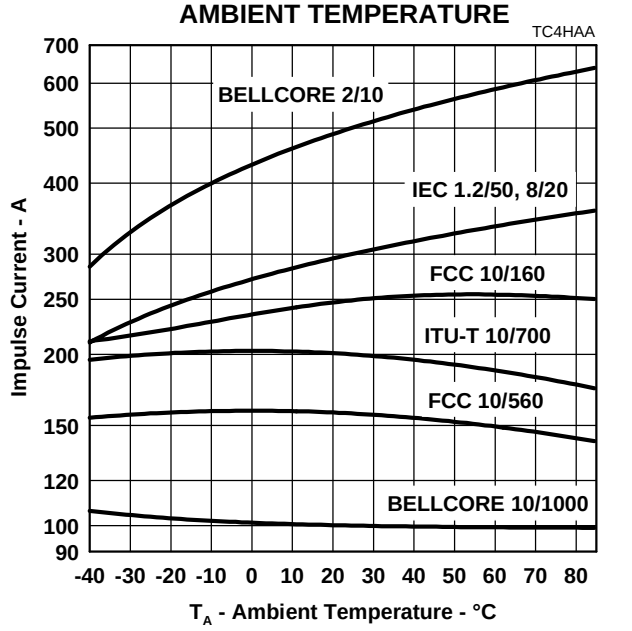


Figure 11.

APPLICATIONS INFORMATION

deployment

These devices are two terminal overvoltage protectors. They may be used either singly to limit the voltage between two conductors (Figure 12) or in multiples to limit the voltage at several points in a circuit (Figure 13).

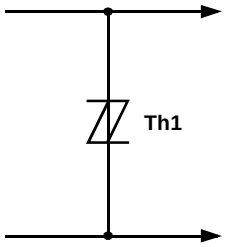


Figure 12. TWO POINT PROTECTION

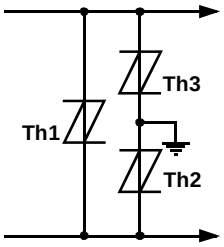


Figure 13. MULTI-POINT PROTECTION

In Figure 12, protector Th1 limits the maximum voltage between the two conductors to $\pm V_{(BO)}$. This configuration is normally used to protect circuits without a ground reference, such as modems. In Figure 13, protectors Th2 and Th3 limit the maximum voltage between each conductor and ground to the $\pm V_{(BO)}$ of the individual protector. Protector Th1 limits the maximum voltage between the two conductors to its $\pm V_{(BO)}$ value. If the equipment being protected has all its vulnerable components connected between the conductors and ground, then protector Th1 is not required.

impulse testing

To verify the withstand capability and safety of the equipment, standards require that the equipment is tested with various impulse wave forms. The table below shows some common values.

STANDARD	PEAK VOLTAGE SETTING V	VOLTAGE WAVE FORM µs	PEAK CURRENT VALUE A	CURRENT WAVE FORM µs	TISP4xxxH3 25 °C RATING A	SERIES RESISTANCE Ω
GR-1089-CORE	2500	2/10	500	2/10	500	0
	1000	10/1000	100	10/1000	100	
FCC Part 68 (March 1998)	1500	10/160	200	10/160	250	0
	800	10/560	100	10/560	160	0
	1500	9/720 †	37.5	5/320 †	200	0
	1000	9/720 †	25	5/320 †	200	0
I3124	1500	0.5/700	37.5	0.2/310	200	0
ITU-T K20/K21	1500 4000	10/700	37.5 100	5/310	200	0

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K21 10/700 impulse generator

If the impulse generator current exceeds the protectors current rating then a series resistance can be used to reduce the current to the protectors rated value and so prevent possible failure. The required value of series resistance for a given waveform is given by the following calculations. First, the minimum total circuit impedance is found by dividing the impulse generators peak voltage by the protectors rated current. The impulse generators fictive impedance (generators peak voltage divided by peak short circuit current) is then subtracted from the minimum total circuit impedance to give the required value of series resistance. In some cases the equipment will require verification over a temperature range. By using the rated waveform values from Figure 11, the appropriate series resistor value can be calculated for ambient temperatures in the range of -40 °C to 85 °C.

a.c. power testing

The protector can withstand currents applied for times not exceeding those shown in Figure 8. Currents that exceed these times must be terminated or reduced to avoid protector failure. Fuses, PTC (Positive Temperature Coefficient) resistors and fusible resistors are overcurrent protection devices which can be used to reduce the current flow. Protective fuses may range from a few hundred milliamperes to one ampere. In some cases it may be necessary to add some extra series resistance to prevent the fuse opening during impulse testing. The current versus time characteristic of the overcurrent protector must be below the line shown in Figure 8. In some cases there may be a further time limit imposed by the test standard (e.g. UL 1459 wiring simulator failure).

capacitance

The protector characteristic off-state capacitance values are given for d.c. bias voltage, V_D, values of 0, -1 V, -2 V and -50 V. Where possible values are also given for -100 V. Values for other voltages may be calculated by multiplying the V_D = 0 capacitance value by the factor given in Figure 6. Up to 10 MHz the capacitance is essentially independent of frequency. Above 10 MHz the effective capacitance is strongly dependent on connection inductance. In many applications, such as Figure 15 and Figure 17, the typical conductor bias voltages will be about -2 V and -50 V. Figure 7 shows the differential (line unbalance) capacitance caused by biasing one protector at -2 V and the other at -50 V.

normal system voltage levels

The protector should not clip or limit the voltages that occur in normal system operation. For unusual conditions, such as ringing without the line connected, some degree of clipping is permissible. Under this condition about 10 V of clipping is normally possible without activating the ring trip circuit.

Figure 10 allows the calculation of the protector V_{DRM} value at temperatures below 25 °C. The calculated value should not be less than the maximum normal system voltages. The TISP4260H3LM, with a V_{DRM} of 200 V, can be used for the protection of ring generators producing 100 V rms of ring on a battery voltage of -58 V (Th2 and Th3 in Figure 17). The peak ring voltage will be 58 + 1.414*100 = 199.4 V. However, this is the open circuit voltage and the connection of the line and its equipment will reduce the peak voltage. In the extreme case of an unconnected line, clipping the peak voltage to 190 V should not activate the ring trip. This level of clipping would occur at the temperature when the V_{DRM} has reduced to 190/200 = 0.95 of its 25 °C value. Figure 10 shows that this condition will occur at an ambient temperature of -22 °C. In this example, the TISP4260H3LM will allow normal equipment operation provided that the minimum expected ambient temperature does not fall below -22 °C.

JESD51 thermal measurement method

To standardise thermal measurements, the EIA (Electronic Industries Alliance) has created the JESD51 standard. Part 2 of the standard (JESD51-2, 1995) describes the test environment. This is a 0.0283 m^3 (1 ft^3) cube which contains the test PCB (Printed Circuit Board) horizontally mounted at the centre. Part 3 of the standard (JESD51-3, 1996) defines two test PCBs for surface mount components; one for packages smaller than 27 mm on a side and the other for packages up to 48 mm. The LM package measurements used the smaller 76.2 mm x 114.3 mm (3.0 “ x 4.5 “) PCB. The JESD51-3 PCBs are designed to have low effective thermal conductivity (high thermal resistance) and represent a worse case condition. The PCBs used in the majority of applications will achieve lower values of thermal resistance and so can dissipate higher power levels than indicated by the JESD51 values.

typical circuits

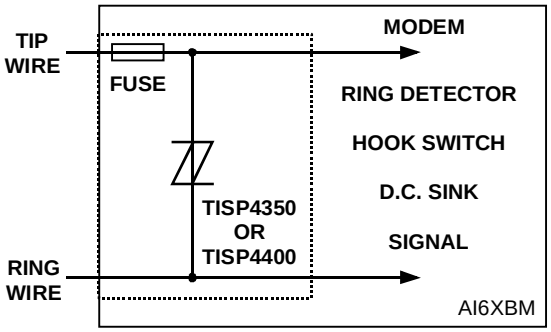


Figure 14. MODEM INTER-WIRE PROTECTION

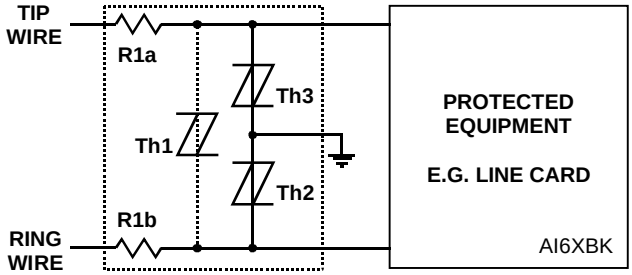


Figure 15. PROTECTION MODULE

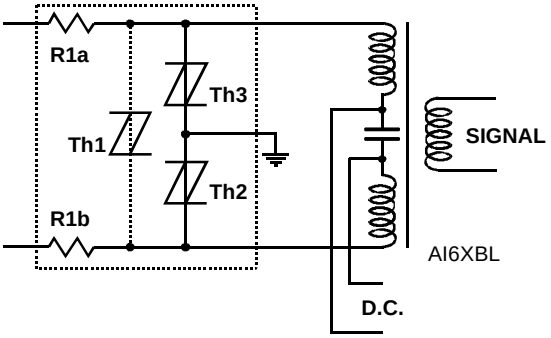


Figure 16. ISDN PROTECTION

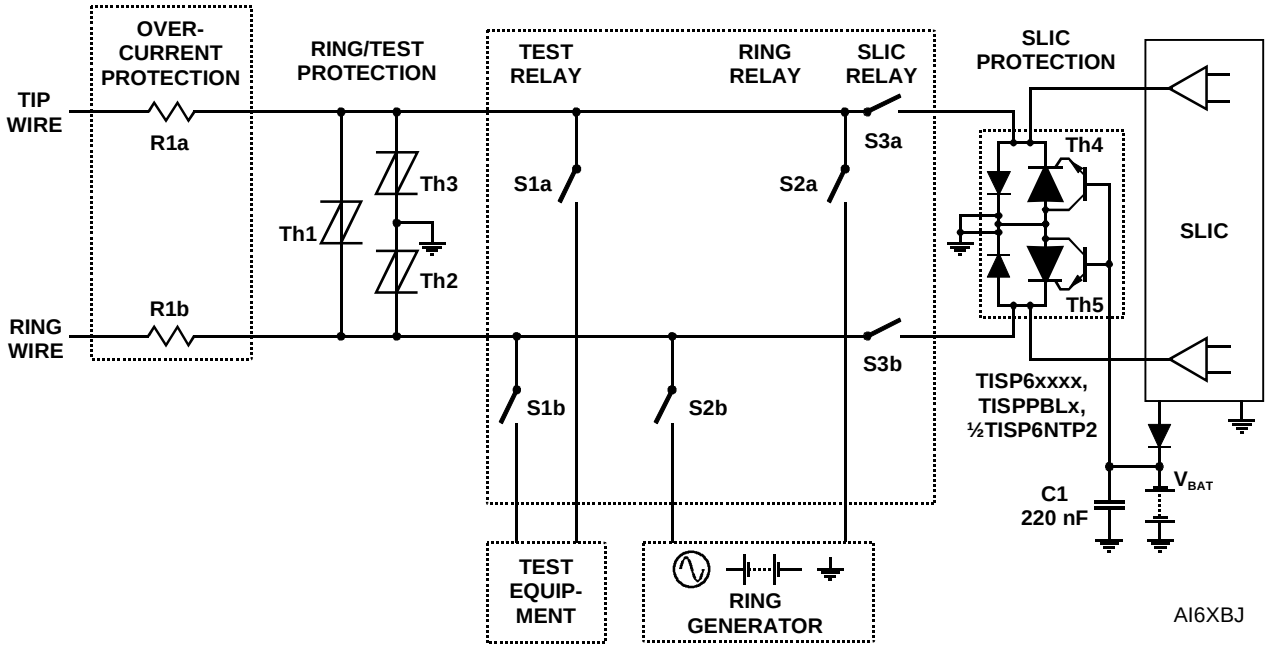


Figure 17. LINE CARD RING/TEST PROTECTION

MECHANICAL DATA

device symbolization code

Devices will be coded as below.

DEVICE	SYMOBLIZATION CODE
TISP4070H3	4070H3
TISP4080H3	4080H3
TISP4095H3	4095H3
TISP4125H3	4125H3
TISP4145H3	4145H3
TISP4165H3	4165H3
TISP4180H3	4180H3
TISP4220H3	4220H3
TISP4240H3	4240H3
TISP4260H3	4260H3
TISP4300H3	4300H3
TISP4350H3	4350H3
TISP4400H3	4400H3

carrier information

Devices are shipped in one of the carriers below. A reel contains 2 000 devices.

PACKAGE TYPE	CARRIER	ORDER #
Straight Lead DO-92	Bulk Pack	TISP4xxxH3LM
Straight Lead DO-92	Tape and Reeled	TISP4xxxH3LMR
Formed Lead DO-92	Tape and Reeled	TISP4xxxH3LMFR

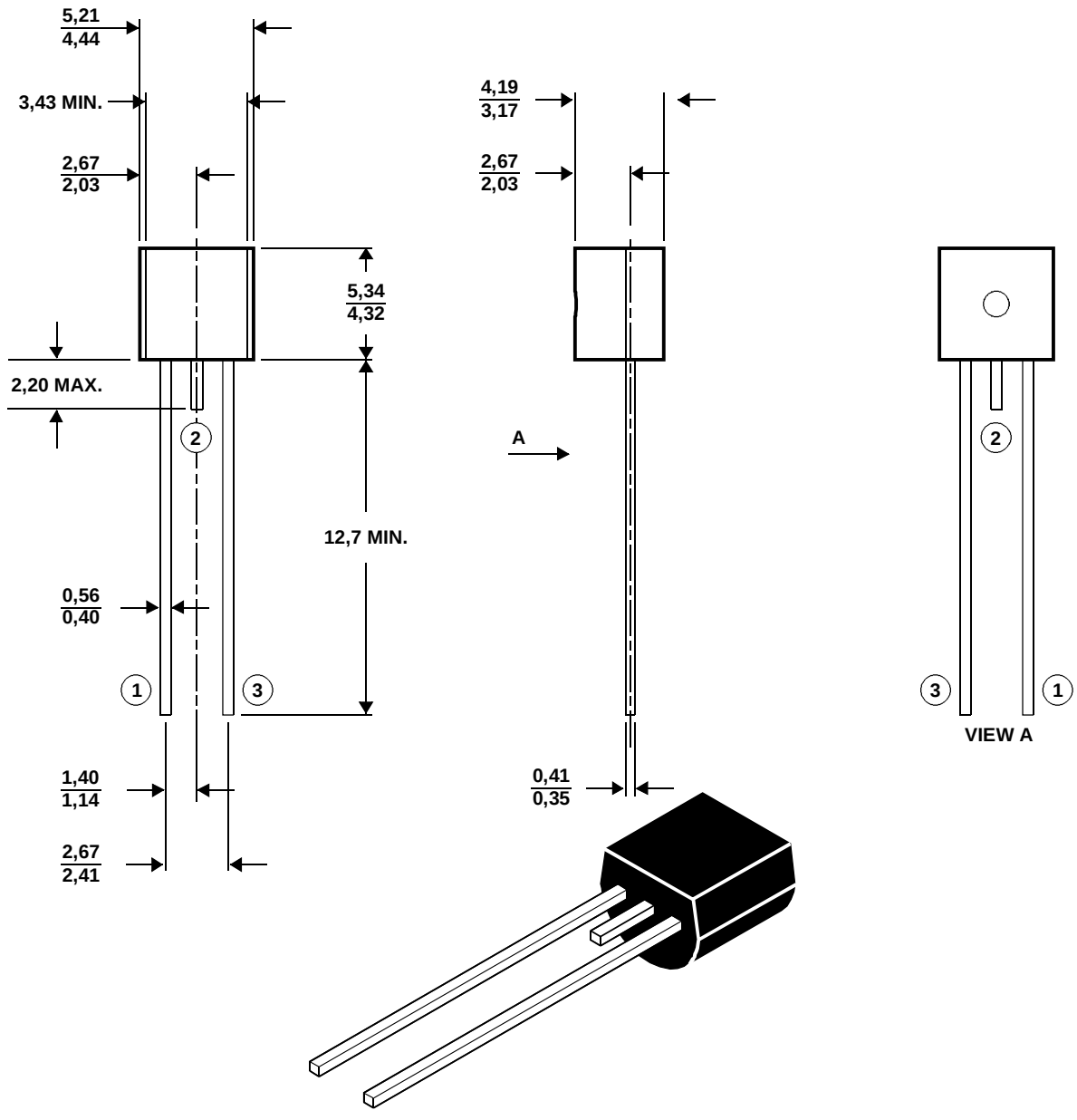
MECHANICAL DATA

LM002 (DO-92)

2-pin cylindrical plastic package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly. .

LM002 Package (DO-92)



ALL LINEAR DIMENSIONS IN MILLIMETERS

MD4XARA

PRODUCT INFORMATION

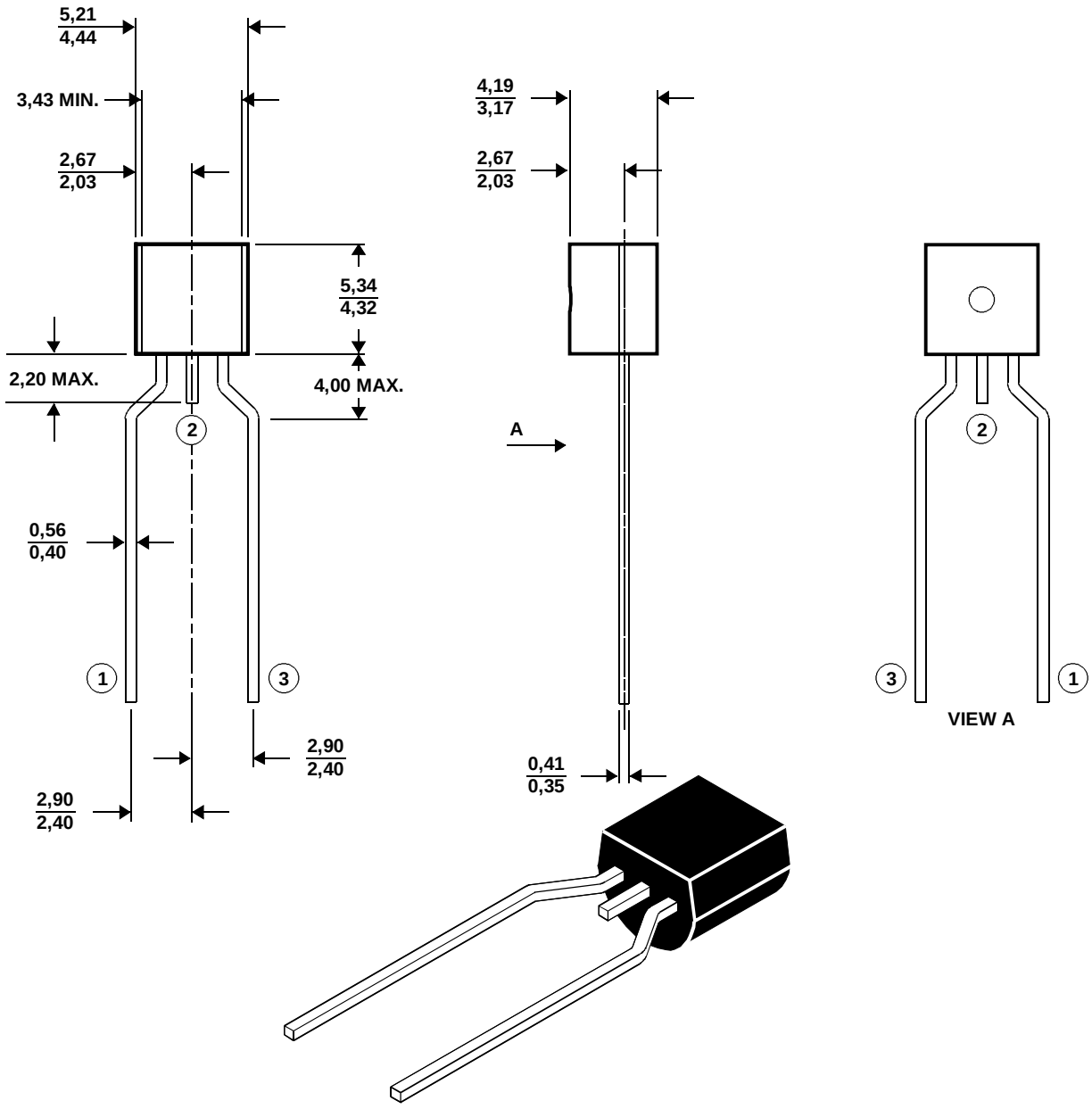
MECHANICAL DATA

LM002 (DO-92) - Formed Leads Version

2-pin cylindrical plastic package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LMF002 (DO-92) - Formed Leads Version of LM002

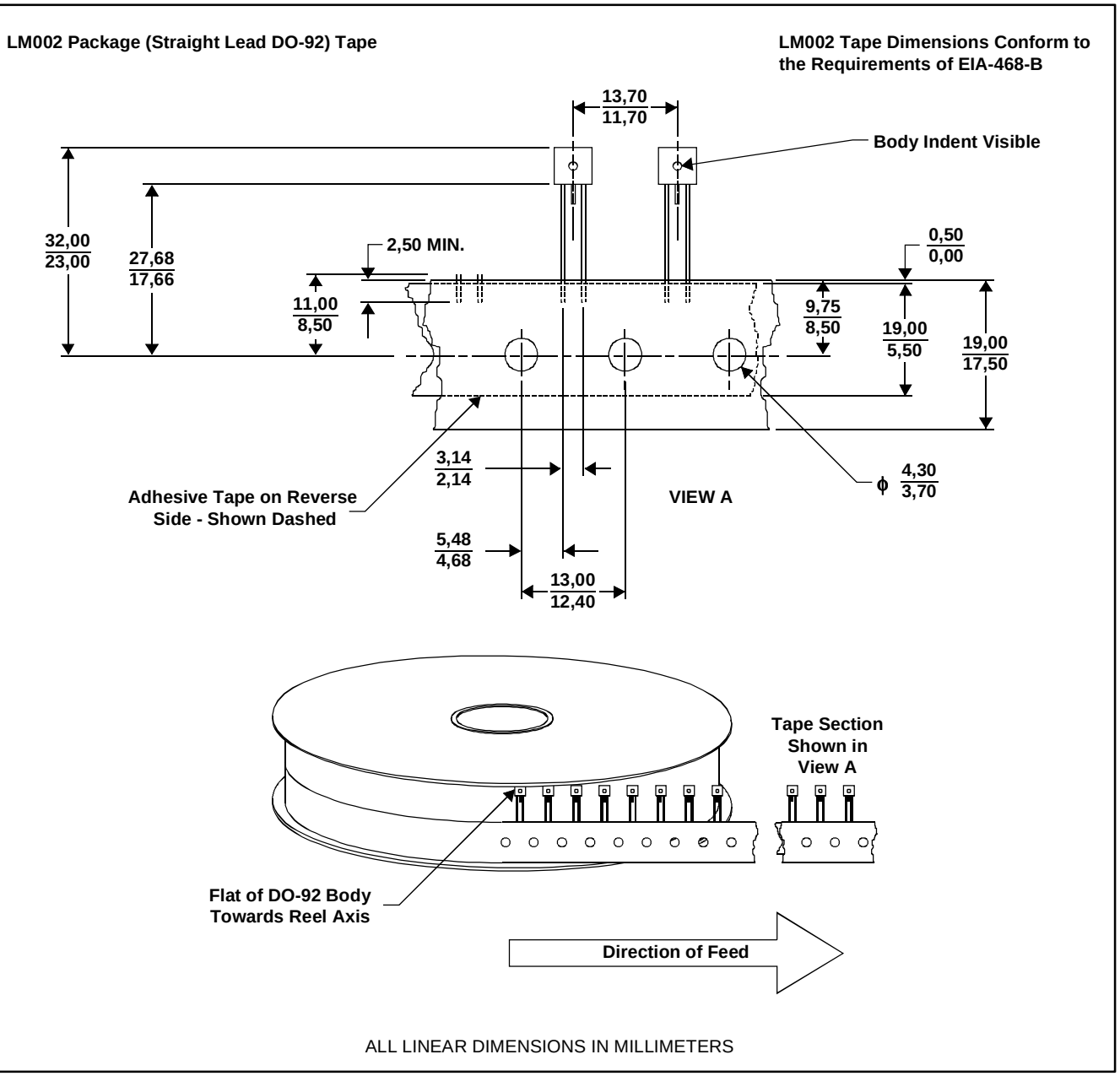


ALL LINEAR DIMENSIONS IN MILLIMETERS

MD4XASA

MECHANICAL DATA

tape dimensions



ALL LINEAR DIMENSIONS IN MILLIMETERS

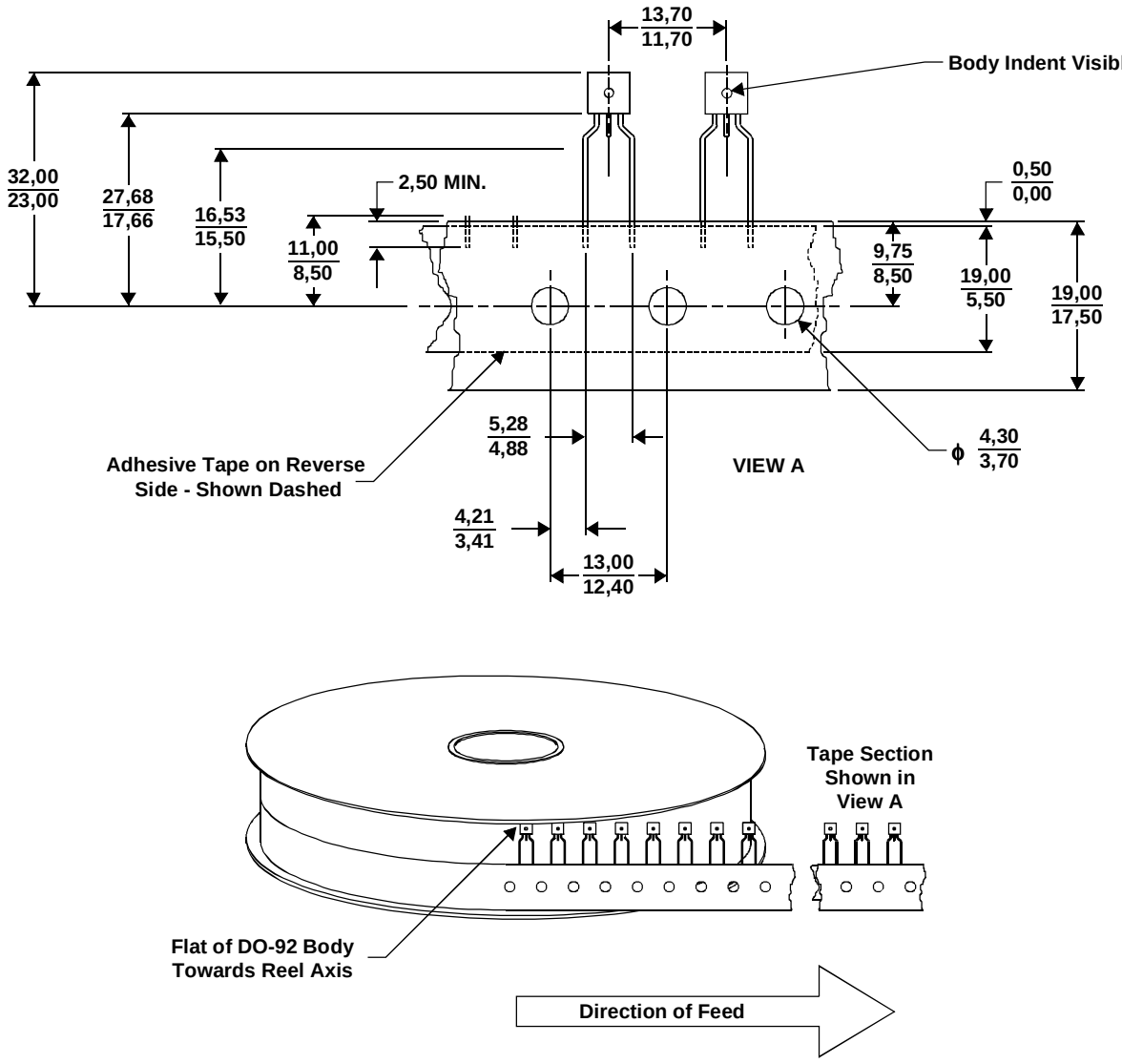
MD4XAPC

MECHANICAL DATA

tape dimensions

LMF002 Package (Formed Lead DO-92) Tape

LMF002 Tape Dimensions Conform to the Requirements of EIA-468-B



ALL LINEAR DIMENSIONS IN MILLIMETERS

MD4XAQC

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