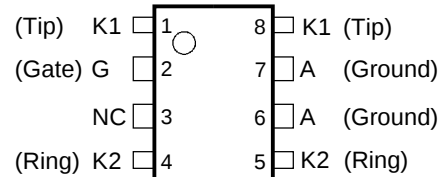


PROGRAMMABLE SLIC OVERVOLTAGE PROTECTION

- **Programmable Voltage Triggered SCR with high Holding Current**
- **Transistor Buffered Inputs for Low V_{GG} current**
- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
10/700 μ s	CCITT IX K17	38
10/1000 μ s	REA PE-60	30

P PACKAGE
(TOP VIEW)



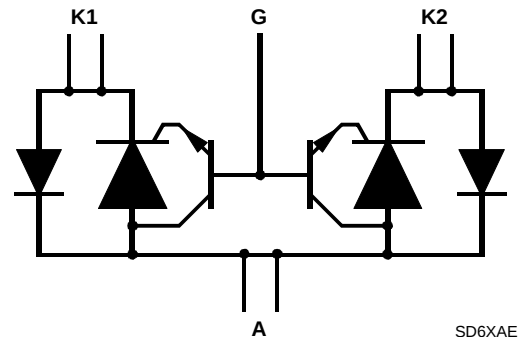
NC - No internal connection
 Terminal typical application names shown in parenthesis
 MD6XAV

description

The TISP61CAP3 is a programmable overvoltage protector designed to protect SLIC applications against lightning and transients induced by ac power lines. Normally the V_{GG} (Gate) terminal will be connected to the negative supply rail of the SLIC

When a negative transient exceeds the negative supply rail voltage of the SLIC it will cause the thyristor to crowbar, shunting the surge to ground. The high crowbar holding current prevents dc latchup as the transient subsides. Positive transients are clipped by diode action.

device symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, V_{GG} , applied to the G terminal.

absolute maximum ratings

RATING	SYMBOL	VALUE	UNIT
Non-repetitive peak on-state pulse current (see Notes 1, 2 and 3) 5/310 μ s (CCITT IX K17, open-circuit voltage wave shape 1.5 kV, 10/700 μ s) 10/1000 μ s (REA PE-60, open-circuit voltage wave shape 10/1000 μ s)	I_{TSP}	38 30	A
Non-repetitive peak on-state current, 50 Hz, 1 s (see Notes 1 and 2)	I_{TSM}	2.5	A rms
Maximum gate current	I_{GM}	2	A
Repetitive peak off-state voltage	V_{DRM}	- 80	V
Maximum gate supply voltage	$V_{GG(max)}$	- 80	V

- NOTES: 1. Above 70°C, derate linearly to zero at 150°C case temperature
 2. This value applies when the initial case temperature is at (or below) 70°C. The surge may be repeated after the device has returned to thermal equilibrium.
 3. Most PTT's quote an unloaded voltage waveform. In operation the TISP essentially shorts the generator output. The resulting loaded current waveform is specified.

PRODUCT INFORMATION

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.

TISP61CAP3

PROGRAMMABLE

OVERVOLTAGE PROTECTOR

SEPTEMBER 1994 - REVISED SEPTEMBER 1997

electrical characteristics, $T_J = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F Forward voltage	$I_F = 5\text{ A}$			3	V
V_{FR} Forward recovery voltage	$dv/dt = 300\text{ V}/\mu\text{s}$ $di/dt < 10\text{ A}/\mu\text{s}$ $R_{SOURCE} = 30\ \Omega$			7	V
$V_{GK(BO)}$ Gate cathode voltage at breakover ($V_{(BO)} - V_{GG}$)	$dv/dt = -250\text{ V}/\text{ms}$ $-72 < V_{GG} < -10\text{ V}$ $R_{SOURCE} = 300\ \Omega$			-3	V
$V_{GK(BO)}$ Impulse gate cathode voltage at breakover ($V_{(BO)} - V_{GG}$)	$dv/dt = -300\text{ V}/\mu\text{s}$ $di/dt < -10\text{ A}/\mu\text{s}$ $R_{SOURCE} = 30\ \Omega$			-15	V
V_T On-state voltage	$I_T = -4\text{ A}$ $-72 < V_{GG} < -10\text{ V}$			-3	V
I_D Off-state current	$V_D = -80\text{ V}$ $V_{GG} = -80\text{ V}$			-10	μA
I_S Switching current	$dv/dt = -250\text{ V}/\text{ms}$ $-72 < V_{GG} < -10\text{ V}$ $R_{SOURCE} = 300\ \Omega$	-0.15			A
I_H Holding current	$di/dt = 30\text{ mA}/\mu\text{s}$ $-72 < V_{GG} < -10\text{ V}$	-0.15			A
I_{GAO} Gate reverse current with cathode open	$V_{GG} = -72\text{ V}$			-10	μA
I_{GAT} Gate reverse current in the on-state	$V_{GG} = -72\text{ V}$ $I_T = -0.5\text{ A}$			-1	mA
I_{GAF} Gate reverse current in the forward conducting state	$V_{GG} = -72\text{ V}$ $I_T = 1\text{ A}$ $I_T = 5\text{ A}$		-10 -30		mA
I_{GSM} Peak gate switching current	$dv/dt = -250\text{ V}/\text{ms}$ $-72 < V_{GG} < -10\text{ V}$ $R_{SOURCE} = 300\ \Omega$			5	mA
C_{off} Off-state capacitance	$-72 < V_{GG} < -10\text{ V}$ $V_D = -3\text{ V}$ $V_D = -48\text{ V}$ (see Note 4)			150 80	pF
dv/dt Critical rate of rise of off-state voltage	$V_{GG} = -72\text{ V}$, linear ramp, Maximum ramp value $> 0.85 V_{GG}$	-50			V/ μs

NOTE 4: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.

PARAMETER MEASUREMENT INFORMATION

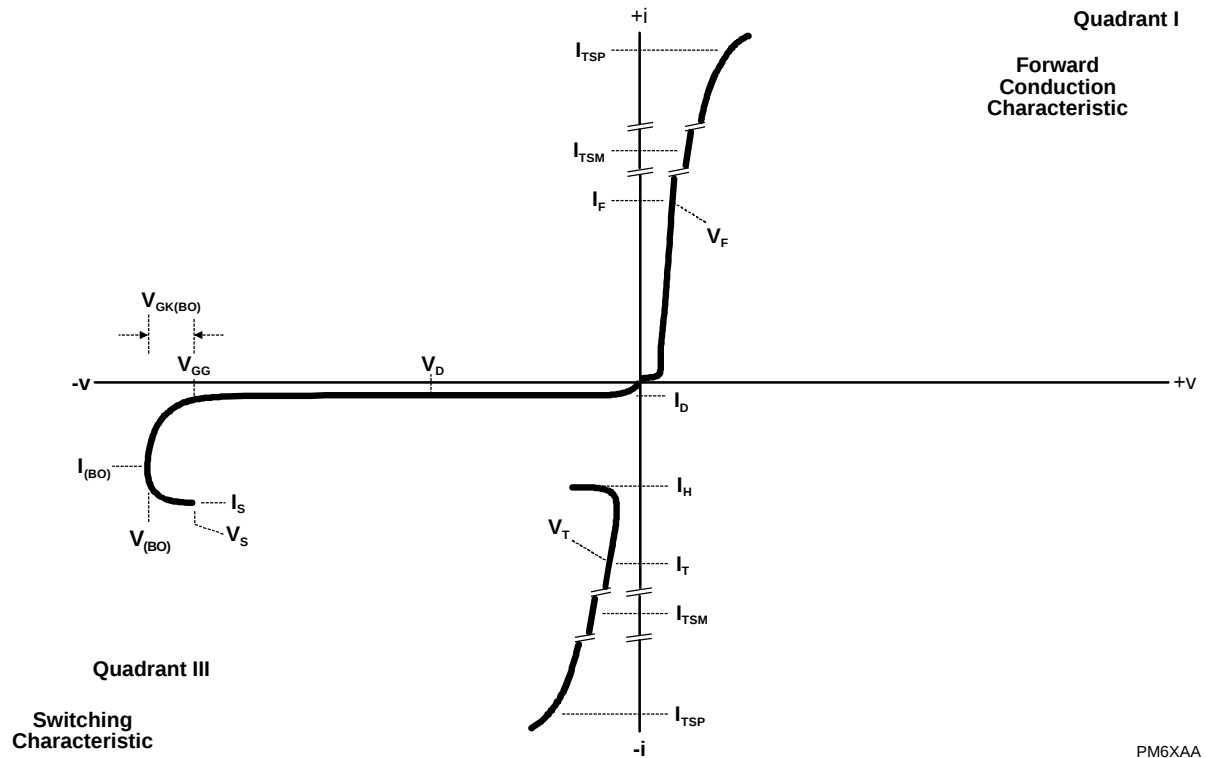


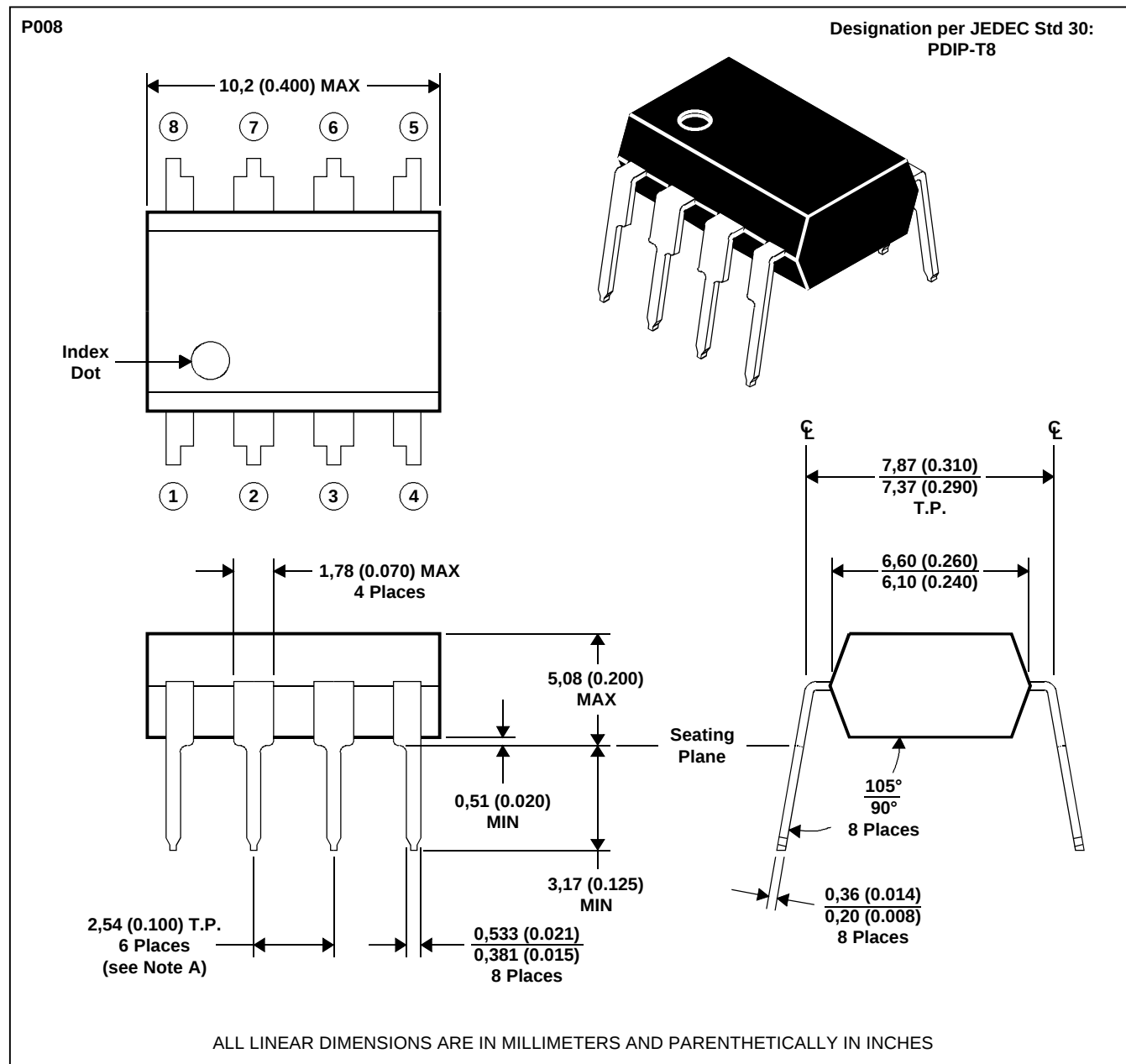
Figure 1. VOLTAGE-CURRENT CHARACTERISTIC

MECHANICAL DATA

P008

plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position

MDXXABA

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