AN6387

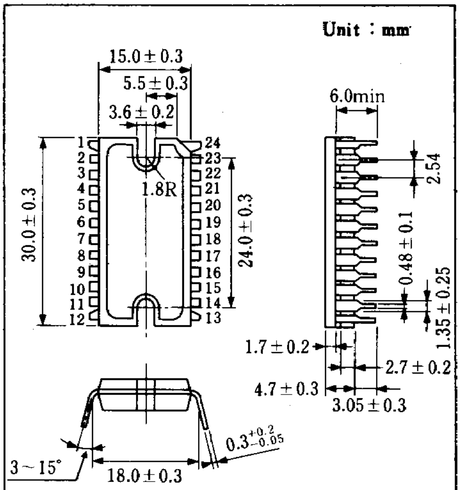
VCR Cylinder Direct Motor Drive Circuit

■ Outline

The AN6387 is an integrated circuit designed to drive a VCR cylinder DD motor.

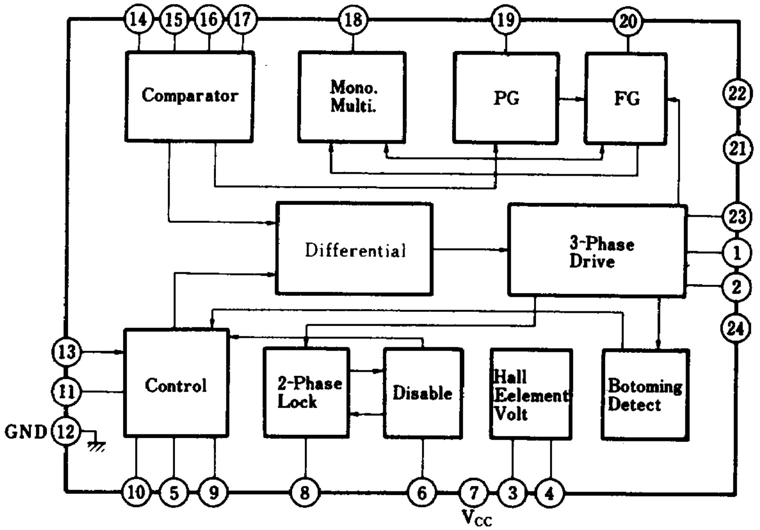
■ Features

- The functions consist of :
  - 3-Phase motor drive circuit
  - 2-Phase Hall element input circuit
  - PG, FG, generator circuit
  - Motor lock detector
- Supply voltage : either 9V or 12V



24-Lead DIL Plastic Package(Power Type)

■ Block Diagram



■ Pin

Pin No.	Pin Name		Pin No.	Pin Name	
1	Motor Current	(2)	13	Torque Direct Voltage	
2	Output	(3)	14	Hall Element Voltage Input	(1)
3	Hall Element Ref. Voltage		15		(2)
4	Hall Element Voltage		16		(3)
5	Motor Current Detect		17		(4)
6	Disable		18	MM Output	
7	V_{CC}		19	PG Output	
8	Lock Detect		20	FG Output	
9	Phase Compensation		21	V_M	
10	Phase Compensation		22	NC	
11	Servo Ref. Voltage		23	Motor Current Output(1)	
12	GND		24	Motor Current	

■ Absolute Maximum Ratings (Ta = 25℃)

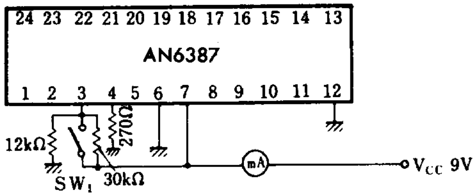
Item	Symbol	Rating		Unit	Note
Supply Voltage	V_{CC}	14.4		V	
Circuit Voltage	V_{n-12}	0	40	V	n = 1,2,23
Circuit Voltage	V_{21-12}	0	24	V	
Circuit Current	I_n	0	1500	mA	n = 1,2,23
Power Dissipation	P_D	10		W	
Operating Ambient Temperature	V_{opr}	−20 ~ +70		℃	
Storage Temperature	T_{stg}	−40 ~ +150		℃	

■ Electrical Characteristics (Ta = 25℃ ± 2℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Total Current	I_{tot}	1	$V_{CC}=9V$, disable	4.0		20	mA
ET-ATC Transfer Gain	$G_{(IO)}$	2	$V_{CC}=9V$	0.86		1.06	
ATC Limit Voltage	$V_{(lim)}$	2	$V_{CC}=9V$, at full-torque command	0.44		0.50	V
Saturation Detect Gain	$G_{(S)}$	3	$V_{CC}=9V$, $R_d=0.47\Omega$	0.5		1.5	
Saturation Detect Start Voltage	$V_{(Det\ 1)}$	3	$V_{CC}=9V$, $R_d=0.47\Omega$	1.0		1.8	V
Saturation Detect End Voltage	$V_{(Det\ 2)}$	3	$V_{CC}=9V$, $R_d=0.47\Omega$	0.5		1.0	V
HV Output Voltage	V_{HV}	1	$V_{CC}=9V$, $V_{SV}=2.6V$, $R_{HV}=270\Omega$	2.1			V
HV Protect Voltage	$V_{(Protect)}$	1	$V_{CC}=9V$, $V_{SV}=V_{CC}$	3.5		4.3	V
$\overline{DS}$ Level Voltage	$V_{\overline{DS}}$	2	$V_{CC}=9V$			1.2	V
ETR Voltage	V_{ETR}	2	$V_{CC}=9V$	4.3		4.7	V
HEM, $\overline{HEM}$, HES, $\overline{HES}$ Bias Current	I_{Bias}	2	$V_{CC}=9V$	−6			μA
HES-$\overline{HES}$ Comparator Offset Voltage	$V_{I(offset)S}$	2	$V_{CC}=9V$	−6		6	mV
HEM-$\overline{HEM}$ Comparator Offset Voltage	$V_{I(offset)M}$	2	$V_{CC}=9V$	−6		6	mV
PG Lowest Voltage	V_{OL19}	2	$V_{CC}=9V$, 47kΩ applied to Pin⑲→5V			0.5	V
FG Lowest Voltage	V_{OL29}	4	$V_{CC}=9V$, 47kΩ applied to Pin⑳→5V			0.5	V
BEF Fetch Voltage	V_{BFG}	4	$V_{CC}=V_M=9V$	0.6		1.0	V

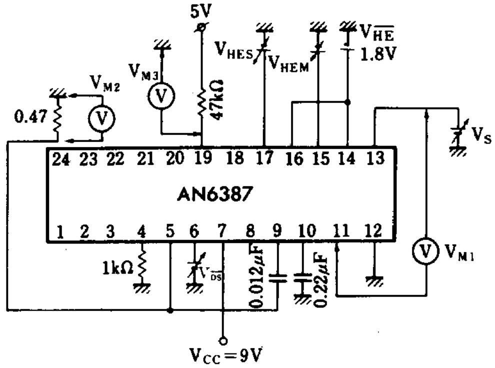
Note: Operating Supply Voltage Range : $V_{CC(opr)}=8\sim13V$ (V_{7-12})

Test Circuit 1 (I_{tot}, V_{HV}, $V_{(Protect)}$)



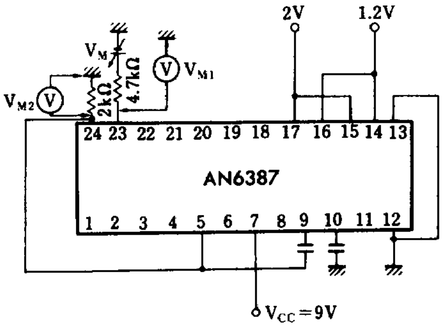
SW_1: Open, Current Value I_{CC}
SW_1: Open, Pin ③ Voltage 2.6V···
Pin④ Voltage V_{HV}
SW_1: Short, Pin ④ Voltage···$V_{(Protect)}$

Test Circuit 2 ($G_{(IO)}$, $V_{(lim)}$, $V_{\overline{DS}}$, V_{ETR}, I_{Bias}, $V_{I(offset)S}$, $V_{I(offset)M}$, V_{OL19})

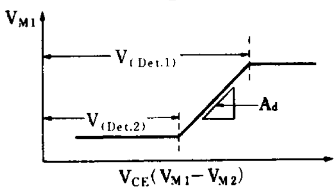


Read V_{M1} and V_{M2} when $V_{HES}=V_{HEM}=2V$, $V_{\overline{DS}}=2V$ and $V_S=0\sim6V$.
G_{IO}, $V_{(lim)}$
(V_{HES}, V_{HEM}, $V_{\overline{HF}}$ current···I_{Bias})
Read V_{M1} when $V_S=0V$. ···$-V_{ETR}$
$V_{HES}=V_{HEM}=2V$, $V_{DS}=2V$
Continuously lowering V_{HES} from 2V, the voltage of $V_{MES}-V_{\overline{HE}}$ when V_{M3} went down : $V_{I(offset)S}$
Next, continuously lowering V_{HEM} from 2V, the voltage of $V_{HEM}-V_{\overline{HE}}$ when V_{M3} went down : $V_{I(offset)M}$, and lowest voltage of V_{M3}···V_{OL19}

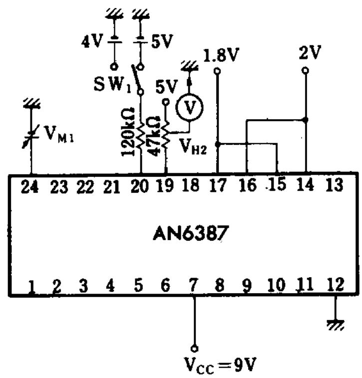
Test Circuit 3 ($G_{(S)}$, $V_{(Det.1)}$, $V_{(Det.2)}$)



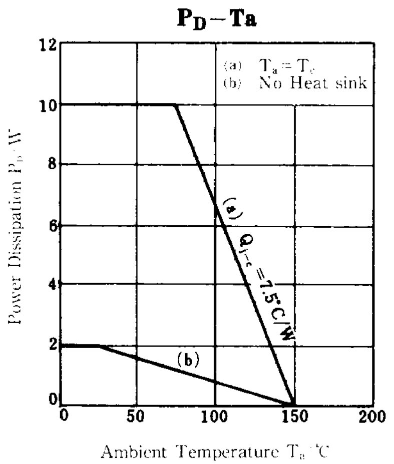
Set V_M at 2V. Continuously increase V_M until it is as shown in the figure below.



Test Circuit 4 (V_{OL20}, V_{BFG})



When $S_1=5V$ and $V_{M1}=9V$, V_{M2}···High voltage
When $S_1=4V$ and $V_{M1}=9V$, V_{M2}···Low voltage···V_{OL20}. At this time, continuously increase V_{M1} up to 10V.
Next, when V_{M1} continuously lowering for $S_1=5V$, the voltage of V_{M1} when V_{M2} became High voltage ···V_{BFG}



■ Application Circuit