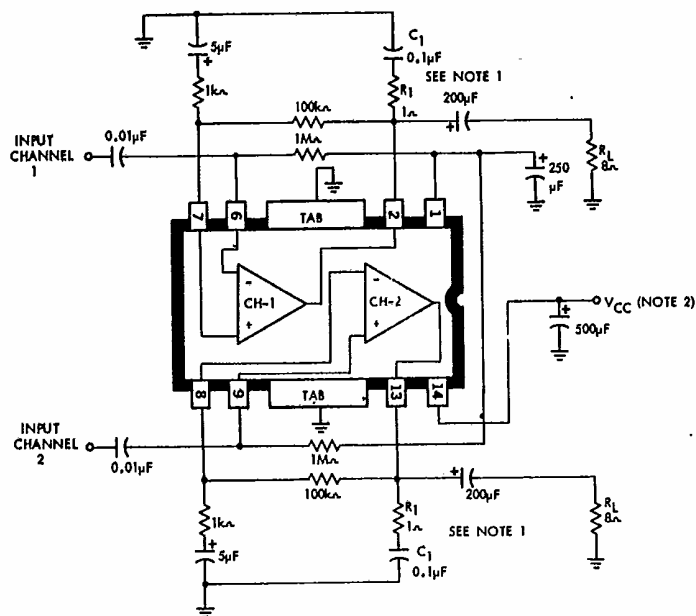
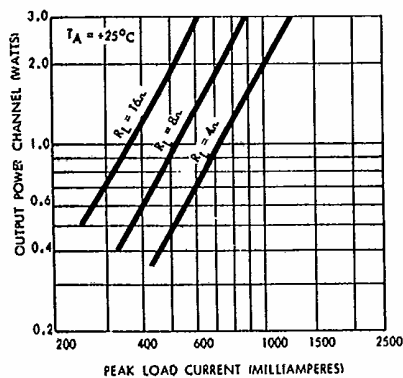


Figure 1
TEST CIRCUIT

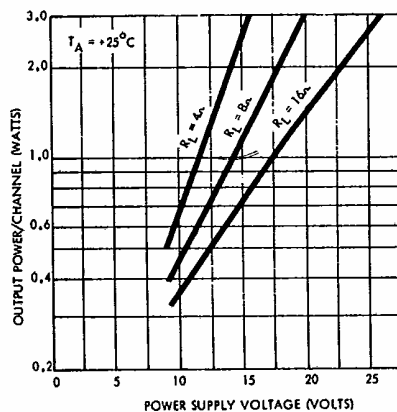


NOTES:

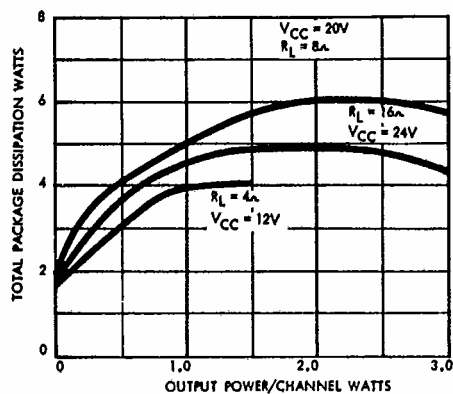
1. Compensation network: R_1 , C_1 values are dependent upon circuit layout.
2. When an unregulated supply voltage is used, the actual voltage present at pin 14 during full signal conditions should not drop below the nominal supply voltage level if full power output is to be maintained.
3. Closed loop gain should be limited to 30dB min. to 60dB max. to maintain stable circuit operation.



OUTPUT POWER/CHANNEL
AS A FUNCTION OF PEAK LOAD CURRENT

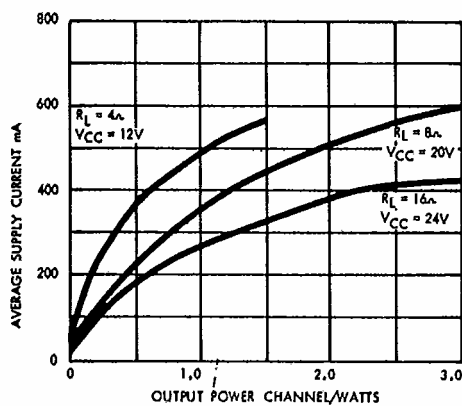


OUTPUT POWER/CHANNEL
AS A FUNCTION OF POWER SUPPLY VOLTAGE

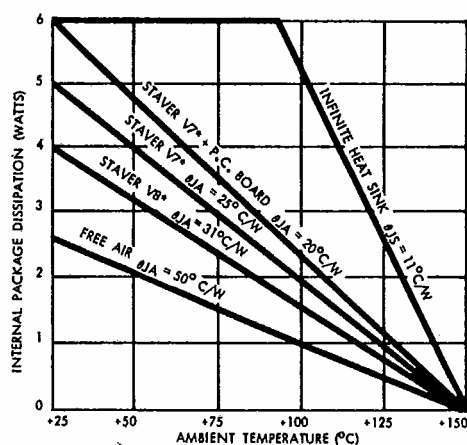


INTERNAL PACKAGE DISSIPATION AS A FUNCTION OF OUTPUT POWER/CHANNEL

Single channel operating only. If both channels are operating simultaneously, the total package dissipation will be the sum total of each individual channel.



SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER/CHANNEL



*V7-2, .015" Silver Bearing Copper Approx. 5 square inches of Surface Area

*V8-2, .015" Silver Bearing Copper with 60/40 Solder, Approx. 2 Square Area

P.C. BOARD IS $2\frac{1}{2}" \times 2\frac{1}{2}"$

PACKAGE HEAT DISSIPATION USING "STAYER" HEAT SINKS