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EM128C08 Family

128Kx8 Bit Ultra-Low Power Asynchronous Static RAM

Overview

The EM128C08 is an integrated memory device containing a low power 1 Mbit Static Random Access Memory organized as 131,072 words by 8 bits. The device is fabricated using NanoAmp's advanced CMOS process and high-speed/low-power circuit technology. This device is designed for very low voltage operation making it quite suitable for battery powered devices. It is also designed for both very low operating and standby-currents. The device pinout is compatible with other standard 128Kx8 SRAMs.

Features

- **Extremely Wide Operating Voltage**
  1.5 to 3.6 Volts
- **Extended Temperature Range**
  Standard: -20^{o} to +80^{o}C
- **Fast Cycle Time**
  Standard: < 70 ns @ 3 Volts
  -10: < 100 ns @ 3 Volts
- **Very Low Operating Current**
  I_{CC} < 1 mA maximum at 2V, 1 Mhz
- **Very Low Data Rentention Voltage**
  1.2 Volts Minimum
- **Very Low Standby Current**
  1 μA max. @ 55^{o}C
- **32-Pin TSOP, STSOP, SOP and 48-Pin BGA Packages Available**

FIGURE 1: Operating Envelope

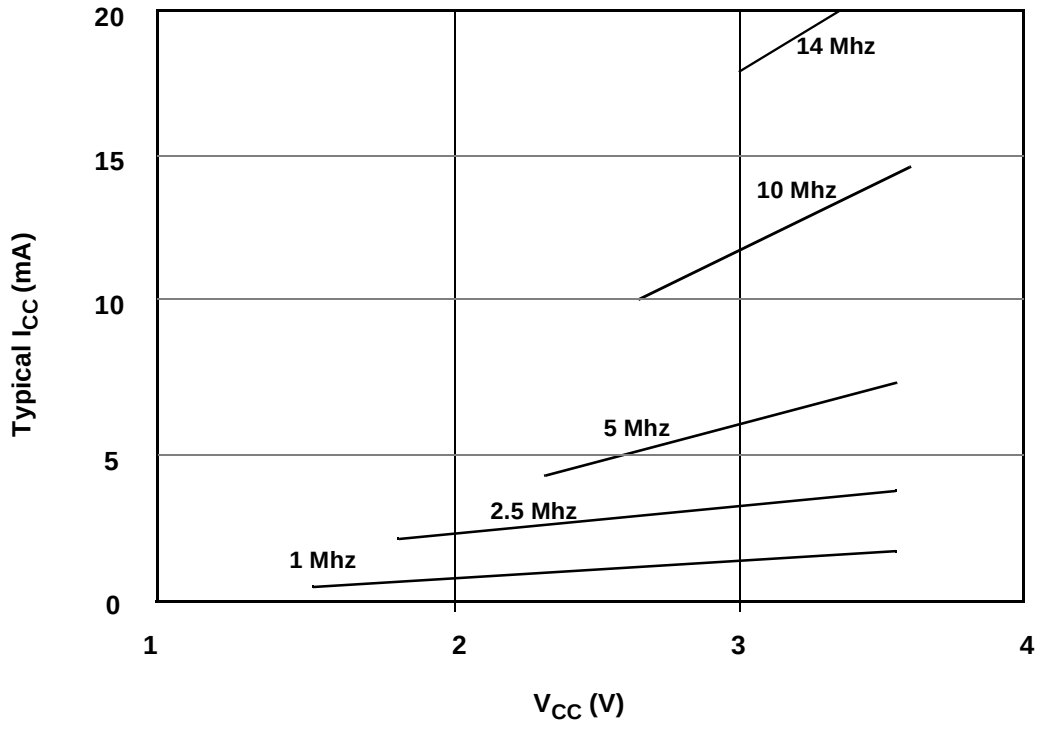
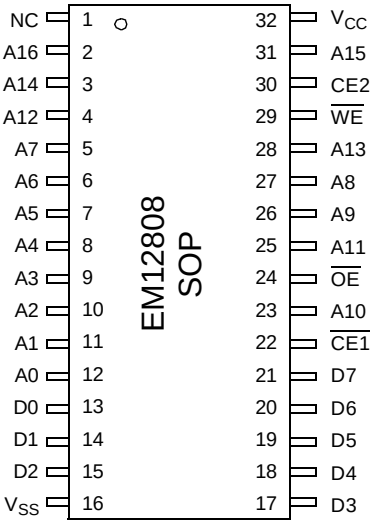


FIGURE 1: Pin Configurations



	1	2	3	4	5	6
A	A5	A7	A16	V_{CC}	$\overline{WE}$	A9
B	A4	A6	A14	A15	A13	A11
C	NC	A12	NC	NC	CE2	A8
D	NC	NC	NC	NC	NC	NC
E	NC	NC	NC	NC	NC	NC
F	A1	D1	NC	NC	D5	$\overline{CE1}$
G	A3	A0	D2	D4	D7	$\overline{OE}$
H	A2	D0	V_{SS}	D3	D6	A10

48 Pin BGA (top)
7mm x 9mm

FIGURE 2: Functional Block Diagram

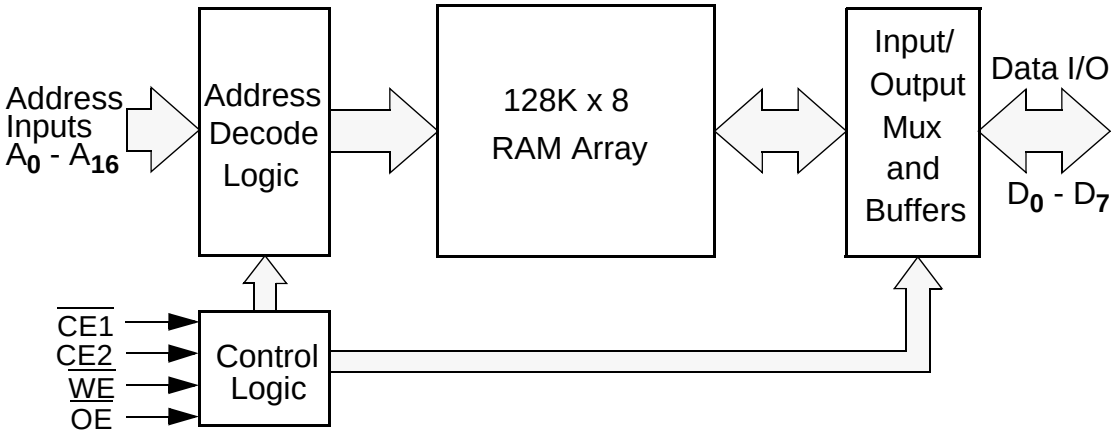


TABLE 1: Pin Description

Pin Name	Pin Function	Pin Name	Pin Function
A0-A16	Address Inputs	$\overline{WE}$	Write Enable (Active Low)
D0-D7	Data Inputs/Outputs	V_{CC}	Power
CE1	Chip Enable (Active Low)	V_{SS}	Ground
CE2	Chip Enable (Active High)	NC	Not Connected (Do not connect signal)
OE	Output Enable (Active Low)		

TABLE 2: Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	D0-D7	MODE	POWER
H	X	X	X	High Z	Standby	Standby
X	L	X	X	High Z	Standby	Standby
L	H	L	X	Data In	Write	Active -> Standby*
L	H	H	L	Data Out	Read	Active -> Standby*
L	H	H	H	High Z	Active	Standby*

*The device will consume active power in this mode whenever addresses are changed

TABLE 3: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to +125	^oC
Operating Temperature	T_A	-20 to +80	^oC

*Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 4: Operating Characteristics (Over the Specified Temperature Range)

Item	Symbol	Test Conditions	EM128C08		Unit
			Min.	Max.	
Operating Supply Voltage	V_{CC}		1.5	3.6	V
Data Retention Voltage	V_{DR}	$\overline{CE1}$ = V_{CC} or CE2 = 0	1.2		V
Input High Voltage	V_{IH}		0.7V_{CC}	V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3	0.3*V_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = -0.1mA	0.8*V_{CC}		V
Output Low Voltage	V_{OL}	I_{OL} = 0.1mA		0.2*V_{CC}	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ or $\overline{CE1}$ = V_{CC} or CE2 = 0		0.5	µA
Operating Supply Current (Note 1)	I_{CC}	V_{IN} = V_{CC} or 0V $\overline{CE1}$ = 0 and CE2 = V_{CC}		0.5*f*V	mA
Standby Current (Note 2), and Data Retention Current	I_{SB},I_{DR}	V_{IN}=V_{CC} or 0V, t_A=25 ^oC		0.2	µA
		V_{IN}=V_{CC} or 0V, t_A=55 ^oC		1	
		V_{IN}=V_{CC} or 0V, t_A=80 ^oC		10	

Note 1. Operating current is a linear function of operating frequency and voltage. You may calculate operating current using the formula shown with operating frequency (f) expressed in Mhz and operating voltage (V) in volts. Example: Operating at 2 Mhz at 3.0 volts will draw a maximum current of 0.5*2*3 = 3.0 mA.

Note 2. This device assumes a standby mode if either $\overline{CE1}$ is disabled (high) or CE2 is disabled (low). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) regardless of the state of CE1 or CE2. In order to achieve low standby current in the enabled mode (CE1 low and CE2 high), all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

TABLE 5: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 Mhz, T_A = 25^oC		5	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 Mhz, T_A = 25^oC		5	pF

Note: These parameters are verified in device characterization and are not 100% tested

TABLE 6: Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5V_{CC}$
Operating Temperature - Standard Version	-40 to +85 ^{O}C
Operating Temperature - Commercial Version	-20 to +80 ^{O}C
Output Load	CL = 50pF

TABLE 7: Timing - EM128C08 (Standard Version) Only

Item	Symbol	1.5 to 3.6 V		1.8 to 3.6 V		2.7 to 3.6 V		3.0 to 3.6 V		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	500		200		85		70		ns
Address Access Time	t_{AA}		500		200		85		70	ns
Chip Enable Access Time	t_{CE}		500		200		85		70	ns
Output Enable to Valid Output	t_{OE}		100		50		20		20	ns
Chip Enable to Low-Z output	t_{LZ}	0		0		0		0		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	100	0	50	0	20	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	100	0	50	0	20	0	20	ns
Output Hold from Address Change	t_{OH}	10		10		10		10		ns
Write Cycle Time	t_{WC}	500		200		85		70		ns
Chip Enable to End of Write	t_{CW}	500		200		85		70		ns
Address Valid to End of Write	t_{AW}	500		200		85		70		ns
Address Set-Up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	250		100		40		35		ns
Write Recovery Time	t_{WR}		0		0		0		0	ns
Write to High-Z Output	t_{WHZ}	0	50	0	40	0	20	0	20	ns
Data to Write Time Overlap	t_{DW}	200		80		40		30		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Low-Z Output	t_{OW}	10		10		10		10		ns

TABLE 8: Timing - EM128C08-10 Version

Item	Symbol	1.5 to 3.6 V		1.8 to 3.6 V		2.7 to 3.6 V		3.0 to 3.6 V		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	500		300		120		100		ns
Address Access Time	t_{AA}		500		300		120		100	ns
Chip Enable Access Time	t_{CE}		500		300		120		100	ns
Output Enable to Valid Output	t_{OE}		100		60		25		25	ns
Chip Enable to Low-Z output	t_{LZ}	0		0		0		0		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	100	0	60	0	25	0	25	ns
Output Disable to High-Z Output	t_{OHZ}	0	100	0	60	0	25	0	25	ns
Output Hold from Address Change	t_{OH}	10		10		10		10		ns
Write Cycle Time	t_{WC}	500		300		120		100		ns
Chip Enable to End of Write	t_{CW}	500		300		120		100		ns
Address Valid to End of Write	t_{AW}	500		300		120		100		ns
Address Set-Up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	300		100		50		40		ns
Write Recovery Time	t_{WR}		0		0		0		0	ns
Write to High-Z Output	t_{WHZ}	0	100	0	60	0	25	0	25	ns
Data to Write Time Overlap	t_{DW}	300		80		40		30		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Low-Z Output	t_{OW}	10		10		10		10		ns

FIGURE 3: Read Cycle Timing ($\overline{WE}$ = V_{IH})

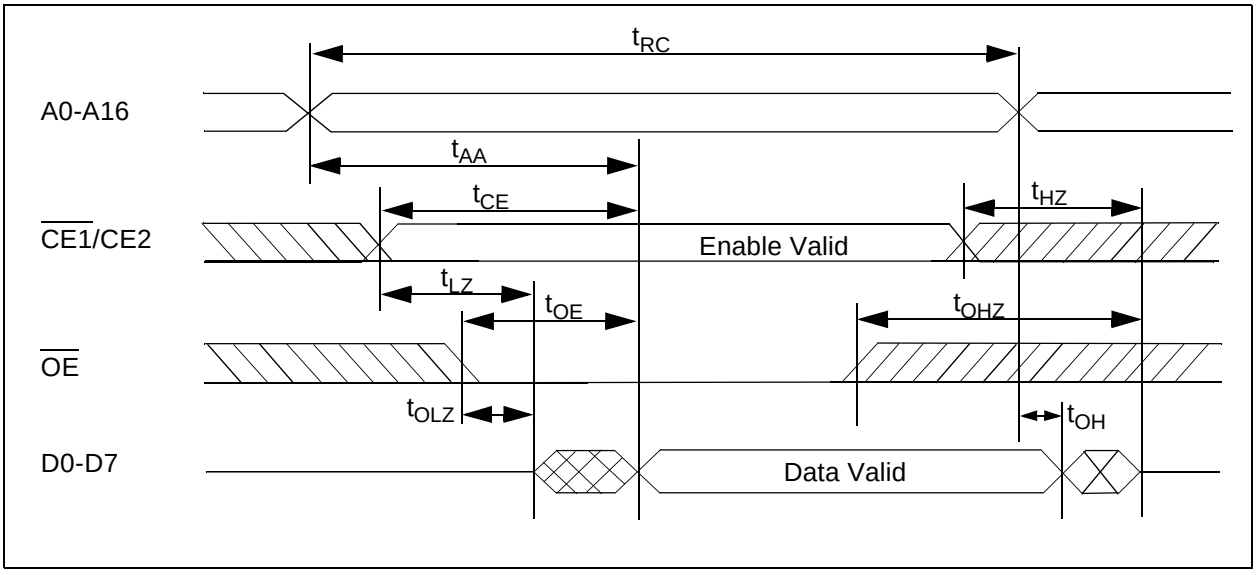


FIGURE 4: Write Cycle Timing ($\overline{OE}$ clock)

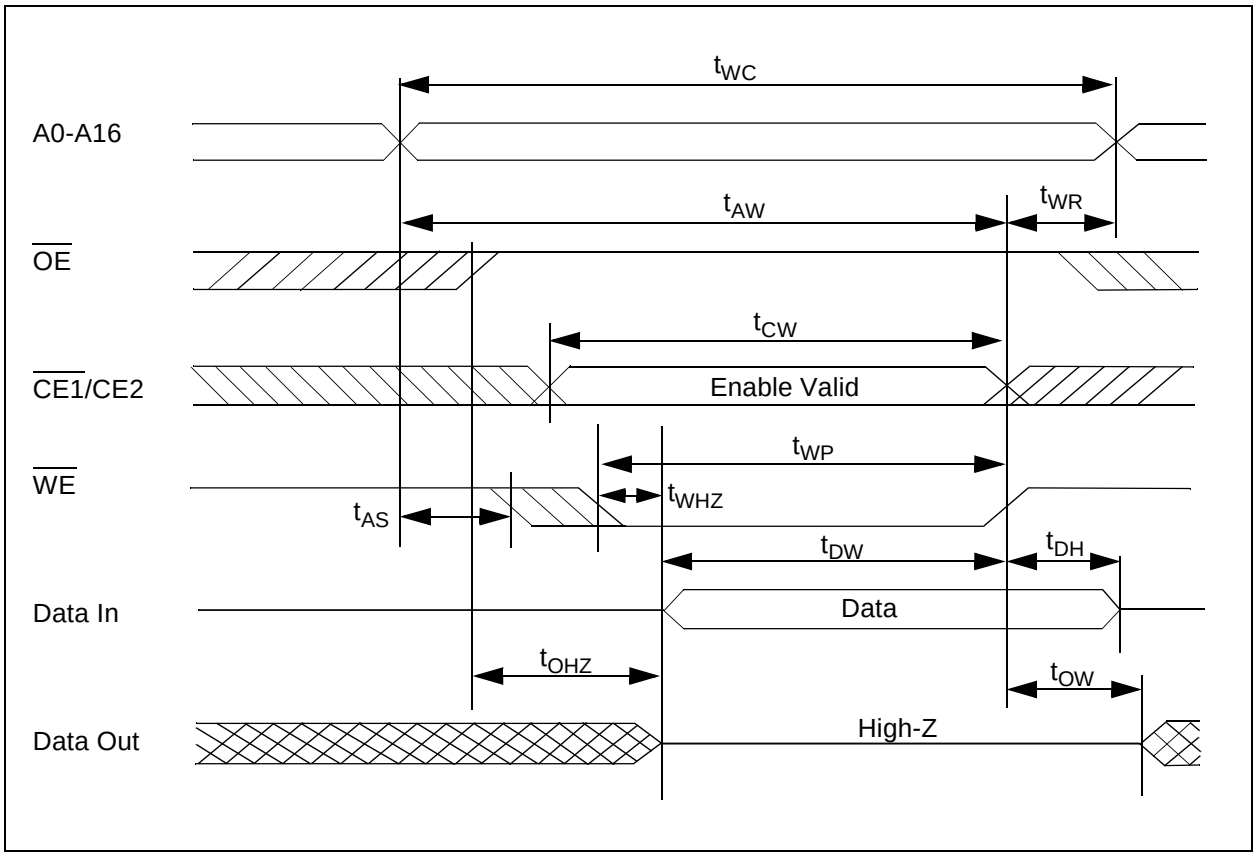


FIGURE 5: Write Cycle Timing ($\overline{OE}$ fixed)

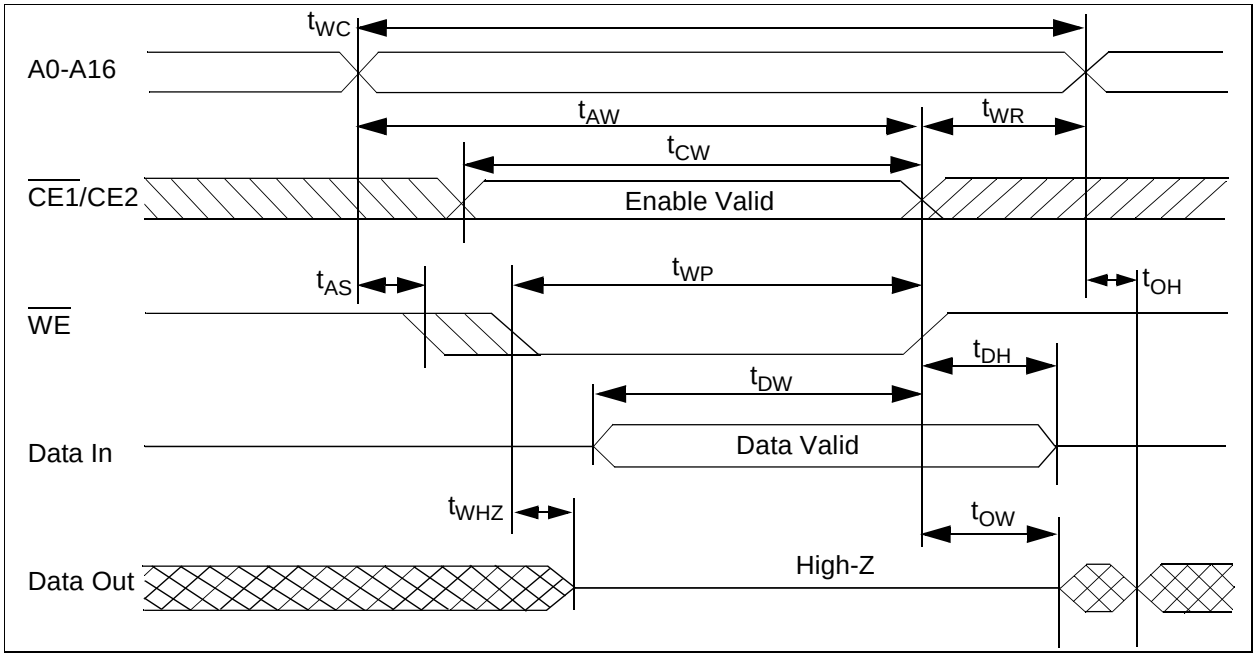


TABLE 9: Ordering Information

Part Number	Package	Temperature Range	Voltage Range	Speed (@ 3V+)
EM128C08S	32 pin SOP	-20 to +80 ^{o}C	1.5 to 3.6 V	70 ns
EM128C08T	32 pin TSOP	-20 to +80 ^{o}C	1.5 to 3.6 V	70 ns
EM128C08N	32 pin STSOP	-20 to +80 ^{o}C	1.5 to 3.6 V	70 ns
EM128C08B	48 pin BGA	-20 to +80 ^{o}C	1.5 to 3.6 V	70 ns
EM128C08S-10	32 pin SOP	-20 to +80 ^{o}C	1.5 to 3.6 V	100 ns
EM128C08T-10	32 pin TSOP	-20 to +80 ^{o}C	1.5 to 3.6 V	100 ns
EM128C08N-10	32 pin STSOP	-20 to +80 ^{o}C	1.5 to 3.6 V	100 ns
EM128C08B-10	48 pin BGA	-20 to +80 ^{o}C	1.5 to 3.6 V	100 ns

TABLE 10: Revision History

Revision #	Date	Change Description
01	Nov. 1, 1997	Initial Formal Release
02	Feb. 2, 1998	Corrected Miscellaneous Errata Modified Cycle Time and Related Parameters from 150 to 200 nS at 1.8 volts
03	Feb. 15, 1998	Added SOP option, Increased standby current
04	Apr. 1, 1998	Clarified CE2 Timing in Figures 3 to 5 Modified Operating Envelope Figure
05	Sep. 1, 1998	Reduced product versions to Standard and Commercial Added BGA option, Extended “standard” voltage range to 1.5 Volts min.
06	May 6, 1999	Standardized on voltage range of 1.5 to 3.6 volts Standardized on temperature range of -20 to 80 ^{o}C
07	June 3, 1999	Revised specifications to show -10 instead of “C” for 100 ns part