ERRATA DATA SHEET

1 MEG DRAM

(1 MEG PAGE MODE DRAM)

MICRON TECHNOLOGY, INC.
2805 East Columbia Road
Boise, Idaho 83706
TEL. (208) 386-3900
TWX 910-970-5973
Quality • Performance • Service

T-46-23-15

MT4C1024E — **1 MEG x 1 BIT DYNAMIC RAM**
MT4C4256E — **256K x 4 BIT DYNAMIC RAM**

FEATURES

- Industry standard ×1 or ×4 pin-out, functions and packages
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Low power, 5mw standby, 175 mw active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden
- Optional Page Mode access cycle

OPTIONS

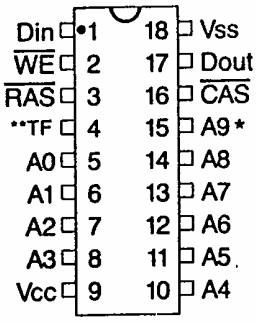
	MARKING
• Timing	×1,×4
100ns access	-10
120ns access	-12
150ns access	-15
• Organization	
1 MEG × 1	MT4C1024E
256K × 4	MT4C4256E
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

- Order Examples:
  1 MEG × 1, 120ns access, in Plastic DIP = MT4C1024E-12

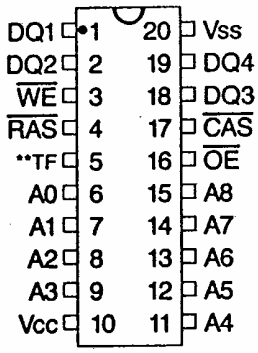
*Address not used for $\overline{RAS}$ only refresh
**TF = Test Function, ground or leave as a no-connect for normal device operation.

PIN ASSIGNMENT (TOP VIEW)

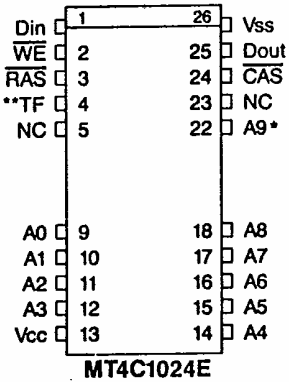
MT4C1024E
18 Pin DIP



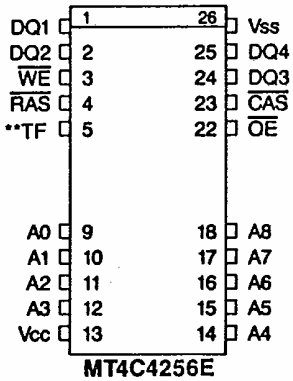
MT4C4256E
20 Pin DIP



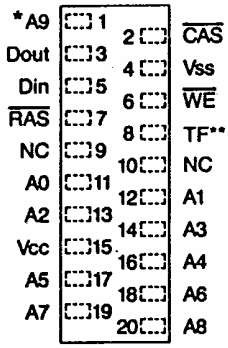
MT4C1024E
20 Pin SOJ



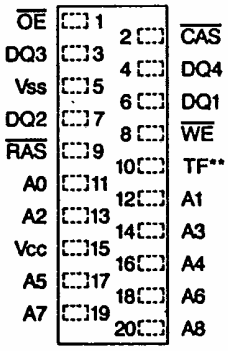
MT4C4256E
20 Pin SOJ



MT4C1024E
20 Pin ZIP



MT4C4256E
20 Pin ZIP



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacturer's products meeting JEDEC standards. Several parameters are sampled; however, functionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. The success of our memory business depends on the success of your application.

ERRATA DATA SHEET
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ TA ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	190		220		260		ns	
Read-Modify-Write cycle time	tRWC	220		255		295		ns	
Page mode cycle time	tPC	75		90		110		ns	
Access time from $\overline{RAS}$	tRAC		100		120		150	ns	
Access time from $\overline{CAS}$	tCAC		50		60		75	ns	
$\overline{RAS}$ pulse width	tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (Page Mode)	tRASP	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	tCPN	15		20		25		ns	
$\overline{CAS}$ precharge time (page mode)	tCP	15		20		25		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD	10	50	15	60	15	75	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	
Row address set-up time	tASR	5		5		5		ns	
Row address hold time	tRAH	10		15		15		ns	
Column address set-up time	tASC	5		5		5		ns	
Column address hold time	tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	tAR	60		70		80		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	
$\overline{CAS}$ to output in low-Z	tCLZ	5		5		5		ns	
Output buffer turn-off delay	tOFF	0	25	0	25	0	30	ns	
$\overline{WE}$ command set-up time	tWCS	0		0		0		ns	
Write command hold time	tWCH	20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	70		80		90		ns	
Write command pulse width	tWP	20		25		30		ns	
Write command to $\overline{RAS}$ lead time	tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	tCWL	25		30		35		ns	
Data-in set-up time	tDS	5		5		5		ns	
Data-in hold time	tDH	15		20		25		ns	
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	70		80		90		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	35		40		45		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	90		110		135		ns	
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	
Refresh Period (512 cycles)	tREF		8		8		8	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	20		25		30		ns	

MT4C4256E ONLY:

Output Enable	tOE		25		25		30	ns	
Output Disable	tOD		25		25		30	ns	