

IRLR/U3410

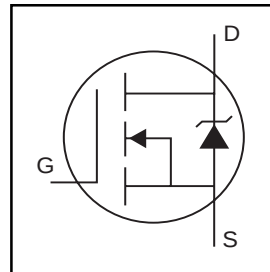
HEXFET® Power MOSFET

- Logic Level Gate Drive
- Ultra Low On-Resistance
- Surface Mount (IRLR3410)
- Straight Lead (IRLU3410)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

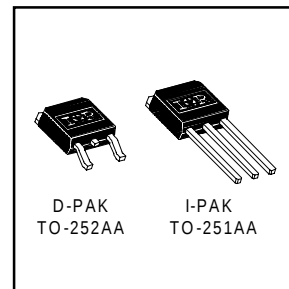
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



$V_{DS} = 100V$
 $R_{DS(on)} = 0.105\Omega$
 $I_D = 17A$



D-PAK
TO-252AA

I-PAK
TO-251AA

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	17	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	
I_{DM}	Pulsed Drain Current ①⑤	60	
$P_D @ T_C = 25^\circ C$	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②⑤	150	mJ
I_{AR}	Avalanche Current①⑤	9.0	A
E_{AR}	Repetitive Avalanche Energy①⑤	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.122	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.105	W	$V_{GS} = 10V, I_D = 10A$ ④
		—	—	0.125		$V_{GS} = 5.0V, I_D = 10A$ ④
		—	—	0.155		$V_{GS} = 4.0V, I_D = 9.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	7.7	—	—	S	$V_{DS} = 25V, I_D = 9.0A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	34	nC	$I_D = 9.0A$
Q_{gs}	Gate-to-Source Charge	—	—	4.8		$V_{DS} = 80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	20		$V_{GS} = 5.0V$, See Fig. 6 and 13 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	7.2	—	ns	$V_{DD} = 50V$
t_r	Rise Time	—	53	—		$I_D = 9.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G = 6.0\Omega, V_{GS} = 5.0V$
t_f	Fall Time	—	26	—		$R_D = 5.5\Omega$, See Fig. 10 ④ ⑤
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑥
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	800	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	160	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	90	—		$f = 1.0MHz$, See Fig. 5 ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ① ⑤	—	—	60		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 9.0A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	140	210	ns	$T_J = 25^\circ\text{C}, I_F = 9.0A$
Q_{rr}	Reverse Recovery Charge	—	740	1100	nC	$di/dt = 100A/\mu s$ ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 3.1mH$
 $R_G = 25\Omega$, $I_{AS} = 9.0A$. (See Figure 12)
 ③ $I_{SD} \leq 9.0A$, $di/dt \leq 540A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$
 ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$
 ⑤ Uses IRL530N data and test conditions
 ⑥ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
 For recommended footprint and soldering techniques refer to application note #AN-994

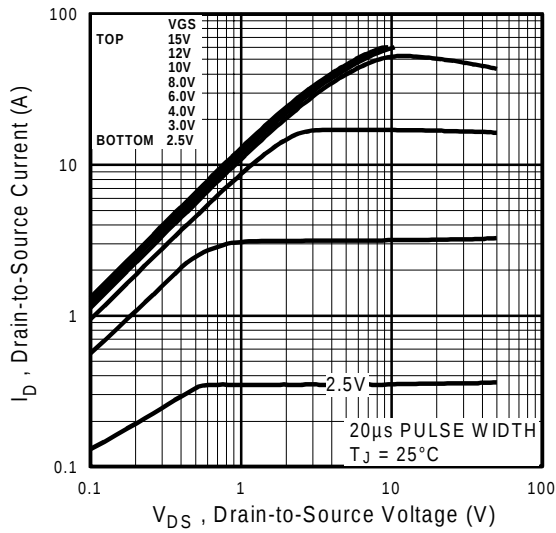


Fig 1. Typical Output Characteristics

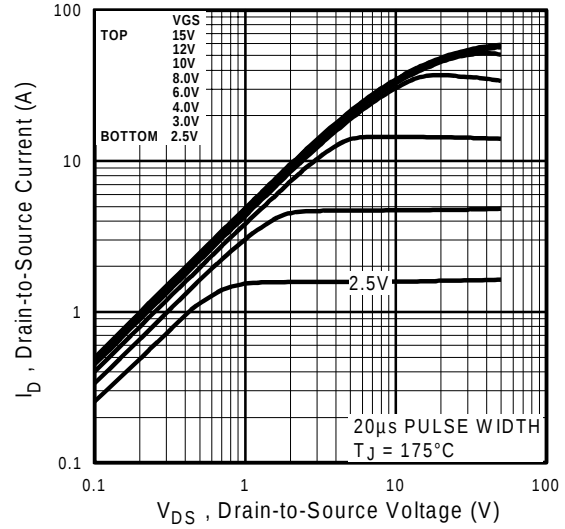


Fig 2. Typical Output Characteristics

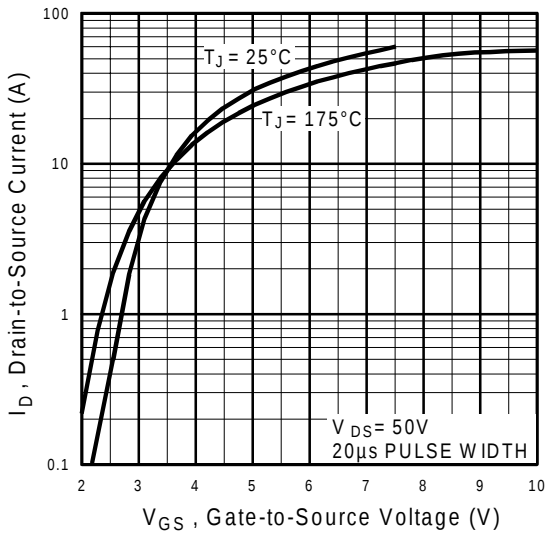


Fig 3. Typical Transfer Characteristics

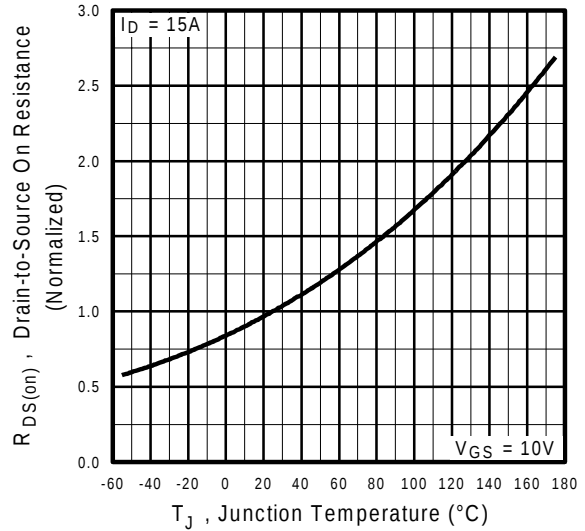


Fig 4. Normalized On-Resistance Vs. Temperature

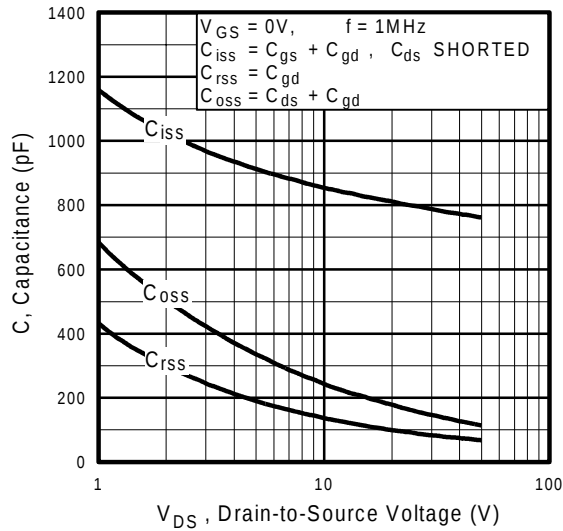


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

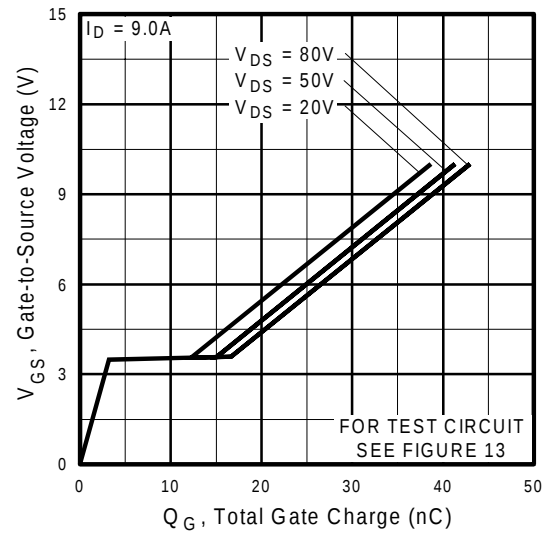


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

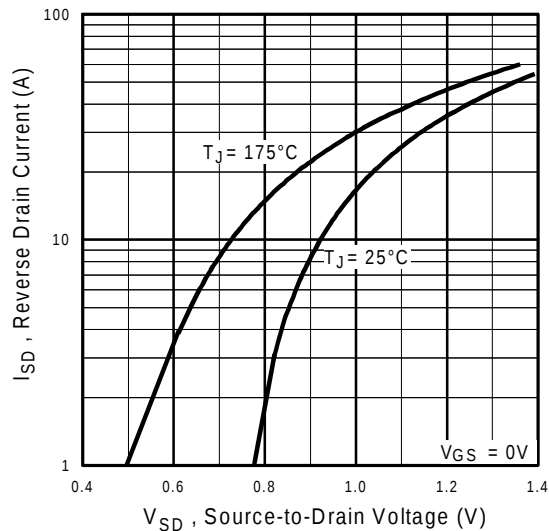


Fig 7. Typical Source-Drain Diode Forward Voltage

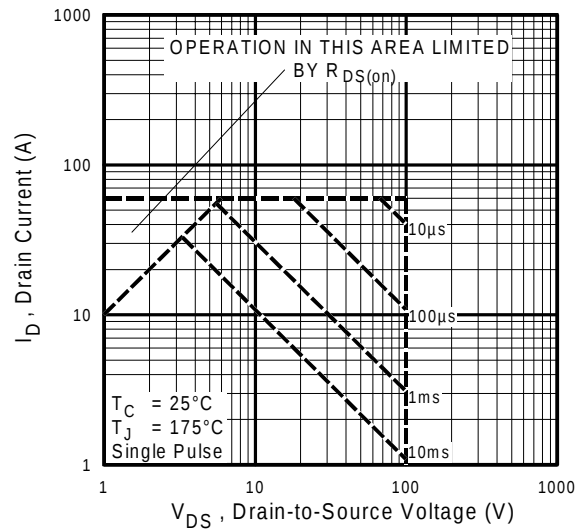


Fig 8. Maximum Safe Operating Area

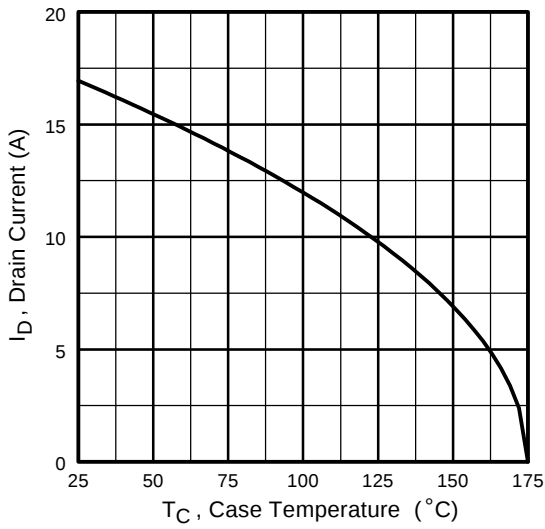


Fig 9. Maximum Drain Current Vs. Case Temperature

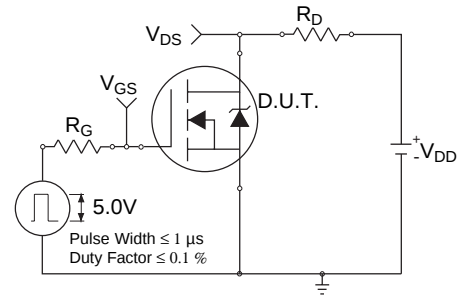


Fig 10a. Switching Time Test Circuit

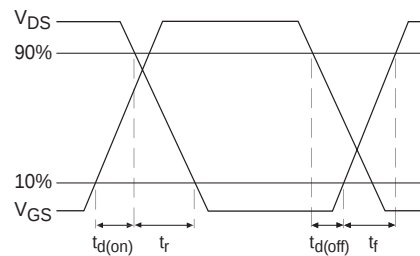


Fig 10b. Switching Time Waveforms

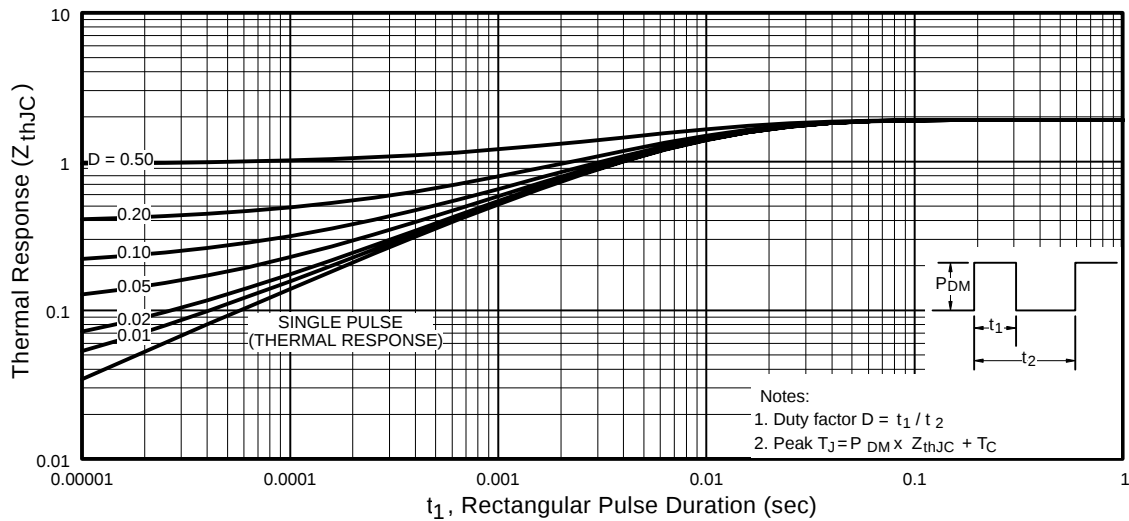


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

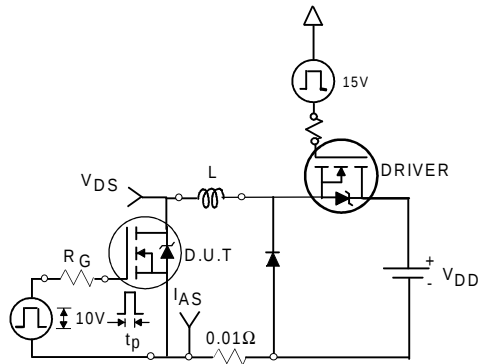


Fig 12a. Unclamped Inductive Test Circuit

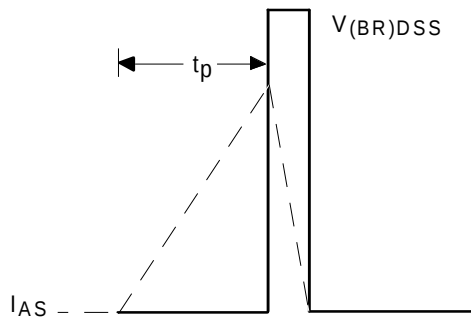


Fig 12b. Unclamped Inductive Waveforms

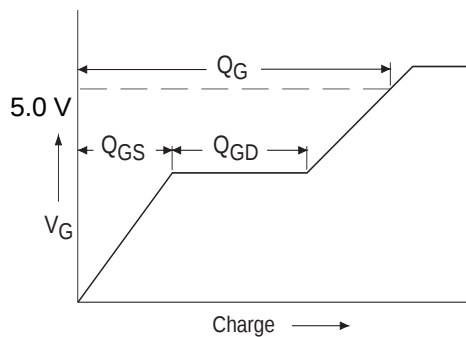


Fig 13a. Basic Gate Charge Waveform

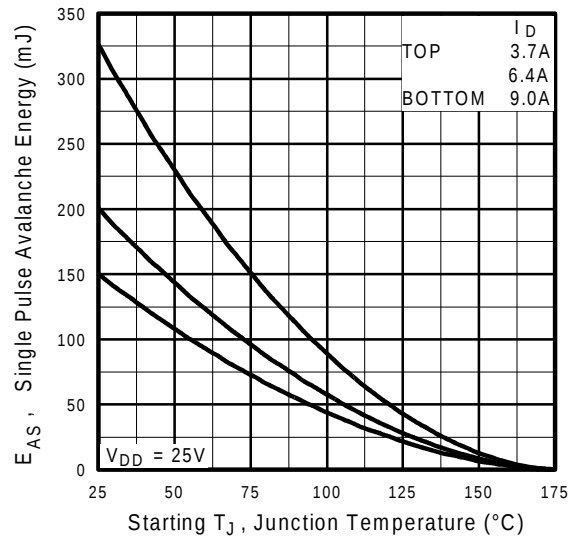
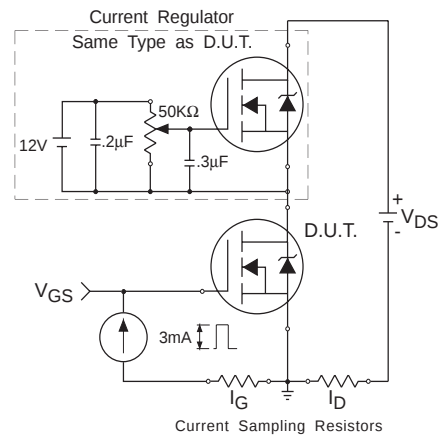
Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

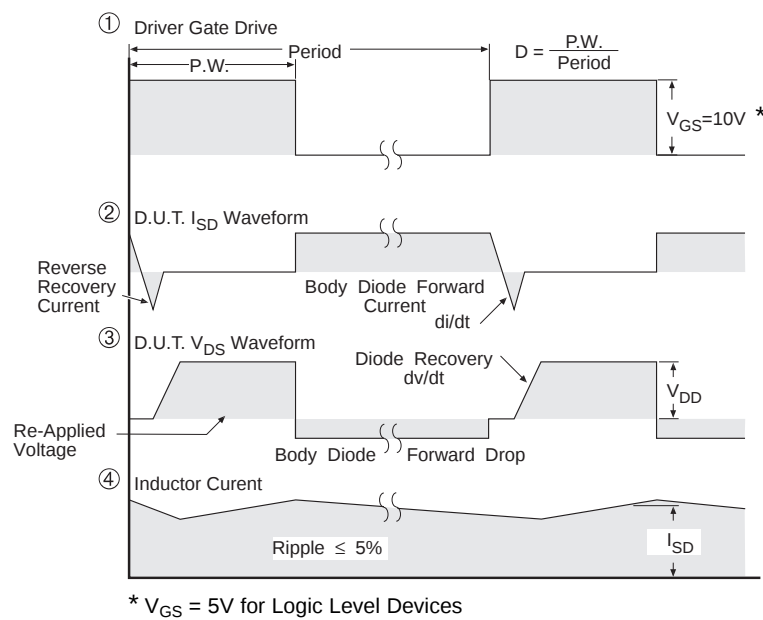
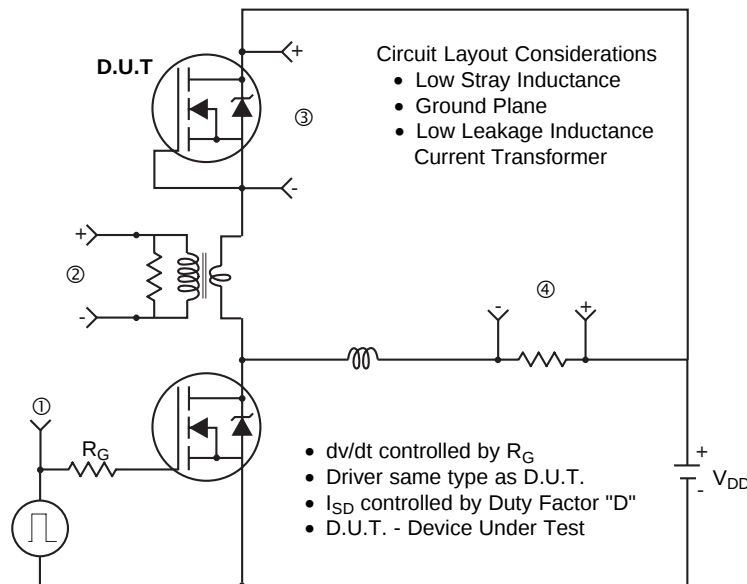
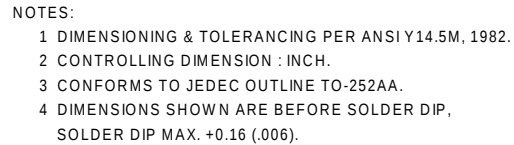


Fig 14. For N-Channel HEXFETS

Dimensions are shown in millimeters (inches)



TO-252AA (D-PARK)

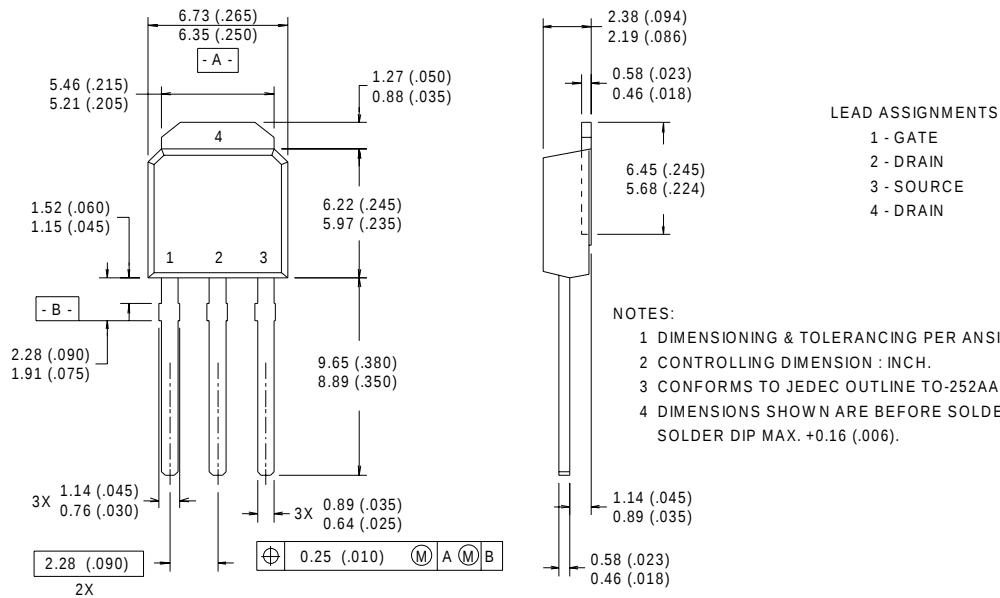
Diagram illustrating the markings on a MOSFET package (IRFR120) and their corresponding labels:

- INTERNATIONAL RECTIFIER LOGO**: Points to the "IR" logo on the package.
- FIRST PORTION OF PART NUMBER**: Points to the "120" marking on the package.
- ASSEMBLY LOT CODE**: Points to the "9U" marking on the package.
- SECOND PORTION OF PART NUMBER**: Points to the "1P" marking on the package.

Package Outline

TO-251AA Outline

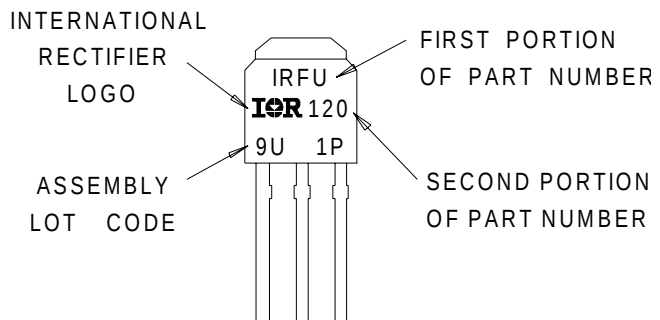
Dimensions are shown in millimeters (inches)



Part Marking Information

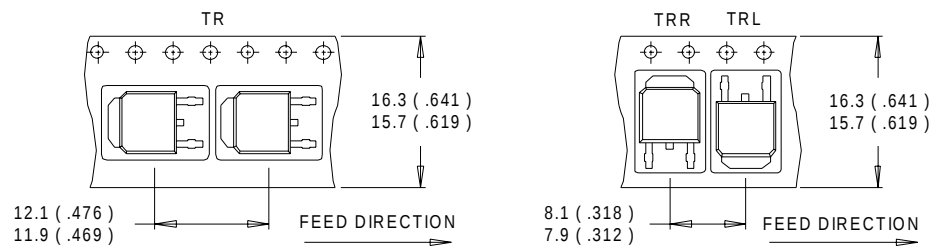
TO-251AA (I-PARK)

EXAMPLE : THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 9U1P



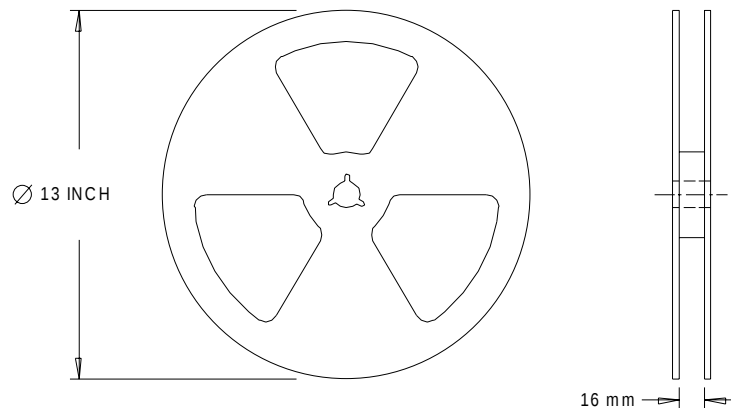
Tape & Reel Information

TO-252AA



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

International
IR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T 3Z2, Tel: (905) 453 2200

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: 171 (K&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81 33 983 0086

IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 16907 Tel: 65 221 8371

Data and specifications subject to change without notice.

5/98