Data Sheet PD No. 60179-I

International
IOR Rectifier

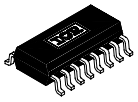
IR21571(S)

FULLY INTEGRATED BALLAST CONTROL IC

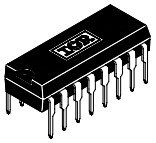
Features

- Programmable preheat time & frequency
- Programmable ignition ramp
- Protection from failure-to-strike
- Lamp filament sensing & protection
- Protection from operation below resonance - 0.2V CS threshold sync' d to falling edge on LO
- Protection from low-line condition
- Automatic restart for lamp exchange
- Thermal overload protection
- Programmable deadtime
- Integrated 600V level-shifting gate driver
- Internal 15.6V zener clamp diode on VCC
- Micropower startup (150uA)
- Latch immunity protection on all leads
- ESD protection on all leads

Packages



16 Lead SOIC
(narrow body)

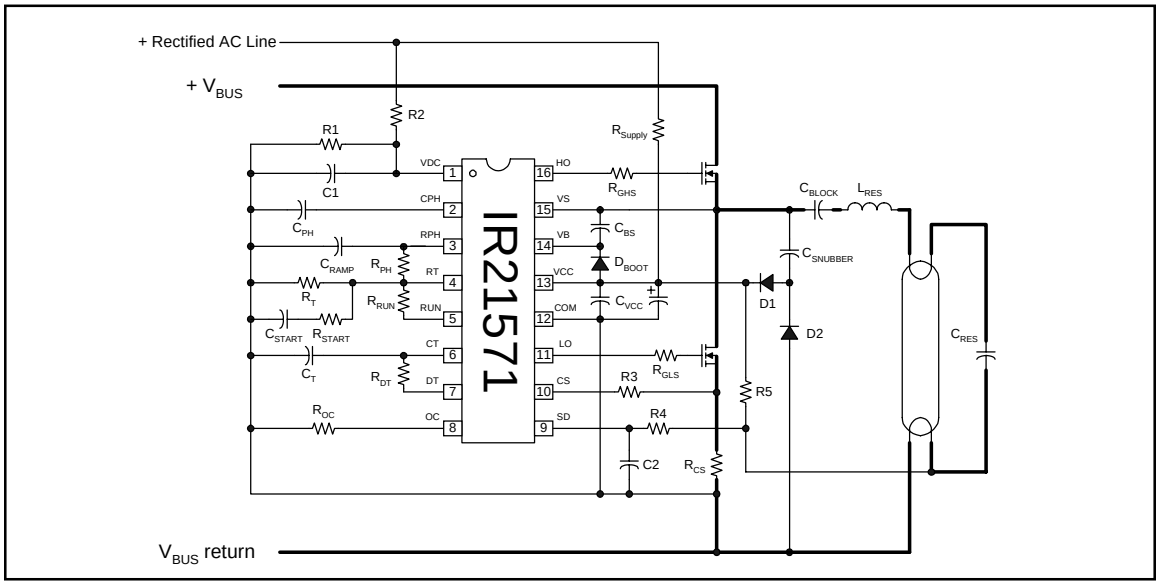


16 Lead PDIP

Description

The IR21571 is a fully integrated, fully protected 600V ballast control IC designed to drive virtually all types of rapid start fluorescent lamp ballasts. Externally programmable features such as preheat time & frequency, ignition ramp characteristics, and running mode operating frequency provide a high degree of flexibility for the ballast design engineer. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, low dc bus conditions, thermal overload, or lamp failure during normal operation, as well as an automatic restart function, have been included in the design. The heart of this control IC is a variable frequency oscillator with externally programmable deadtime. Precise control of a 50% duty cycle is accomplished using a T-flip-flop. The IR21571 is available in both 16 pin DIP and 16 pin narrow body SOIC packages.

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
I_{OMAX}	Maximum allowable output current (either output) due to external power transistor miller effect		-500	500	mA
I_{RT}	R_T pin current		-5	5	
V_{CT}	C_T pin voltage		-0.3	5.5	V
V_{DC}	V_{DC} pin voltage		-0.3	V_{CC} + 0.3	
I_{CPH}	CPH pin current		-5	5	mA
I_{RPH}	RPH pin current		-5	5	
I_{RUN}	RUN pin current		-5	5	
I_{DT}	Deadtime pin current		-5	5	
V_{CS}	Current sense pin voltage		-0.3	5.5	V
I_{CS}	Current sense pin current		-5	5	mA
I_{OC}	Over-current threshold pin current		-5	5	
I_{SD}	Shutdown pin current		-5	5	
I_{CC}	Supply current (note 1)		-20	20	
dV/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(16 lead PDIP)	—	1.60	W
	$P_D = (T_{JMAX}-T_A)/Rth_{JA}$	(16 lead SOIC)	—	1.00	
Rth_{JA}	Thermal resistance, junction to ambient	(16 lead PDIP)	—	75	°C/W
		(16 lead SOIC)	—	115	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	-3.0	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	Note 2	10	mA
V_{DC}	V_{DC} lead voltage	0	VCC	V
C_T	C_T lead capacitance	220	—	pF
R_{DT}	Deadtime resistance	1.0	—	kΩ
R_{OC}	Over-current (CS+) threshold programming resistance	—	50	
I_{RT}	R_T lead current (Note 3)	-500	-50	uA
I_{RPH}	RPH lead current (Note 3)	0	450	
I_{RUN}	RUN lead current (Note 3)	0	450	
I_{SD}	Shutdown lead current	-1	1	mA
I_{CS}	Current sense lead current	-1	1	
T_J	Junction temperature	-40	125	°C
VBSMIN	Minimum required VBS voltage for proper HO functionality	—	5	V

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 40.0kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 0.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.5	11.4	12.4	V	V_{CC} rising from 0V
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	1.5	1.8	2.2		
I_{QCCUV}	UVLO mode quiescent current	50	150	300	µA	V_{CC} < V_{CCUV-}
I_{QCCFLT}	Fault-mode quiescent current	75	200	300		SD=5V, CS = 2V or Tj > T_{SD}
I_{QCC}	Quiescent V_{CC} supply current	2.9	3.8	4.3	mA	R_T no connection, C_T connected to COM
I_{CC50K}	V_{CC} supply current, f= 50kHz	4.0	5.5	7.0		R_T =36kΩ, R_{DT} = 5.6kΩ, C_T=220pF
V_{CLAMP}	V_{CC} zener clamp voltage	14.5	15.6	16.5	V	I_{CC} = 10mA

Note 2: Enough current should be supplied into the VCC lead to keep the internal 15.6V zener clamp diode on this lead regulating its voltage.

Note 3: Due to the fact that the RT input is a voltage-controlled current source, the total RT lead current is the sum of all the parallel current sources connected to that lead. For optimum oscillator current mirror performance, this total current should be kept between 50µA and 500µA. During the preheat mode, the total current flowing out of the RT lead consists of the RPH lead current plus the current due to the RT resistor. During the run mode, the total RT lead current consists of the RUN lead current plus the current due to the RT resistor.

Electrical Characteristics (cont.)

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 40.0kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 0.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

Floating Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{QBS0}	Quiescent V_{BS} supply current	0	0	15	µA	V_{HO} = V_S
I_{QBS1}	Quiescent V_{BS} supply current	5	35	65		V_{HO} = V_B
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V

Oscillator I/O Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
fosc	Oscillator frequency	45.5	48	50.5	kHz	R_T = 16.9kΩ, R_{DT} = 6.1kΩ, C_T=470pF
d	Oscillator duty cycle	49.5	50	50.5	%	
V_{CT+}	Upper C_T ramp voltage threshold	3.7	4.0	4.3	V	
V_{CT-}	Lower C_T ramp voltage threshold	1.85	2.0	2.15		
V_{CTFLT}	Fault-mode C_T lead voltage	—	0	50	mV	SD = 5V, CS = 2V, or Tj > TSD
V_{RT}	R_T lead voltage	1.85	2.0	2.15	V	
V_{RTFLT}	Fault-mode R_T lead voltage	—	0	50	mV	SD = 5V, CS = 2V, or Tj > TSD
tdlo	LO output deadtime	2	2.3	2.5	µsec	
tdho	HO output deadtime	2	2.3	2.5		

Preheat Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{CPH}	CPH lead charging current	0.72	0.85	0.98	µA	V_{CPH} = 5.3V
V_{CPHIGN}	CPH lead Ignition mode threshold voltage	3.7	4.0	4.3	V	
V_{CPHRUN}	CPH lead run mode threshold voltage	4.7	5.15	5.45		
$V_{CPHCLMP}$	CPH lead clamp voltage	9.0	9.5	10.5		I_{CPH} = 1mA
V_{CPHFLT}	Fault-mode CPH lead voltage	—	0	300	mV	SD = 5V, CS = 2V, or Tj > TSD

RPH Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RPHLK}	Open circuit RPH lead leakage current	—	0.01	0.1	µA	V_{RPH}= 5V,V_{RPH}= 6V
V_{RPHFLT}	Fault-mode RPH lead voltage	—	0	50	mV	SD = 5V, CS = 2V, or Tj > TSD

Electrical Characteristics (cont.)

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 40.0kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 0.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

RUN Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RUNLK}	Open circuit RUN lead leakage current	—	0.01	0.1	µA	V_{RUN} = 5V
V_{RUNFLT}	Fault-mode RUN lead voltage	—	0	50	mV	SD = 5V, CS = 2V, or Tj > TSD

Protection Circuitry Characteristics

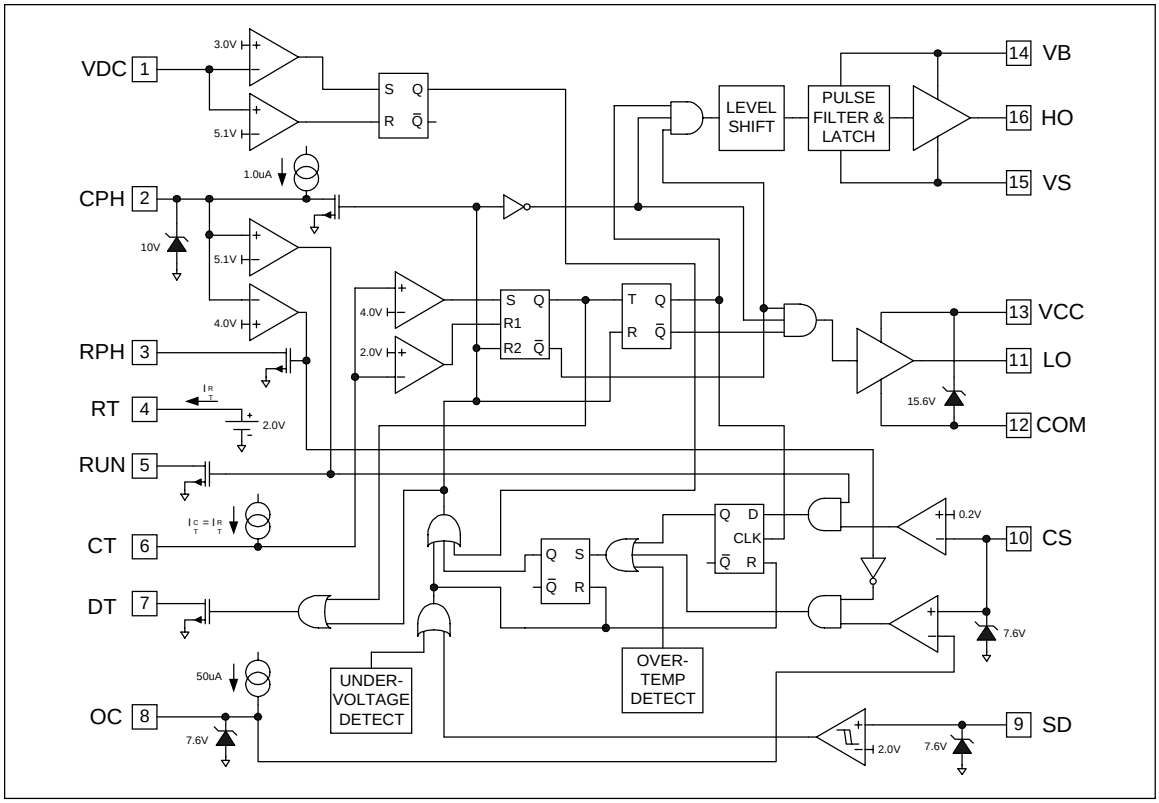
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{SD+}	Rising shutdown lead threshold voltage	1.9	2.1	2.3	V	
V_{SDHYS}	Shutdown pin threshold hysteresis	100	150	200	mV	
V_{CS+}	Over-current sense threshold voltage	0.99	1.10	1.21	V	
V_{CS-}	Under-current sense threshold voltage	0.15	0.2	0.35		
T_{CS}	Over-current sense propogation delay	100	250	400	nsec	Delay from CS to LO
V_{DC+}	Low V_{BUS}/rectified line input upper threshold	5.0	5.20	5.6	V	
V_{DC-}	Low V_{BUS}/rectified line input lower threshold	2.85	3.3	3.3		
T_{SD}	Thermal shutdown junction temperature	150	160	170	°C	Note 4

Gate Driver Output Characteristics

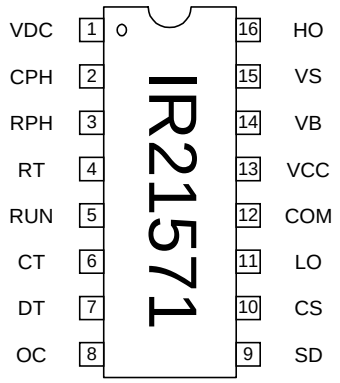
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
VOL	Low-level output voltage	—	0	100	mV	I_O = 0
V_{OH}	High level output voltage	—	0	100		V_{BIAS} - V_O, I_O = 0
t_r	Turn-on rise time	55	85	150	nsec	
t_f	Turn-off fall time	35	45	100		

Note 4: When the IC senses an overtemperature condition (Tj > 160ºC), the IC is latched off. In order to reset this Fault Latch, the SD lead must be cycled high and then low, or the V_{CC} supply to the IC must be cycled below the falling undervoltage lockout threshold (V_{CCUV-}).

Functional Block Diagram

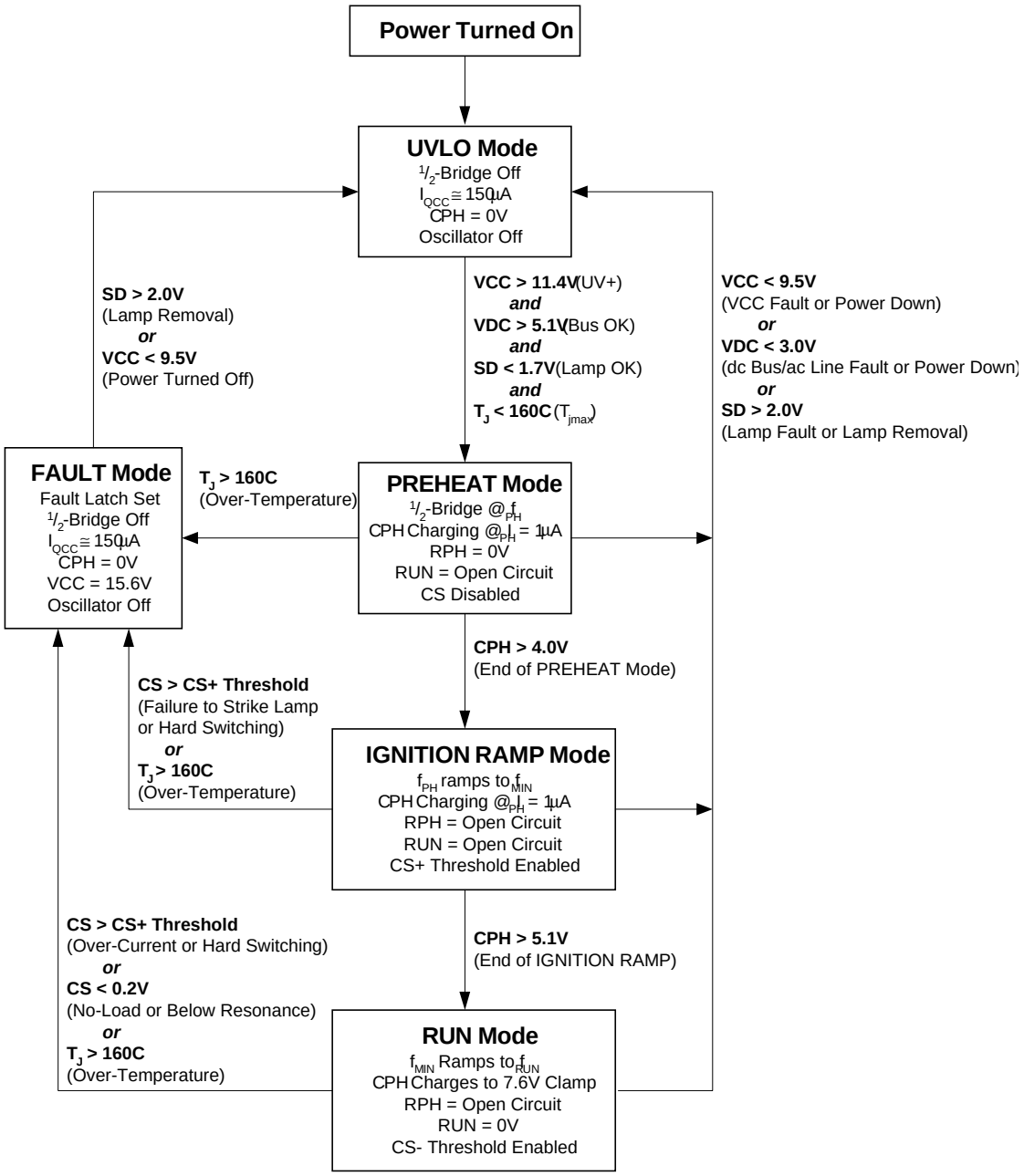


Lead Assignments & Definitions



Pin #	Symbol	Description
1	VDC	DC Bus Sensing Input
2	CPH	Preheat Timing Capacitor
3	RPH	Preheat Frequency Resistor & Ignition Capacitor
4	RT	Oscillator Timing Resistor
5	RUN	Run Frequency Resistor
6	CT	Oscillator Timing Capacitor
7	DT	Deadtime Programming
8	OC	Over-current (CS+) Threshold Programming
9	SD	Shutdown Input
10	CS	Current Sensing Input
11	LO	Low-Side Gate Driver Output
12	COM	IC Power & Signal Ground
13	VCC	Logic & Low-Side Gate Driver Supply
14	VB	High-Side Gate Driver Floating Supply
15	VS	High Voltage Floating Return
16	HO	High-Side Gate Driver Output

IR21571 State Diagram



Description of Operation & Component Selection Tips

Supply Bypassing and PC Board Layout Rules

Component selection and placement on the pc board is extremely important when using power control ICs. VCC should be bypassed to COM as close to the IC terminals as possible with a low ESR/ESL capacitor, as shown in Figure 1 below.

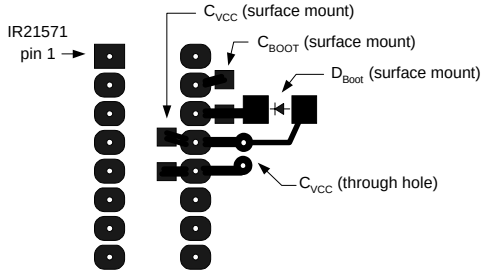


Figure 1: Supply bypassing PCB layout example

A rule of thumb for the value of this bypass capacitor is to keep its minimum value at least 2500 times the value of the total input capacitance (Ciss) of the power transistors being driven. This decoupling capacitor can be split between a higher valued electrolytic type and a lower valued ceramic type connected in parallel, although a good quality electrolytic (e.g., 10µF) placed immediately adjacent to the VCC and COM terminals will work well.

In a typical application circuit, the supply voltage to the IC is normally derived by means of a high value startup resistor (1/4W) from the rectified line voltage, in combination with a charge pump from the output of the half-bridge. With this type of supply arrangement, the internal 15.6V zener clamp diode from VCC to COM will determine the steady state IC supply voltage.

Connecting the IC Ground (COM) to the Power Ground

Both the low power control circuitry and low side gate driver output stage grounds return to this lead within the IC. The COM lead should be connected to the bottom terminal of the current sense resistor in the source of the low side power MOSFET using an individual pc board trace, as shown in Figure 2. In addition, the ground return path of the timing components and VCC decoupling capacitor should be connected directly to the IC COM lead, and not via separate traces or jumpers to other ground traces on the board.

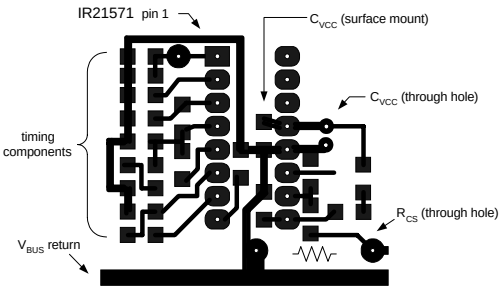


Figure 2: COM lead connection PCB layout example

This connection technique prevents high current ground loops from interfering with the sensitive timing component operation, and allows the entire control circuit to reject common-mode noise due to output switching.

The Control Sequence & Timing Component Selection

The IR21571 uses the following control sequence (Figure 3) to drive rapid start fluorescent lamps.

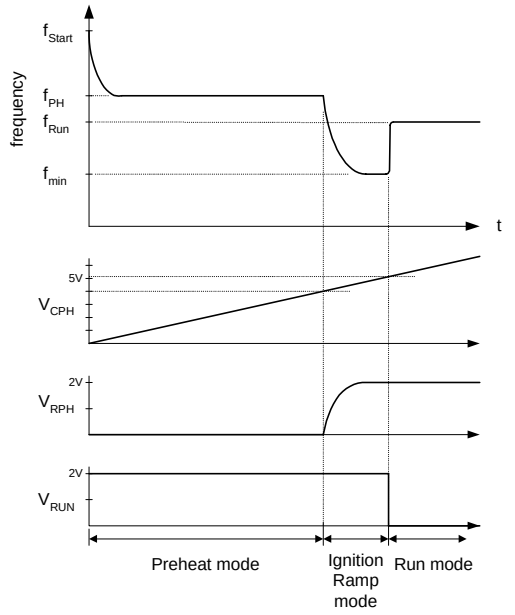


Figure 3: IR21571 control sequence

The control sequence used in the IR21571 allows the Run Mode operating frequency of the ballast to be higher than the ignition frequency (i.e., fstart > fph > frun > fign). This control sequence is recommended for lamp types where the ignition frequency is too close to the run frequency to ensure proper lamp striking for all production resonant LC component tolerances (please note that it is possible to use the IR21571 in systems where fstart > fph > fign > frun, simply by leaving the RUN lead open).

Six leads in the IC are used to control the **Startup, Preheat, Ignition Ramp,** and **Run** modes of operation, and to allow ballast and lamp engineers the flexibility to optimize their designs for virtually any lamp type.

The heart of this controller is an oscillator which resembles those found in many popular PWM voltage regulator ICs. In its simplest form, this oscillator consists of a timing resistor and capacitor connected to ground. The voltage across the timing capacitor CT is a sawtooth, where the rising portion of the ramp is determined by the current in the R_T lead, and the falling portion of the ramp is determined by an external deadtime resistor R_{DT}. The oscillograph in Figure 4 illustrates the relationship between the oscillator capacitor waveform and the gate driver outputs.

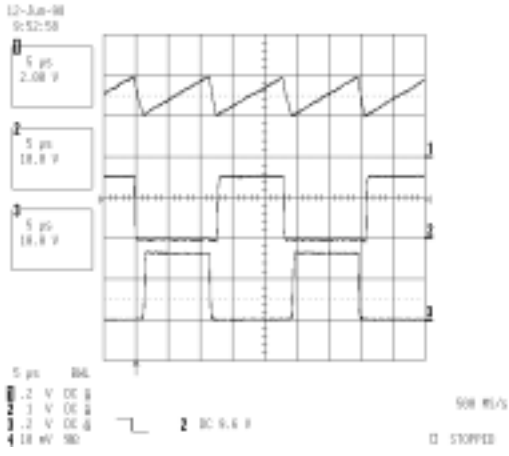


Figure 4

The deadtime can be programmed by means of the external R_{DT} resistor, given a certain range of CT capacitor values, using the graph shown in Figure 5.

The R_T input is a voltage-controlled current source, where the voltage is regulated to be approximately 2.0V. In order to maintain proper linearity between the R_T lead current and the C_T capacitor charging current, the value of the R_T lead current should be kept between 50µA and 500µA. The R_T lead can also be used as a feedback point for closed loop control.

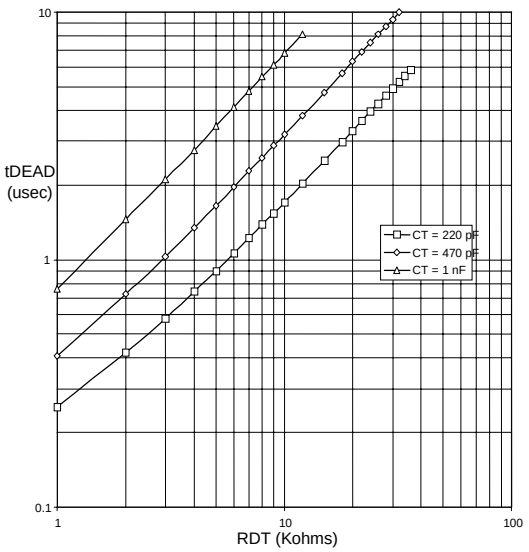


Figure 5: Deadtime versus R_{DT}

During the **Startup Mode**, the operating frequency is determined by the parallel combination of R_{PH}, R_{START}, and R_T, combined with the values of C_{START}, C_T and R_{DT} , as shown in Figure 6. This frequency is normally chosen to ensure that the instantaneous voltage across the lamp during the first few cycles of operation does not exceed the strike potential of the lamp. As the voltage across C_{START} charges up to the R_T lead voltage, the output frequency exponentially decays to the preheat frequency.

During the Preheat Mode, the operating frequency is determined by the parallel combination of R_{PH} and R_T, combined with the value of C_T and R_{DT}. This frequency, along with the Preheat Time, is normally chosen to ensure that adequate heating of the lamp filaments occur. Typically, a 4.5:1 ratio of the hot filament-to-cold filament resistance is desired for maximum lamp life, as shown in Figure 7.

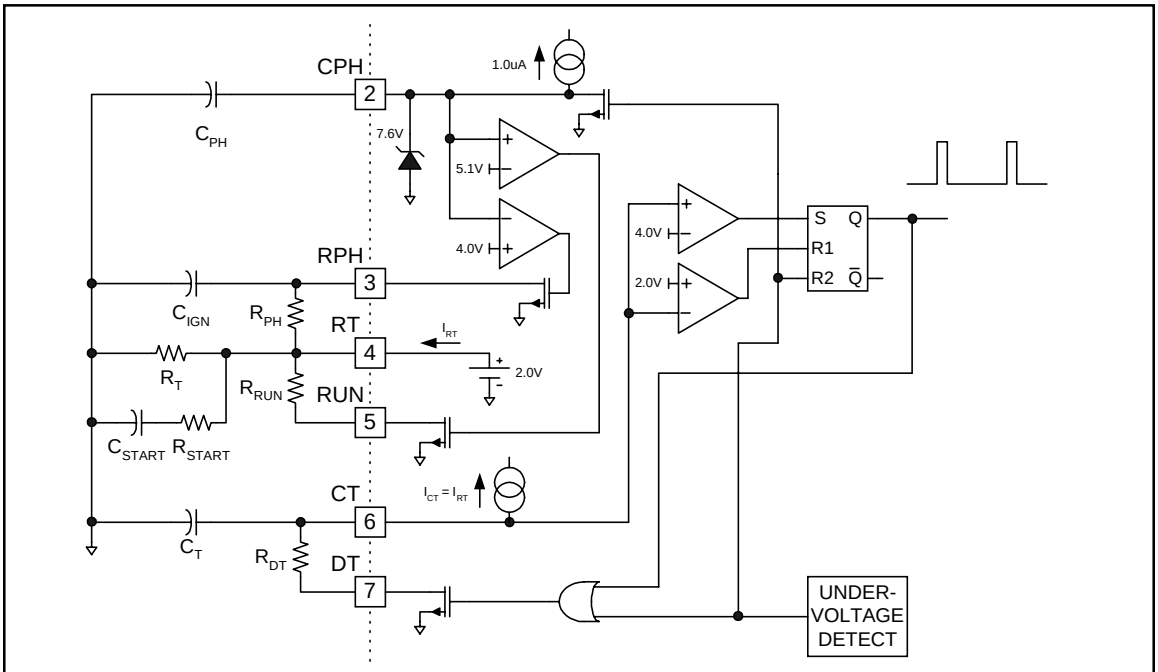


Figure 6: Oscillator section block diagram with external component connection

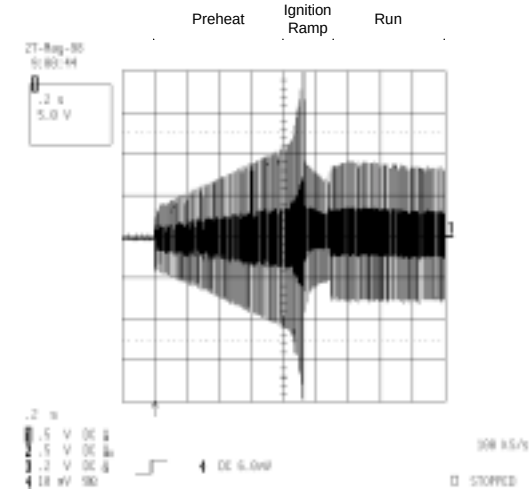


Figure 7: Lamp filament voltage during the preheat, ignition ramp and run modes.

The Preheat Time is programmed by means of the preheat capacitor, C_{PH}, an internal 1µA current source, and an internal threshold on the C_{PH} lead of 4.0V, according to the following formula:

$$t_{PH} = 4.7E6 \cdot C_{PH}, \quad \text{or}$$

$$C_{PH} = 213E-9 \cdot t_{PH}$$

At the end of the Preheat Time, the internal, open-drain transistor holding the R_{PH} lead to ground turns off, and the voltage on this lead charges exponentially up to the R_T lead potential. During this Ignition Ramp Mode, the output frequency exponentially decays to a minimum value. The rate of decay of this frequency is a function of the R_{PH} * C_{PH} time constant. Because the Ignition Ramp Mode ends when the voltage on the C_{PH} lead reaches 5.15V, the Ignition Ramp Mode is always 1/4th as long as the preheat time.
When the C_{PH} lead reaches 5.15V, an open-drain transistor on the RUN lead turns on, and the external R_{RUN} resistor is then in parallel with the R_T resistor. The Run Mode operating frequency is therefore a function of the parallel combination of R_{RUN} and R_T, and this means that the operating power of the lamp can be programmed by means of R_{RUN}.

The following graphs, Figures 8 and 9, illustrate the relationship between the effective R_T resistance (i.e., the parallel combination of resistors which programs the C_T capacitor charging current) and the operating frequency.

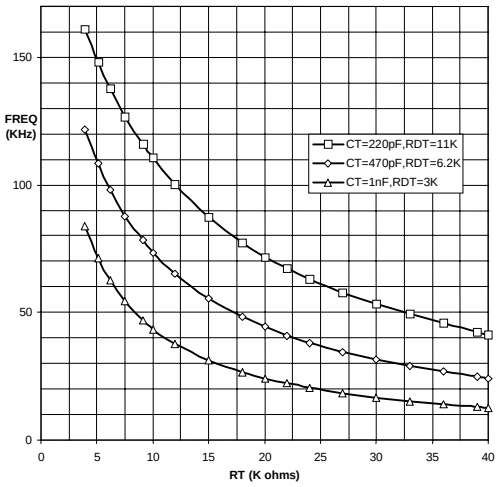


Figure 8: fosc versus effective R_T (t_{DEAD} = 2.0 usec)

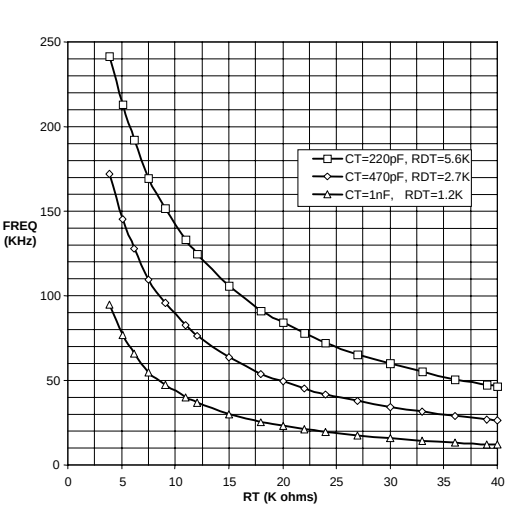


Figure 9: fosc versus effective R_T (t_{DEAD} = 1.0 usec)

Lamp Protection & Automatic Restart Circuitry Operation

Three leads on the IR21571 are used for protection, as shown in Figure 10 below. These are V_{DC} (dc bus monitor), S_D (unlatched shutdown), C_S (latched shutdown) and OC (CS+ threshold programming).

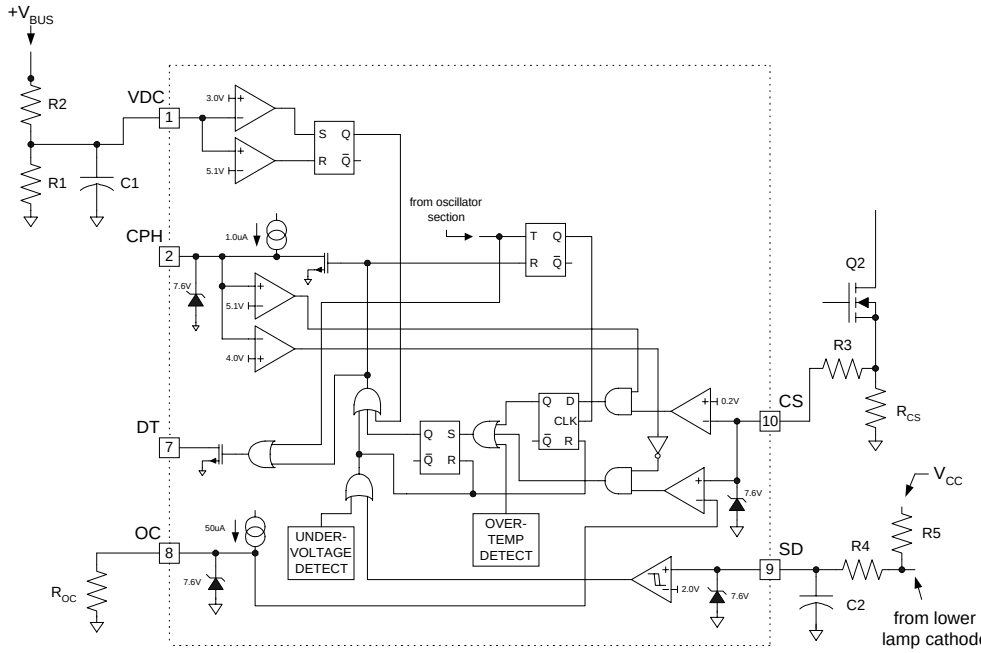


Figure 10: Lamp protection & automatic restart circuitry block diagram with external component connection.

Sensing the DC Bus Voltage

The first of these protection leads senses the voltage on the DC bus by means of an external resistor divider and an internal comparator with hysteresis. When power is first supplied to the IC at system startup, 3 conditions are required before oscillation is initiated: 1.) the voltage on the V_{CC} lead must exceed the rising undervoltage lockout threshold (11.5V), 2.) the voltage at the V_{DC} lead must exceed 5.1V, and 3.) the voltage on the SD lead must be below approximately 1.85V. If a low dc bus condition occurs during normal operation, or if power to the ballast is shut off, the dc bus will collapse prior to the V_{CC} of the chip (assuming the V_{CC} is derived from a charge pump off of the output of the half-bridge). In this case, the voltage on the V_{DC} lead will shut the oscillator off, thereby protecting the power transistors from potentially hazardous hard switching. Approximately 2V of hysteresis has been designed into the internal comparator sensing the V_{DC} lead, in order to account for variations in the dc bus voltage under varying load conditions. When the dc bus recovers, the chip restarts from the beginning of the control sequence, as shown in timing diagram Figure 11.

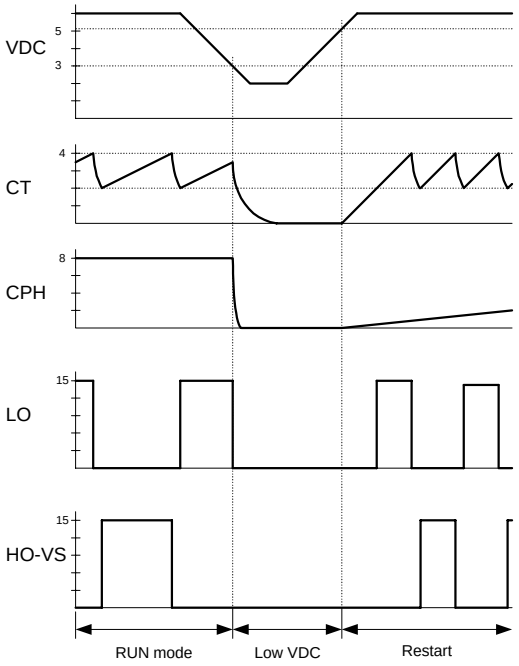


Figure 11: VDC lead fault and auto restart

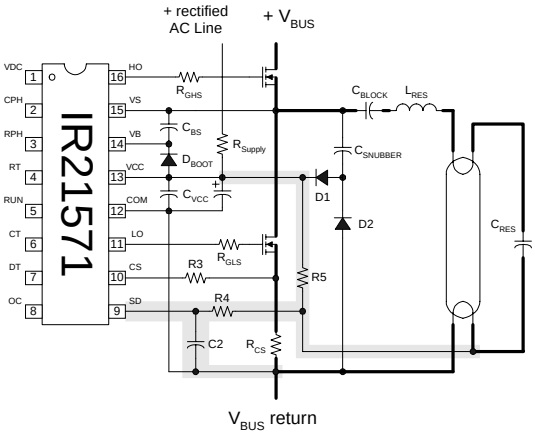


Figure 12: Lamp presence detection circuit connection (shaded area)

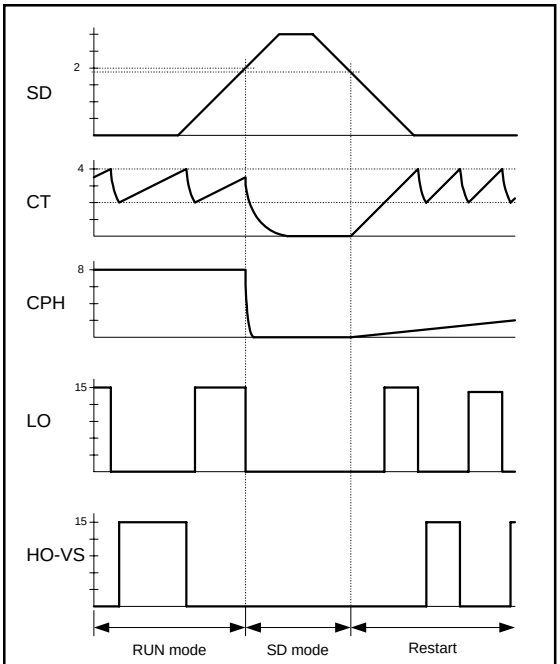


Figure 13: SD lead fault and auto restart

Lamp Presence Detection and Automatic Restart

The second protection lead, SD, is used for both unlatched shutdown and automatic restart functions. The SD lead would normally be connected to an external circuit which senses the presence of the lamp (or lamps), as shown in Figure 12.

When the SD lead exceeds 2.0V (approximately 150mV of hysteresis is included to increase noise immunity), signaling either a lamp fault or lamp removal, the oscillator is disabled, both gate driver outputs are pulled low, and the chip is put into the micropower mode. Since a lamp fault would normally lead to a lamp exchange, when a new lamp is inserted into the fixture, the SD lead would be pulled back to near the ground potential. Under these conditions a reset signal would restart the chip from the beginning of the control sequence, as shown in the timing diagram in Figure 13.

Thus, for a lamp removal and replacement, the ballast automatically restarts the lamp in the proper manner, maximizing lamp life and minimizing stress on the power MOSFETs or IGBTs. The SD lead contains an internal 7.5V zener diode clamp, thereby reducing the number of external components required.

Half-Bridge Current Sensing and Protection

The third lead used for protection is the CS lead, which is normally connected to a resistor in the source of the lower power MOSFET, as shown in Figure 14.

The CS lead is used to sense fault conditions such as failure of a lamp to strike, over-current during normal operation, hard switching, no load, and operation below resonance. If any one of these conditions is sensed, the fault latch is set, the oscillator is disabled, the gate driver outputs go low, and the chip is put into the micropower mode. The CS lead performs its sensing functions on a cycle-by-cycle basis in order to maximize ballast reliability.

For the over-current, failure-to-strike, and hard switching fault conditions, an externally programmable, positive-going CS+ threshold is enabled at the end of the preheat time. The level of this positive-going threshold is determined by the value of the resistor ROC. The value of the resistor ROC is determined by the following formula:

$$R_{OC} = \frac{V_{CS+}}{50E - 6} \text{ or}$$

$$V_{CS+} = 50E - 6 - R_{OC}$$

For the under-current and under-resonance conditions, there is a negative-going CS- threshold of 0.2V which is enabled at the onset of the run mode. The sensing of this CS- threshold is synchronized with the falling edge of the LO output.

Figures 15, 16 and 17 are oscillographs of fault conditions. Figure 15 shows a failure of the lamp to strike, Figure 16 shows a hard switching condition and Figure 17 shows an under-current condition.

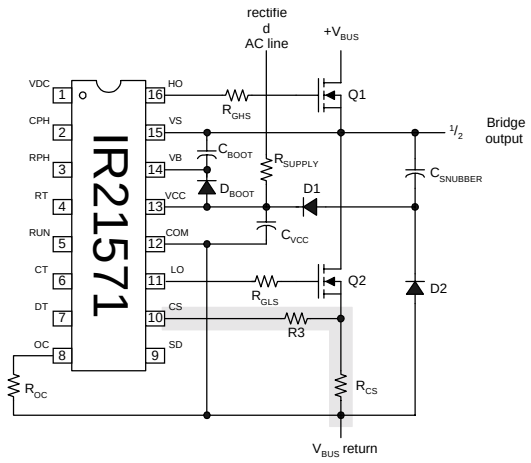


Figure 14: Half-bridge current sensing circuit connection (shaded area)

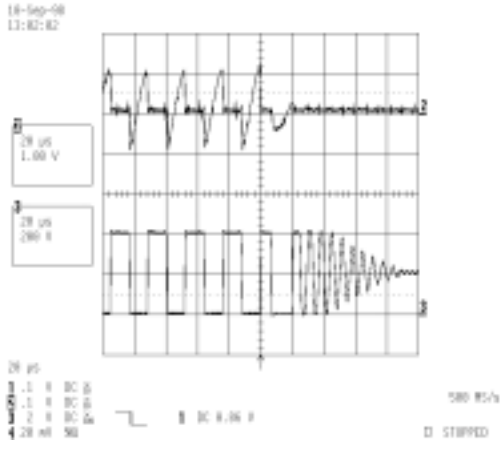


Figure 15: Lamp failure to strike

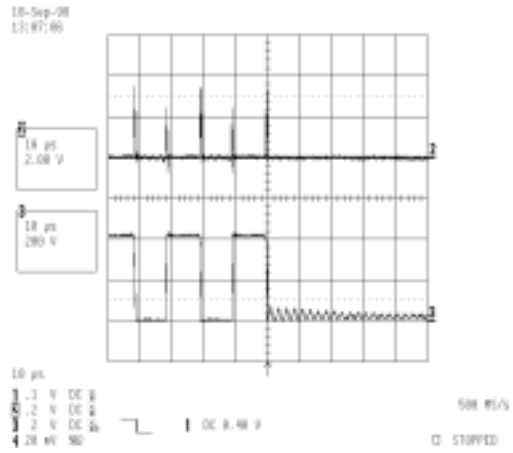


Figure 16: Hard switching condition

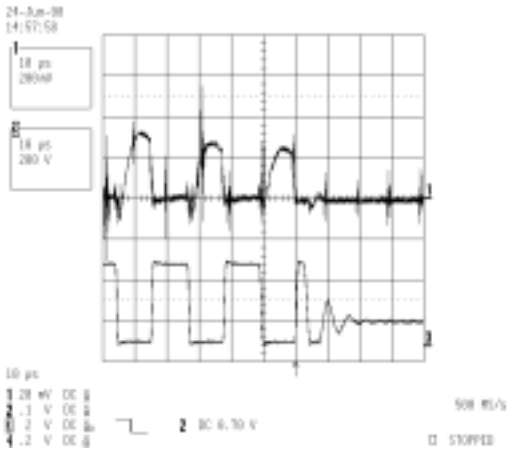


Figure 17: Operation below resonance

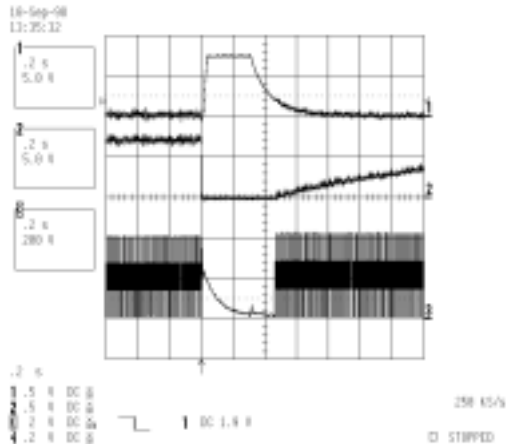


Figure 18: Auto restart for lamp replacement

Recovery from such a fault condition is accomplished by cycling either the SD lead or the V_{CC} lead. When a lamp is removed, the SD lead goes high, the fault latch is reset, and the chip is held off in an unlatched state. Lamp replacement causes the SD lead to go low again, reinitiating the startup sequence. The fault latch can also be reset by the undervoltage lockout signal, if V_{CC} falls below the lower undervoltage threshold.

Bootstrap Supply Considerations

Power is normally supplied to the high-side circuitry by means of a simple charge pump from V_{CC}, as shown in Figure 19.

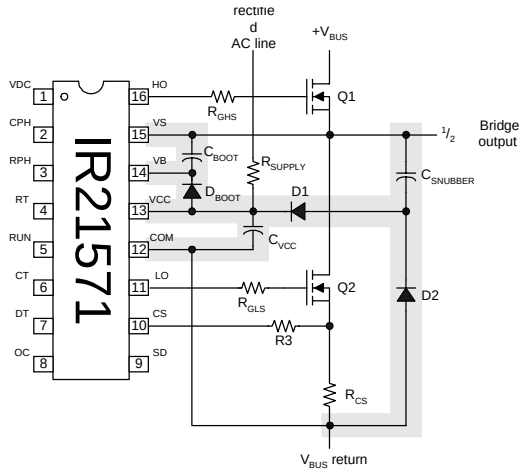


Figure 19: Typical bootstrap supply connection with V_{CC} charge pump from half-bridge output (shaded area)

A high voltage, fast recovery diode D_{BOOT} (the so-called bootstrap diode) is connected between V_{CC} (anode) and VB (cathode), and a capacitor C_{BOOT} (the so-called bootstrap capacitor) is connected between the VB and VS leads. During half-bridge switching, when MOSFET Q2 is on and Q1 is off, the bootstrap capacitor C_{BOOT} is charged from the V_{CC} decoupling capacitor, through the bootstrap diode D_{BOOT}, and through Q2. Alternately, when Q2 is off and Q1 is on, the bootstrap diode is reverse-biased, and the bootstrap capacitor (which ' floats' on the source of the upper power MOSFET) serves as the power supply to the upper gate driver CMOS circuitry. Since the quiescent current in this CMOS circuitry is very low (typically 45µA in the on-state), the majority of the drop in the V_{BS} voltage when Q1 is on occurs due to the transfer of charge from the bootstrap capacitor to the gate of the power MOSFET.

VB should be bypassed to VS as close as possible to the leads of the IC with a low ESR/ESL capacitor. A PCB layout example is shown in figure 20. A rule of thumb for the value of this capacitor is to keep its minimum value at least 50 times the value of the total input capacitance (Ciss) of the MOSFET or IGBT being driven. In addition, the VS lead should be connected directly to the high side power MOSFET source.

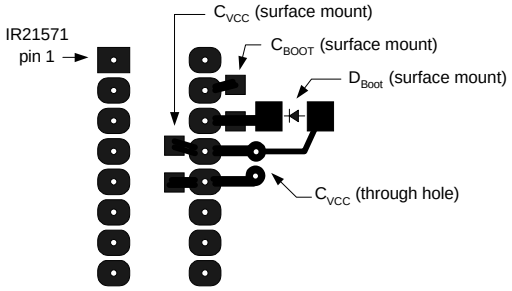
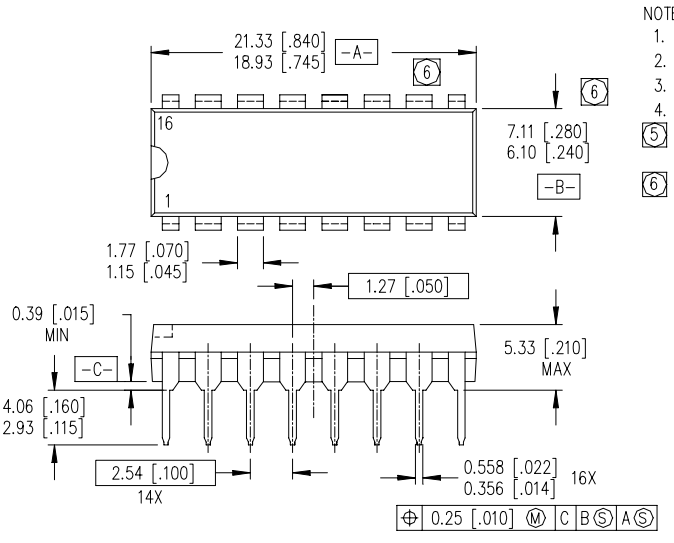
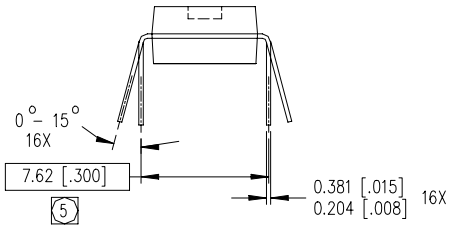


Figure 20: Supply bypassing PCB layout example

Case outlines

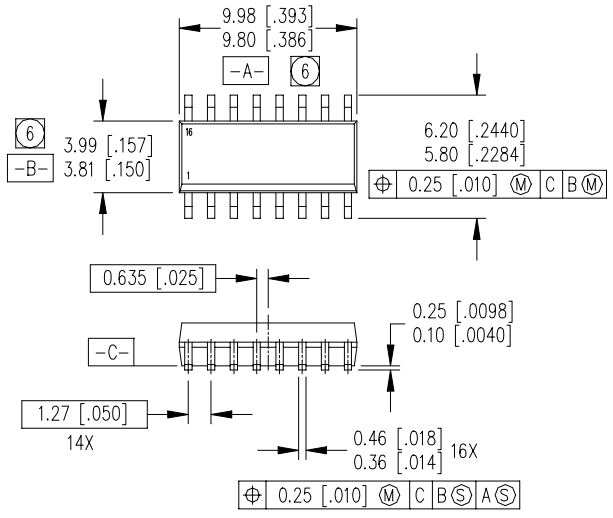


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AA.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

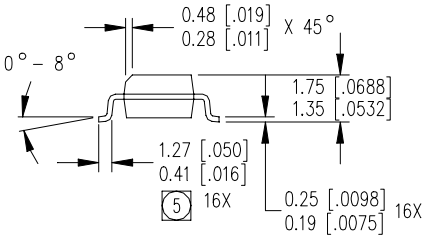


16-Lead PDIP

01-6015
01-3065 00 (MS-001A)



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AC.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



16-Lead SOIC (narrow body)

01-6018
01-3064 00 (MS-012AC)

Data and specifications subject to change without notice 6/28//2003