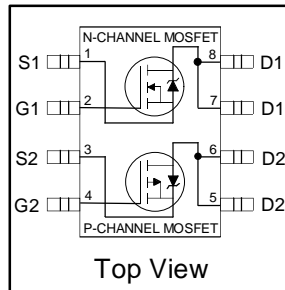


HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

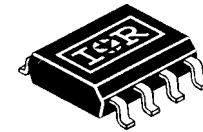


	N-Ch	P-Ch
V_{DS}	30V	-30V
$R_{DS(on)}$	0.050Ω	0.10Ω

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra-red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



SO-8

Absolute Maximum Ratings

Parameter		Max.		Units
		N-Channel	P-Channel	
$I_D @ T_A = 25^\circ\text{C}$	10 Sec. Pulse Drain Current, $V_{GS} @ 10\text{V}$	4.7	-3.5	A
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	4.0	-3.0	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	3.2	-2.4	A
I_{DM}	Pulsed Drain Current $\text{\textcircled{D}}$	16	-12	A
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation (PCB Mount)**	1.4		W
	Linear Derating Factor (PCB Mount)**	0.011		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt $\text{\textcircled{D}}$	6.9	-6.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Amb. (PCB Mount, steady state)**	—	—	90	°C/W

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Description	Type	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.032	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	-0.037	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.050	Ω	$V_{GS} = 10V, I_D = 2.4A$ ③
			—	—	0.080		$V_{GS} = 4.5V, I_D = 2.0A$ ③
		P-Ch	—	—	0.10		$V_{GS} = -10V, I_D = -1.8A$ ③
			—	—	0.16		$V_{GS} = -4.5V, I_D = -1.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-1.0	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	5.2	—	—	S	$V_{DS} = 15V, I_D = 2.4A$ ③
		P-Ch	2.5	—	—		$V_{DS} = -24V, I_D = -1.8A$ ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -24V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	$V_{GS} = \pm 20V$	
Q_g	Total Gate Charge	N-Ch	—	—	25	nC	N-Channel $I_D = 2.6A, V_{DS} = 16V, V_{GS} = 4.5V$ ③
		P-Ch	—	—	25		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	—	2.9	nC	P-Channel $I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V$ ③
		P-Ch	—	—	2.9		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	7.9	nC	P-Channel $I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V$ ③
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	6.8	—	ns	N-Channel $V_{DD} = 10V, I_D = 2.6A, R_G = 6.0\Omega, R_D = 3.8\Omega$ ③
		P-Ch	—	11	—		
t_r	Rise Time	N-Ch	—	21	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega, R_D = 4.5\Omega$ ③
		P-Ch	—	17	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	22	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega, R_D = 4.5\Omega$ ③
		P-Ch	—	25	—		
t_f	Fall Time	N-Ch	—	7.7	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega, R_D = 4.5\Omega$ ③
		P-Ch	—	18	—		
L_D	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead tip and center of die contact
L_S	Internal Source Inductance	N-P	—	6.0	—		
C_{iss}	Input Capacitance	N-Ch	—	520	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	440	—		
C_{oss}	Output Capacitance	N-Ch	—	180	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	200	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	72	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	93	—		

Source-Drain Ratings and Characteristics

Parameter	Description	Type	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.8	A	
		P-Ch	—	—	-1.8		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	16	A	
		P-Ch	—	—	-12		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 1.8A, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.0		$T_J = 25^\circ\text{C}, I_S = -1.8A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	47	71	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 2.6A, di/dt = 100A/\mu s$ ③
		P-Ch	—	53	80		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	56	84	nC	P-Channel $T_J = 25^\circ\text{C}, I_F = -2.2A, di/dt = 100A/\mu s$ ③
		P-Ch	—	66	99		
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is negligible (turn-on is dominated by I_S+I_D)				

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)

② N-Channel $I_{SD} \leq 2.4A, di/dt \leq 73A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
 P-Channel $I_{SD} \leq -1.8A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

N-Channel

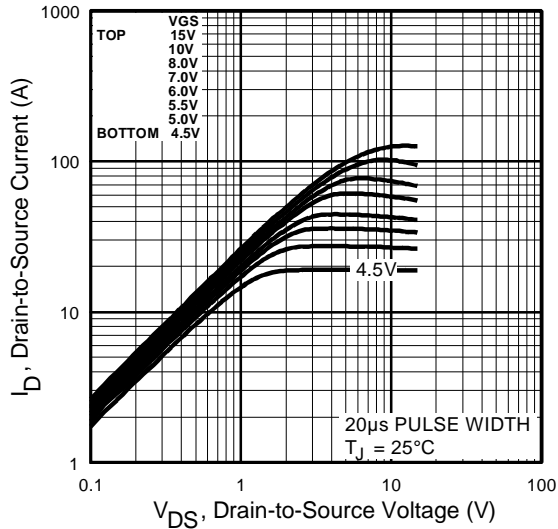


Fig 1. Typical Output Characteristics,
 $T_J = 25^\circ\text{C}$

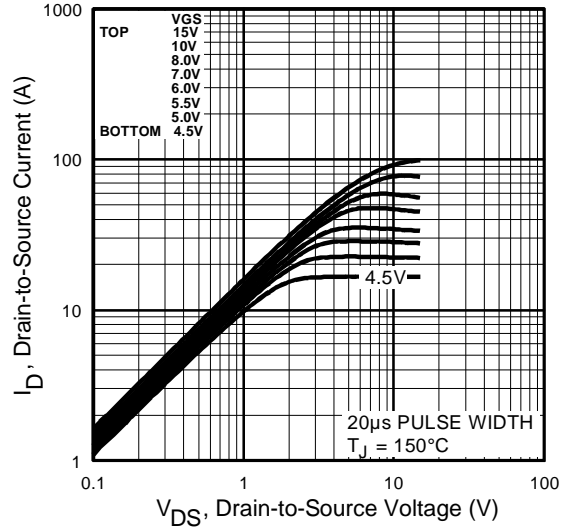


Fig 2. Typical Output Characteristics,
 $T_J = 150^\circ\text{C}$

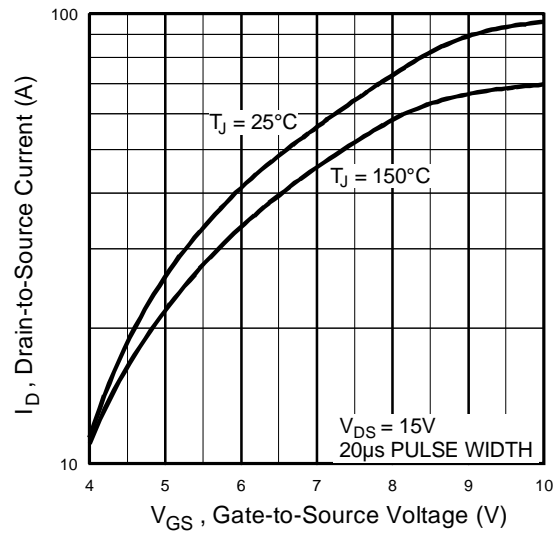


Fig 3. Typical Transfer Characteristics

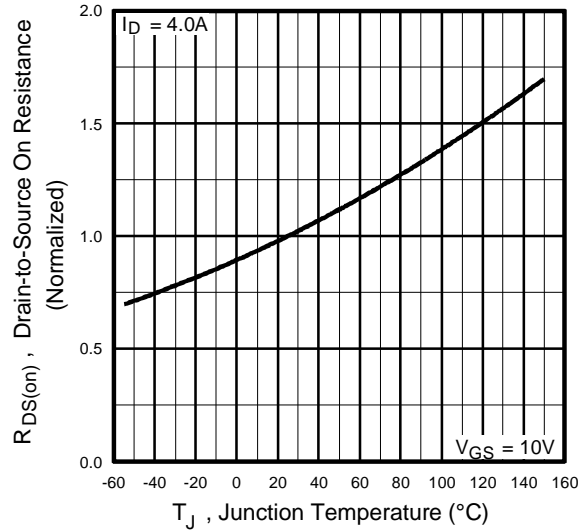


Fig 4. Normalized On-Resistance
Vs. Temperature

N-Channel

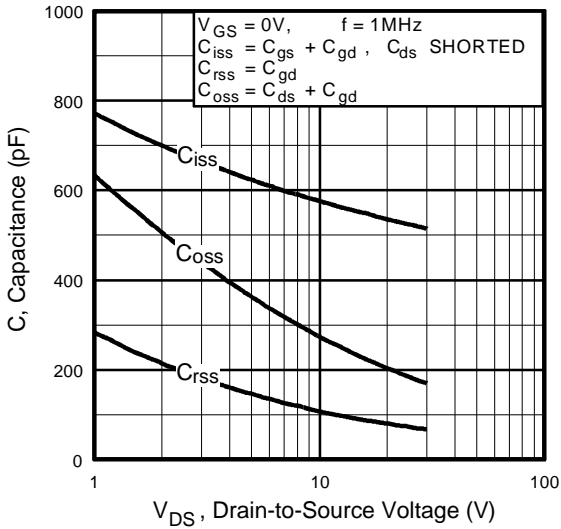


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

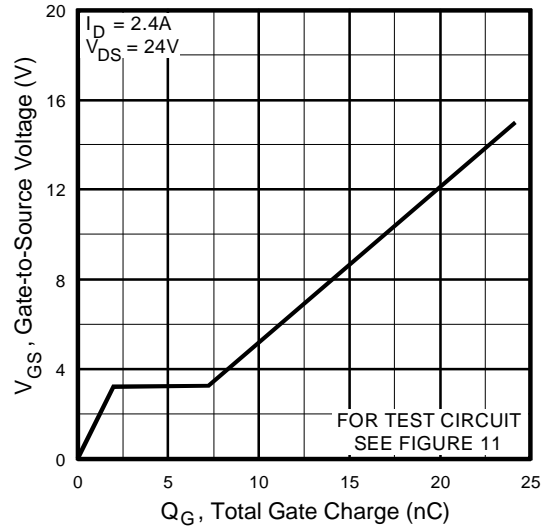


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

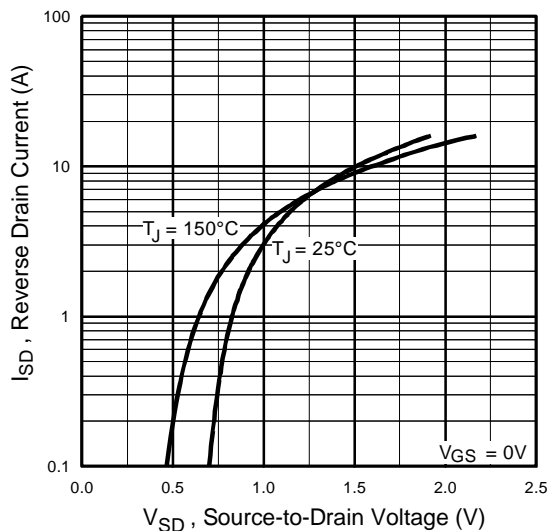


Fig 7. Typical Source-Drain Diode Forward Voltage

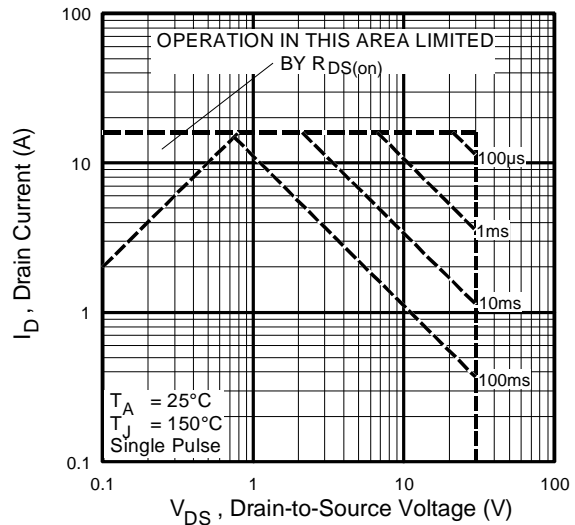


Fig 8. Maximum Safe Operating Area

N-Channel

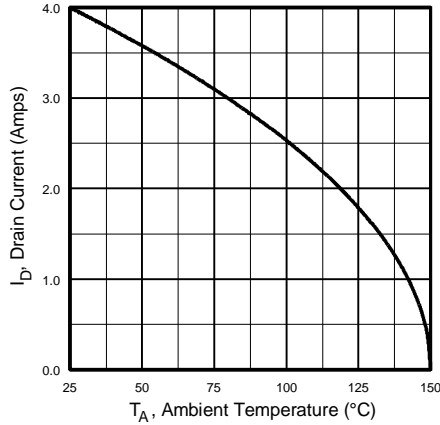


Fig 9. Max. Drain Current Vs. Ambient Temp.

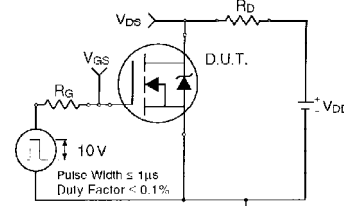


Fig 10a. Switching Time Test Circuit

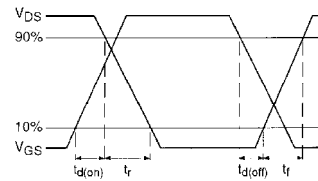


Fig 10b. Switching Time Waveforms

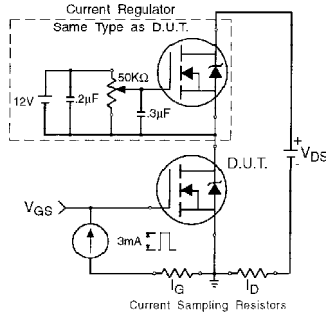


Fig 11a. Gate Charge Test Circuit

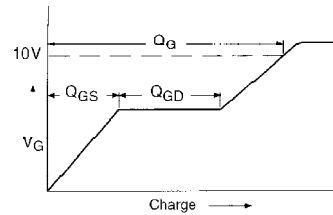


Fig 11b. Basic Gate Charge Waveform

P-Channel

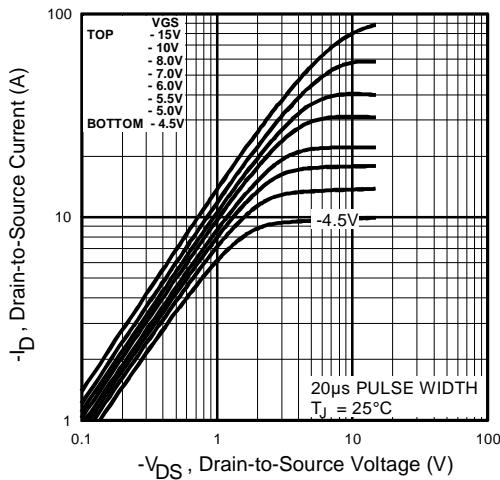


Fig 12. Typical Output Characteristics, $T_J = 25^\circ\text{C}$

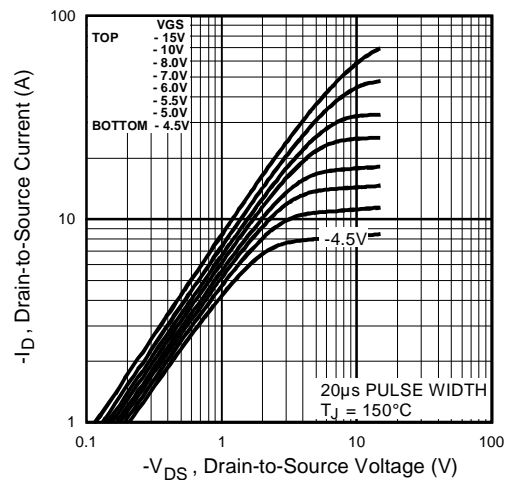


Fig 13. Typical Output Characteristics, $T_J = 150^\circ\text{C}$

P-Channel

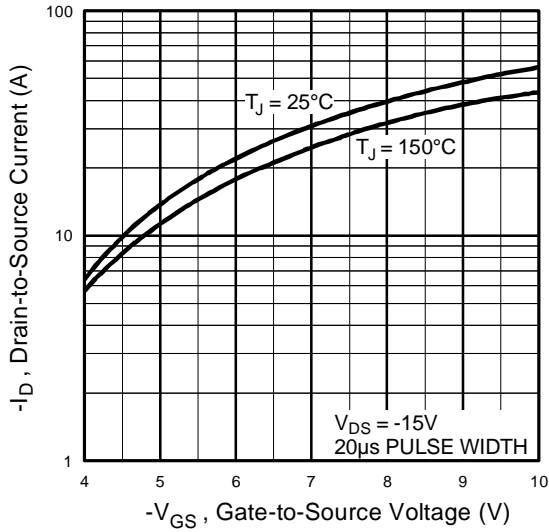


Fig 14. Typical Transfer Characteristics

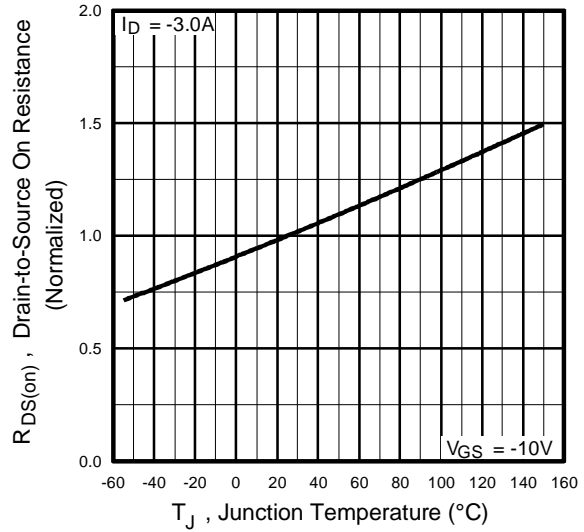


Fig 15. Normalized On-Resistance Vs. Temperature

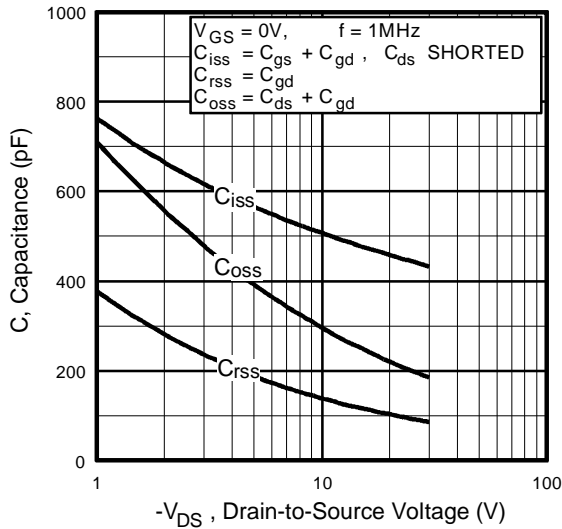


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

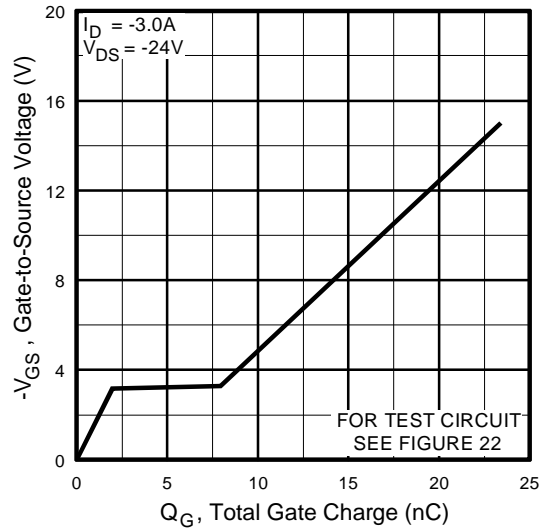


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

P-Channel

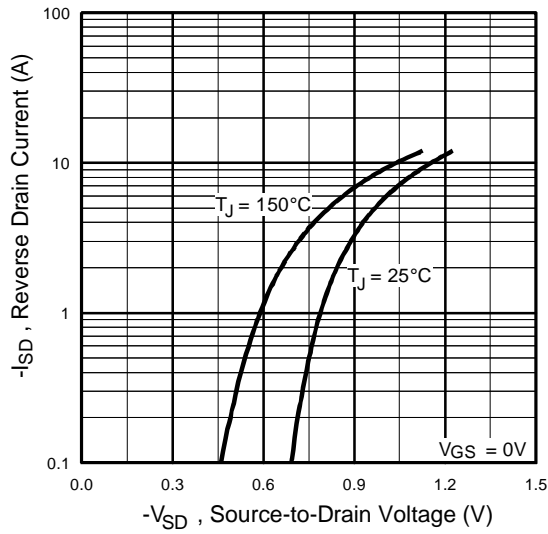


Fig 18. Typical Source-Drain Diode Forward Voltage

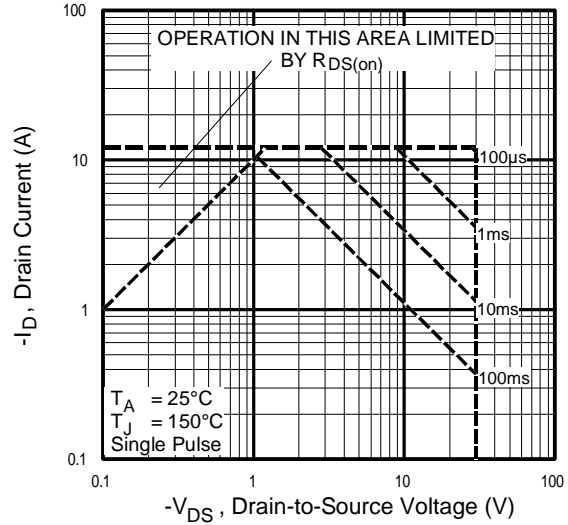


Fig 19. Maximum Safe Operating Area

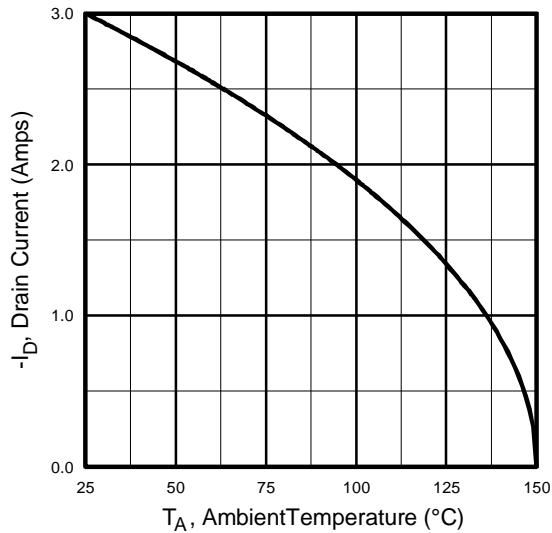


Fig 20. Max. Drain Current Vs. Ambient Temp.

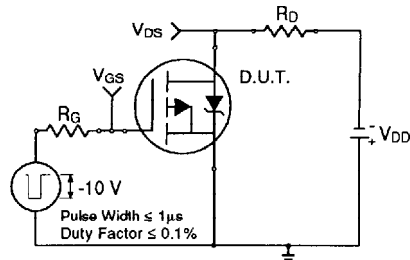


Fig 21a. Switching Time Test Circuit

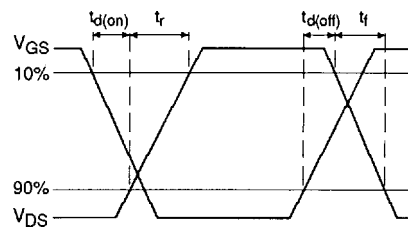


Fig 21b. Switching Time Waveforms

P-Channel

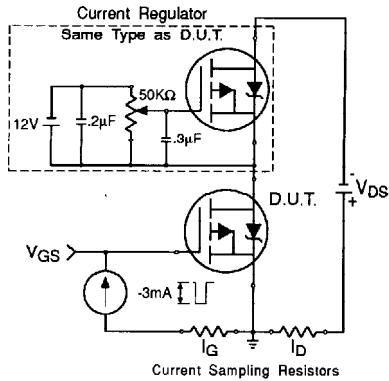


Fig 22b. Gate Charge Test Circuit

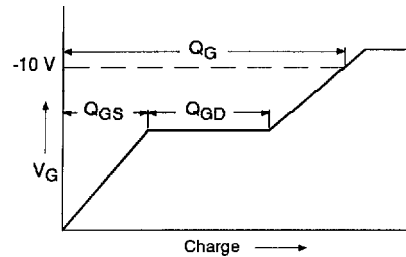


Fig 22b. Basic Gate Charge Waveform

N- and P-Channel

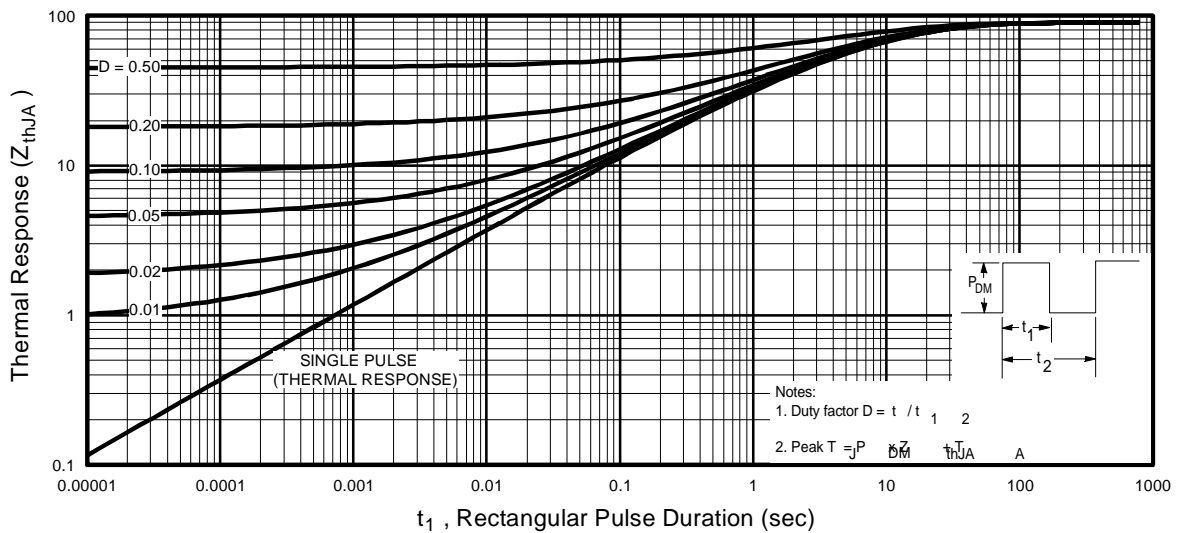


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Refer to the Appendix Section for the following:

Appendix A: Figure 24, Peak Diode Recovery dv/dt Test Circuit — See page 329.

Appendix B: Package Outline Mechanical Drawing — See page 332.

Appendix C: Part Marking Information — See page 332.

Appendix D: Tape and Reel Information — See page 336.