

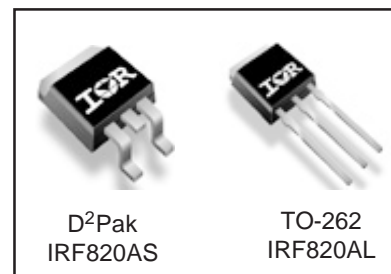
**Applications**

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
500V	3.0Ω	2.5A

**Benefits**

- Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C<sub>OSS</sub> specified (See AN 1001)



**Absolute Maximum Ratings**

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>⑥</sup>	2.5	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>⑥</sup>	1.6	
I <sub>DM</sub>	Pulsed Drain Current <sup>①</sup> ⑥	10	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	50	W
	Linear Derating Factor	0.4	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt <sup>③</sup> ⑥	3.4	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Typical SMPS Topologies:**

- Two Transistor Forward
- Half Bridge and Full Bridge

Notes <sup>①</sup> through <sup>⑤</sup> are on page 8  
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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.0	$\Omega$	$V_{GS} = 10V, I_D = 1.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	1.4	—	—	S	$V_{DS} = 50V, I_D = 1.5A$ ⑥
$Q_g$	Total Gate Charge	—	—	17	nC	$I_D = 2.5A$
$Q_{gs}$	Gate-to-Source Charge	—	—	4.3		$V_{DS} = 400V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	8.5		$V_{GS} = 10V$ , See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	8.1	—	ns	$V_{DD} = 250V$
$t_r$	Rise Time	—	12	—		$I_D = 2.5A$
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		$R_G = 21\Omega$
$t_f$	Fall Time	—	13	—		$R_D = 97\Omega$ , See Fig. 10 ④⑥
$C_{iss}$	Input Capacitance	—	340	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	53	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	2.7	—		$f = 1.0\text{MHz}$ , See Fig. 5⑥
$C_{oss}$	Output Capacitance	—	490	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	15	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	28	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤⑥

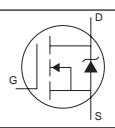
## Avalanche Characteristics

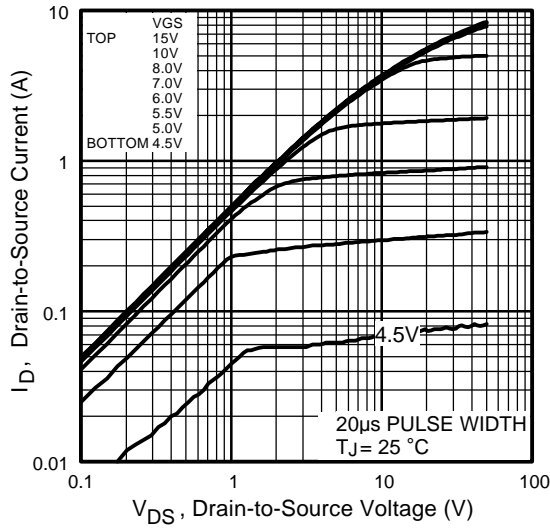
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②⑥	—	140	mJ
$I_{AR}$	Avalanche Current①	—	2.5	A
$E_{AR}$	Repetitive Avalanche Energy①	—	5.0	mJ

## Thermal Resistance

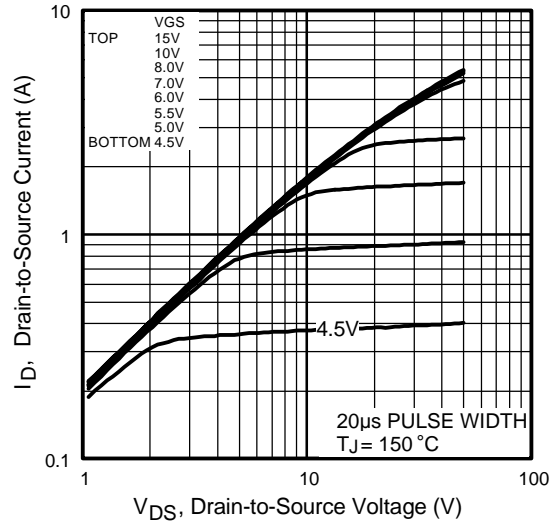
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	—	62	

## Diode Characteristics

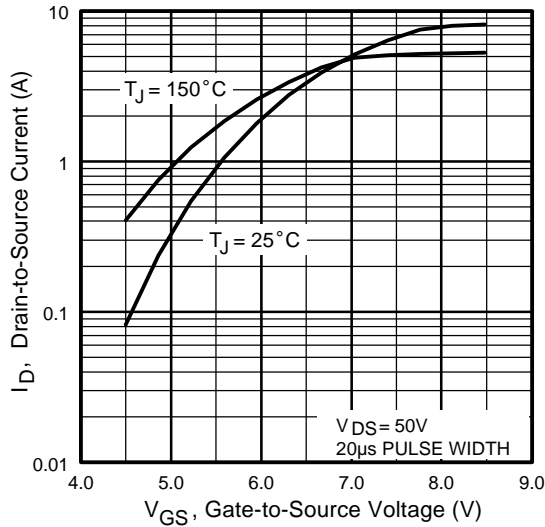
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①⑥	—	—	10		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 2.5A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	330	500	ns	$T_J = 25^\circ\text{C}, I_F = 2.5A$
$Q_{rr}$	Reverse Recovery Charge	—	760	1140	nC	$di/dt = 100A/\mu s$ ④⑥
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				



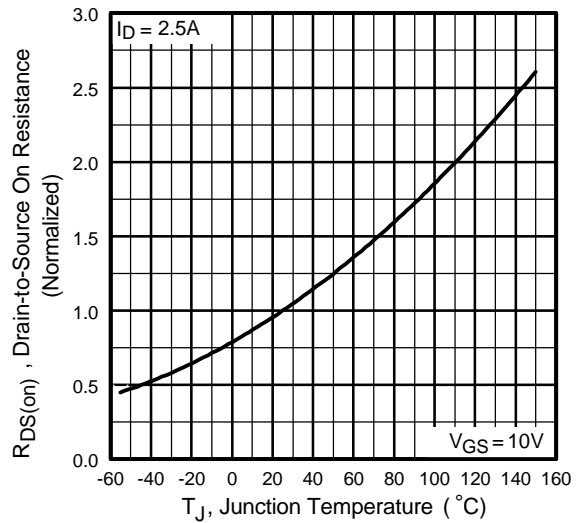
**Fig 1.** Typical Output Characteristics



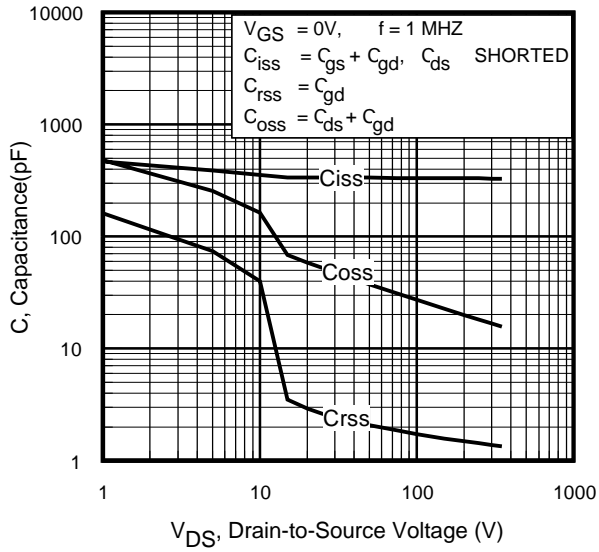
**Fig 2.** Typical Output Characteristics



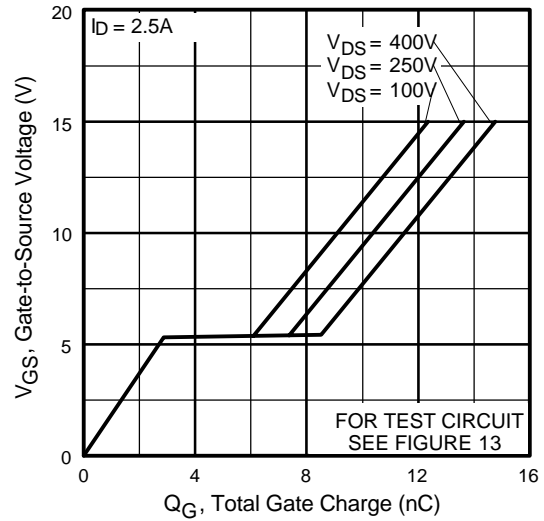
**Fig 3.** Typical Transfer Characteristics



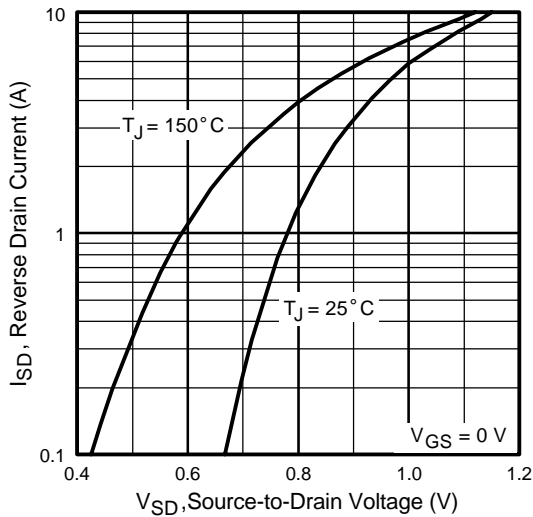
**Fig 4.** Normalized On-Resistance Vs. Temperature



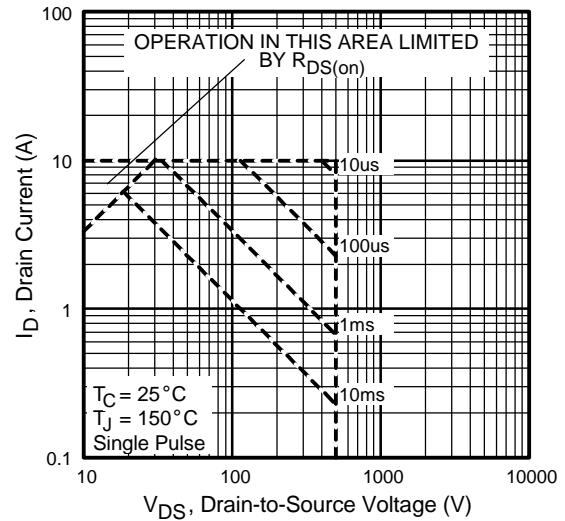
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



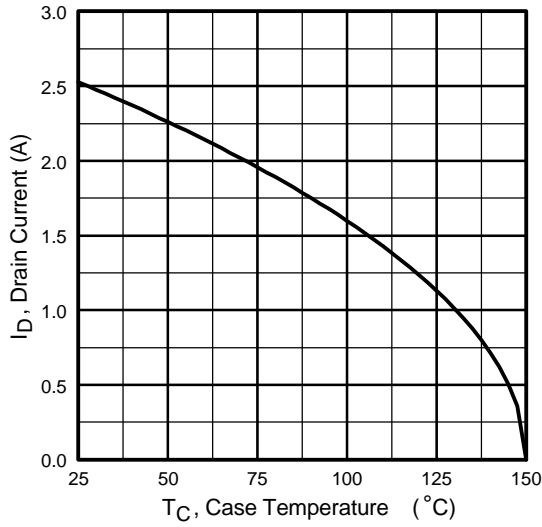
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



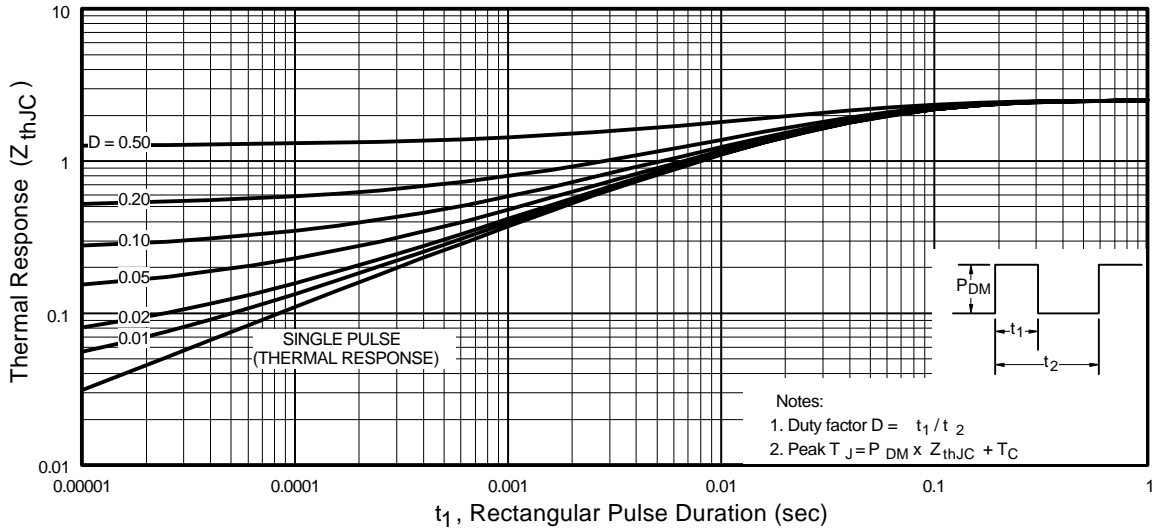
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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**Fig 12a.** Unclamped Inductive Test Circuit



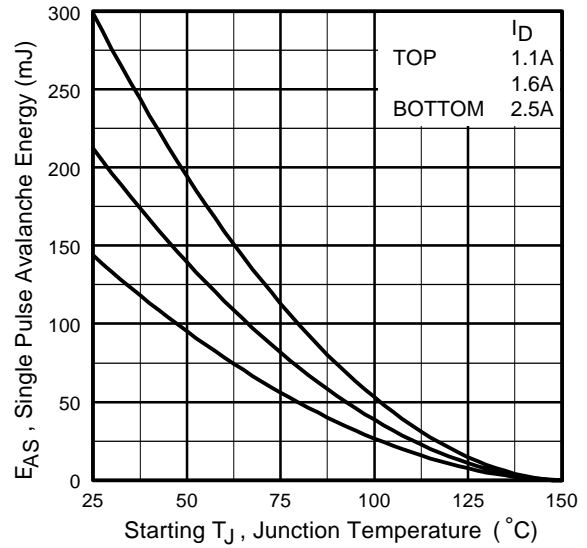
**Fig 12b.** Unclamped Inductive Waveforms



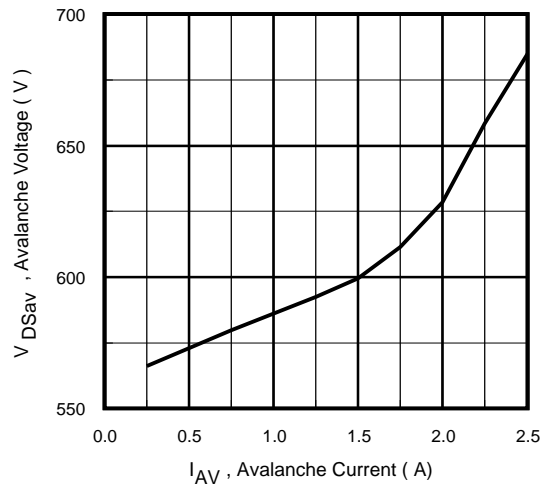
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

**Peak Diode Recovery dv/dt Test Circuit**



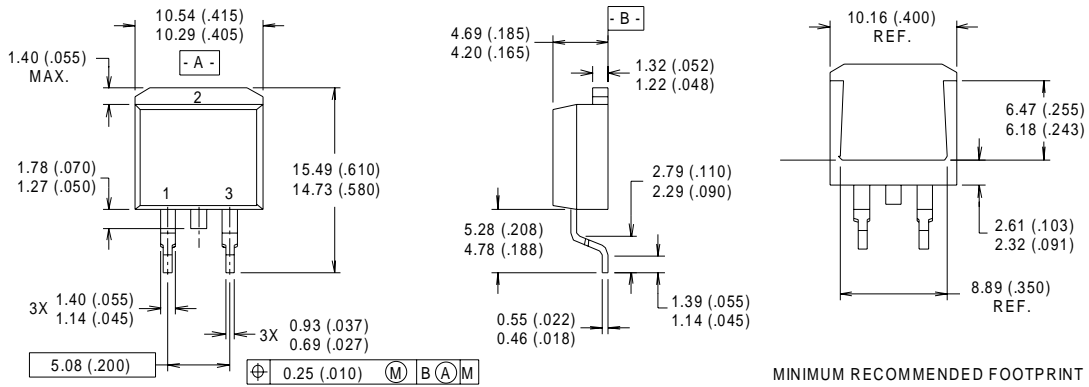
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® power MOSFETs

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## D<sup>2</sup>Pak Package Outline



**NOTES:**

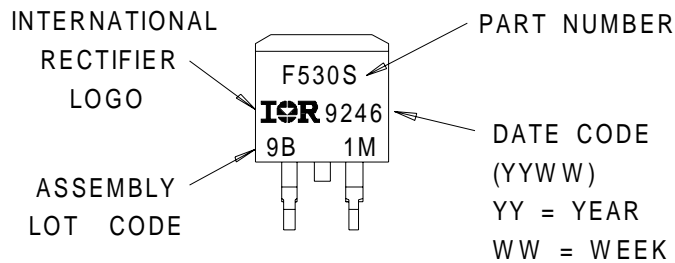
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

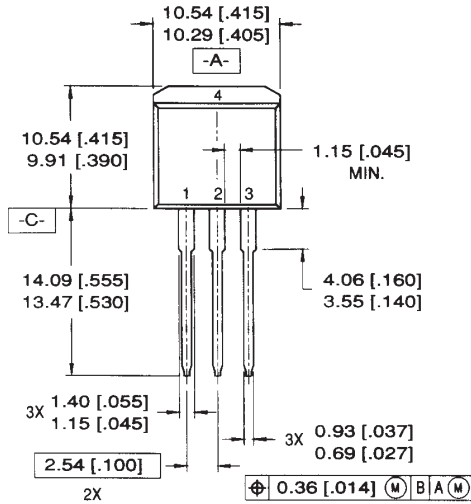
## Part Marking Information

### D<sup>2</sup>Pak



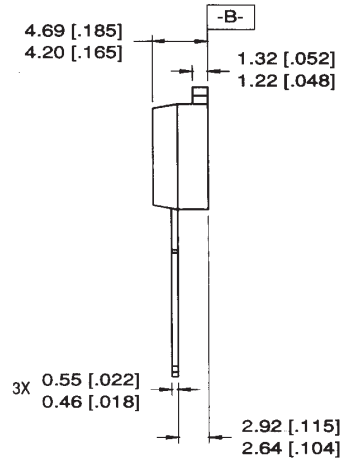


## Package Outline TO-262



**LEAD ASSIGNMENTS**

- 1 = GATE      3 = SOURCE
- 2 = DRAIN    4 = DRAIN

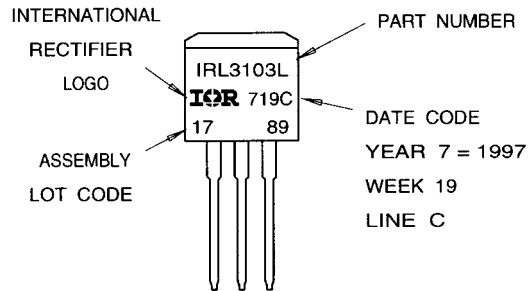


**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## Part Marking Information TO-262

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

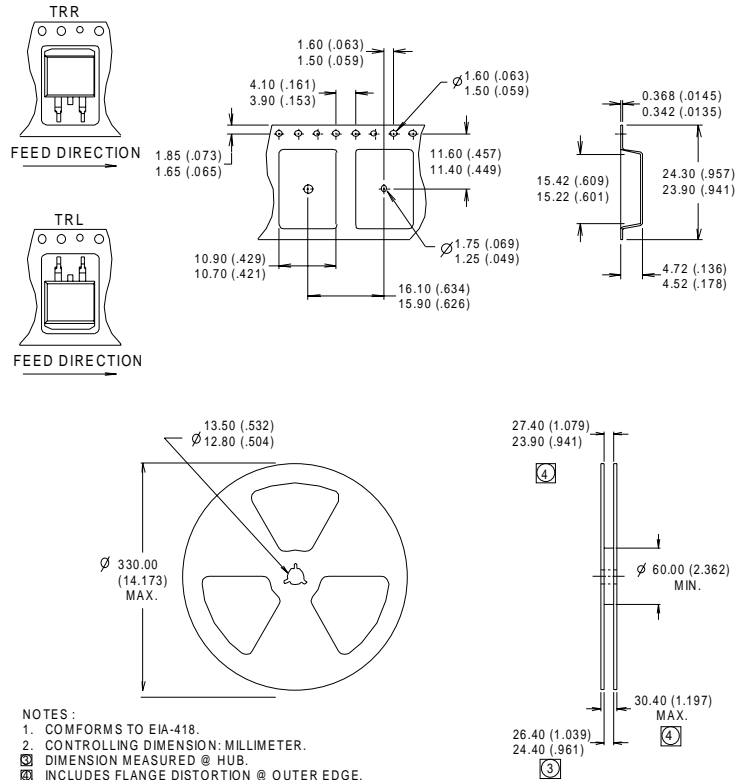


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## Tape & Reel Information

D<sup>2</sup>Pak



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 45\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 2.5\text{A}$ . (See Figure 12)
- ③  $I_{SD} \leq 2.5\text{A}$ ,  $di/dt \leq 270\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ Uses IRF820A data and test conditions

\* When mounted on 1" square PCB ( FR-4 or G-10 Material ).

For recommended footprint and soldering techniques refer to application note #AN-994.

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**IR CANADA:** 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590

**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111

**IR JAPAN:** K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086

**IR SOUTHEAST ASIA:** 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630

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Data and specifications subject to change without notice. 5/00