

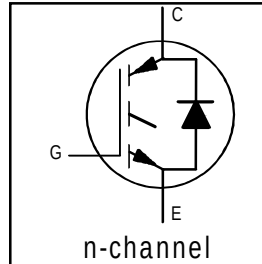
IRG4BC20SD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH
ULTRAFAST SOFT RECOVERY DIODE

Standard Speed IGBT

Features

- Extremely low voltage drop 1.4Vtyp. @ 10A
- S-Series: Minimizes power dissipation at up to 3 KHz PWM frequency in inverter drives, up to 4 KHz in brushless DC drives.
- Very Tight Vce(on) distribution
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard D²Pak package



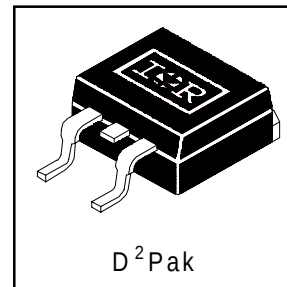
$$V_{CES} = 600V$$

$$V_{CE(on)} \text{ typ.} = 1.4V$$

$$@V_{GE} = 15V, I_C = 10A$$

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's . Minimized recovery characteristics require less/no snubbing
- Lower losses than MOSFET's conduction and Diode losses



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{CES}	Collector-to-Emitter Voltage	600	V
I _C @ T _C = 25°C	Continuous Collector Current	19	A
I _C @ T _C = 100°C	Continuous Collector Current	10	
I _{CM}	Pulsed Collector Current ①	38	
I _{LM}	Clamped Inductive Load Current ②	38	
I _F @ T _C = 100°C	Diode Continuous Forward Current	7.0	
I _{FM}	Diode Maximum Forward Current	38	V
V _{GE}	Gate-to-Emitter Voltage	± 20	
P _D @ T _C = 25°C	Maximum Power Dissipation	60	W
P _D @ T _C = 100°C	Maximum Power Dissipation	24	
T _J	Operating Junction and	-55 to +150	°C
T _{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{qJC}	Junction-to-Case - IGBT	—	2.1	°C/W
R _{qJC}	Junction-to-Case - Diode	—	3.5	
R _{qJA}	Junction-to-Ambient (PCB Mounted,steady-state)*	—	80	
Wt	Weight	1.44	—	g (oz)

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage ^f	600	—	—	V	$V_{GE} = 0V$, $I_C = 250\mu A$
$DV_{(BR)CES}/DT_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/ $^\circ\text{C}$	$V_{GE} = 0V$, $I_C = 1.0mA$
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.40	1.6	V	$I_C = 10A$ $V_{GE} = 15V$
		—	1.85	—		$I_C = 19A$ See Fig. 2, 5
		—	1.44	—		$I_C = 10A$, $T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}$, $I_C = 250\mu A$
$dV_{GE(th)}/dT_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/ $^\circ\text{C}$	$V_{CE} = V_{GE}$, $I_C = 250\mu A$
g_{fe}	Forward Transconductance ④	2.0	5.8	—	S	$V_{CE} = 100V$, $I_C = 10A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V$, $V_{CE} = 600V$
		—	—	1700		$V_{GE} = 0V$, $V_{CE} = 600V$, $T_J = 150^\circ\text{C}$
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	$I_C = 8.0A$ See Fig. 13
		—	1.3	1.6		$I_C = 8.0A$, $T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	40	nC	$I_C = 10A$
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.3	6.5		$V_{CC} = 400V$ See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	15		$V_{GE} = 15V$
$t_{d(on)}$	Turn-On Delay Time	—	62	—	ns	$T_J = 25^\circ\text{C}$
t_r	Rise Time	—	32	—		$I_C = 10A$, $V_{CC} = 480V$
$t_{d(off)}$	Turn-Off Delay Time	—	690	1040		$V_{GE} = 15V$, $R_G = 50\Omega$
t_f	Fall Time	—	480	730	mJ	Energy losses include "tail" and diode reverse recovery.
E_{on}	Turn-On Switching Loss	—	0.32	—		See Fig. 9, 10, 11, 18
E_{off}	Turn-Off Switching Loss	—	2.58	—		
E_{ts}	Total Switching Loss	—	2.90	4.5	mJ	$T_J = 150^\circ\text{C}$, See Fig. 10, 11, 18
$t_{d(on)}$	Turn-On Delay Time	—	64	—		$I_C = 10A$, $V_{CC} = 480V$
t_r	Rise Time	—	35	—		$V_{GE} = 15V$, $R_G = 50\Omega$
$t_{d(off)}$	Turn-Off Delay Time	—	980	—	mJ	Energy losses include "tail" and diode reverse recovery.
t_f	Fall Time	—	800	—		
E_{ts}	Total Switching Loss	—	4.33	—		
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	550	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	39	—		$V_{CC} = 30V$ See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	7.1	—		$f = 1.0MHz$
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	$T_J = 25^\circ\text{C}$ See Fig. 14
		—	55	90		$T_J = 125^\circ\text{C}$
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	$T_J = 25^\circ\text{C}$ See Fig. 15
		—	4.5	8.0		$T_J = 125^\circ\text{C}$
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	$T_J = 25^\circ\text{C}$ See Fig. 16
		—	124	360		$T_J = 125^\circ\text{C}$
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	240	—	A/ μs	$T_J = 25^\circ\text{C}$ See Fig. 17
		—	210	—		$T_J = 125^\circ\text{C}$

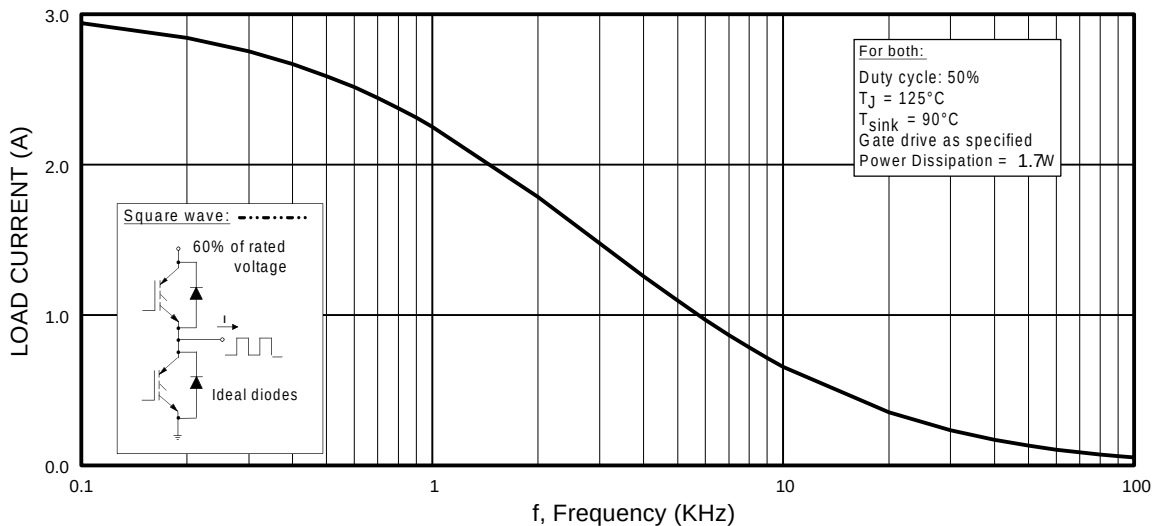


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

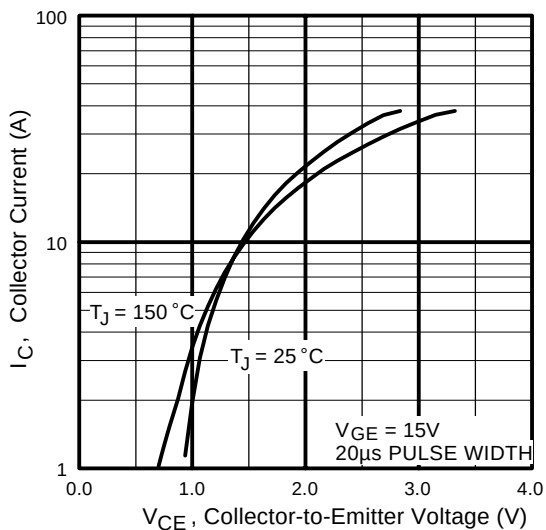


Fig. 2 - Typical Output Characteristics

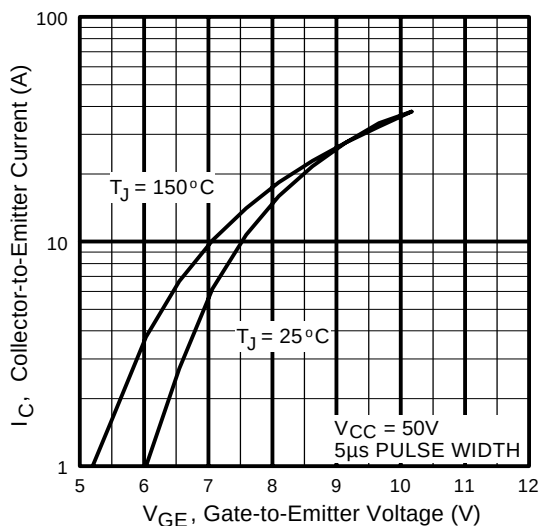


Fig. 3 - Typical Transfer Characteristics

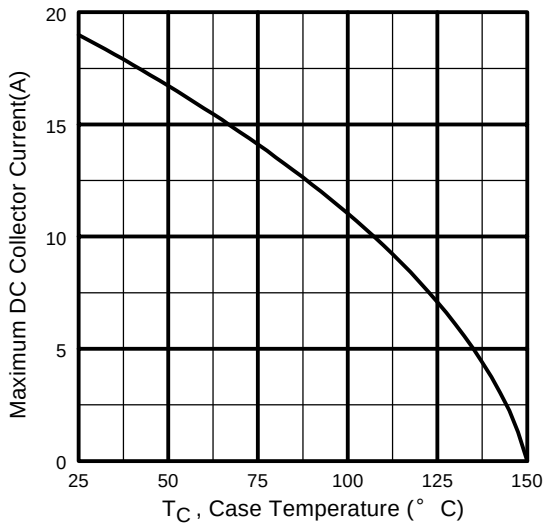


Fig. 4 - Maximum Collector Current vs. Case Temperature

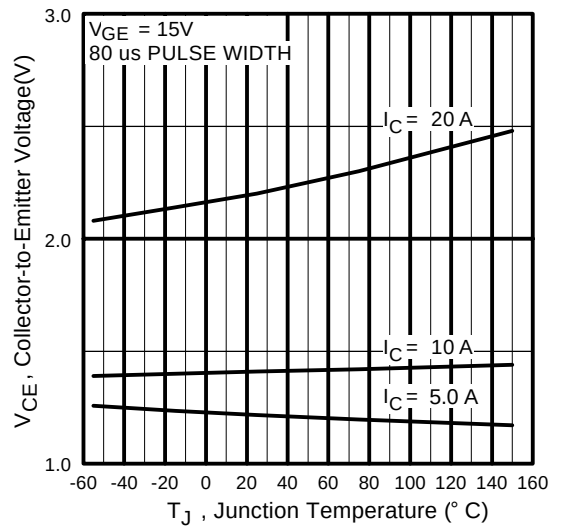


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

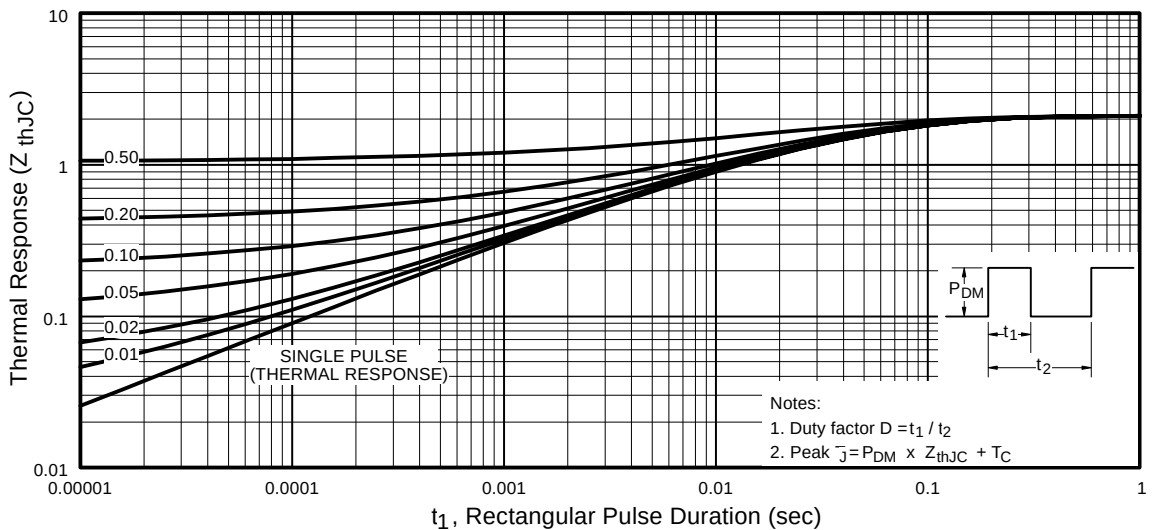


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

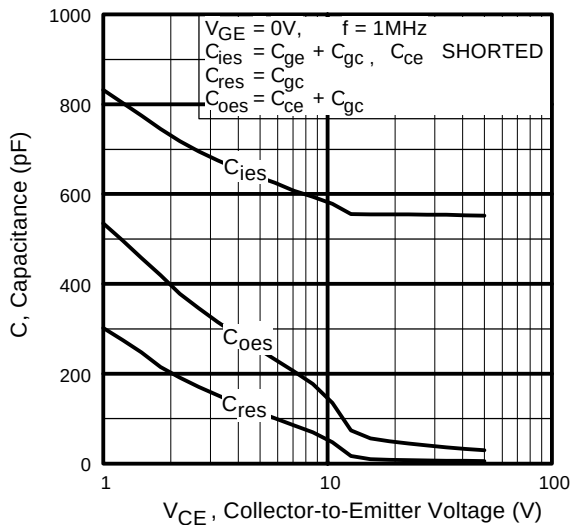


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

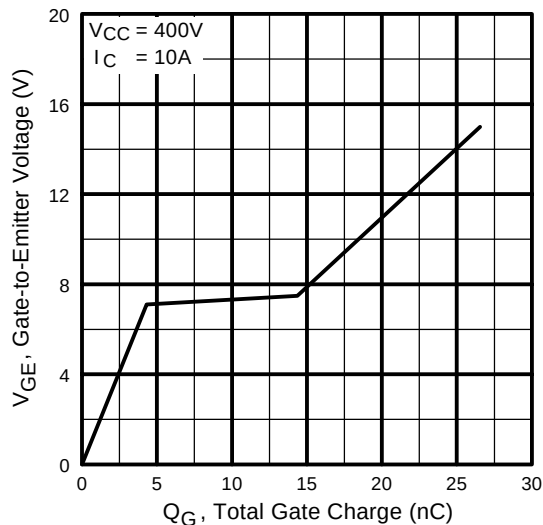


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

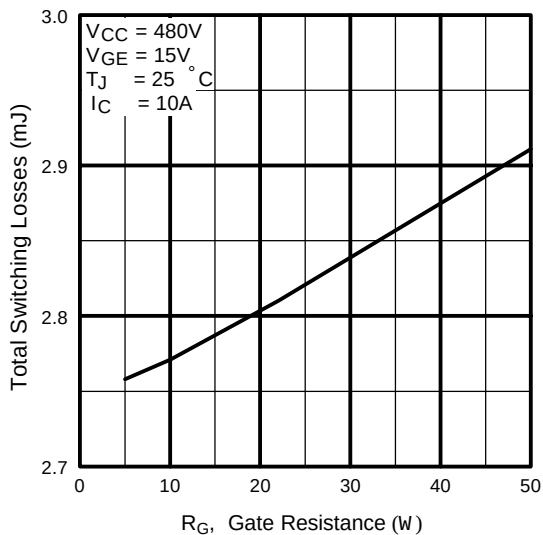


Fig. 9 - Typical Switching Losses vs. Gate Resistance

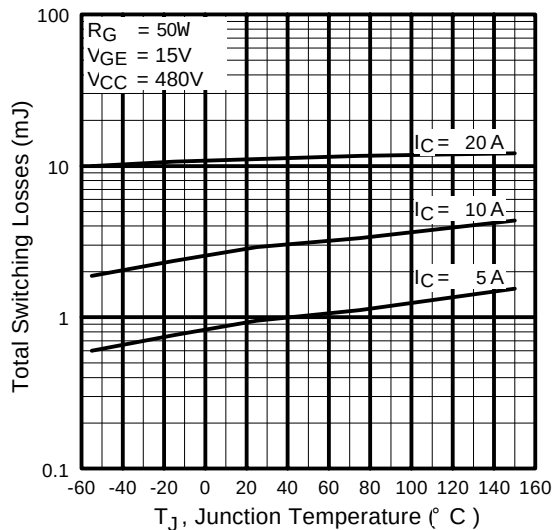


Fig. 10 - Typical Switching Losses vs. Junction Temperature

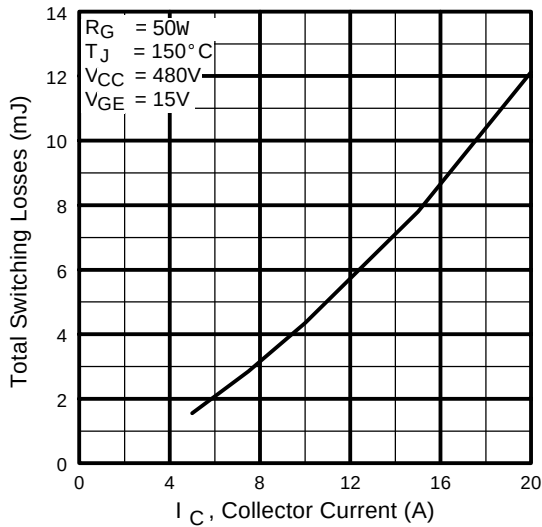


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

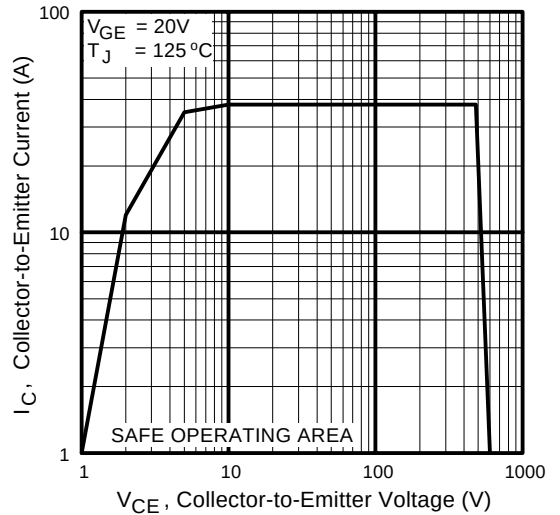


Fig. 12 - Turn-Off SOA

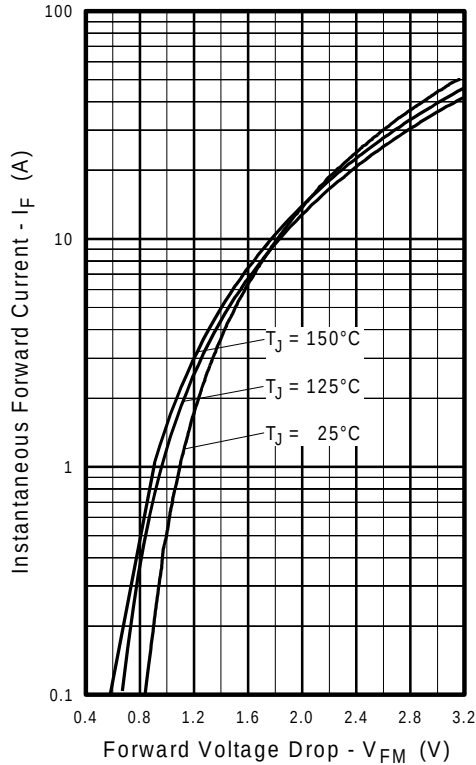


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

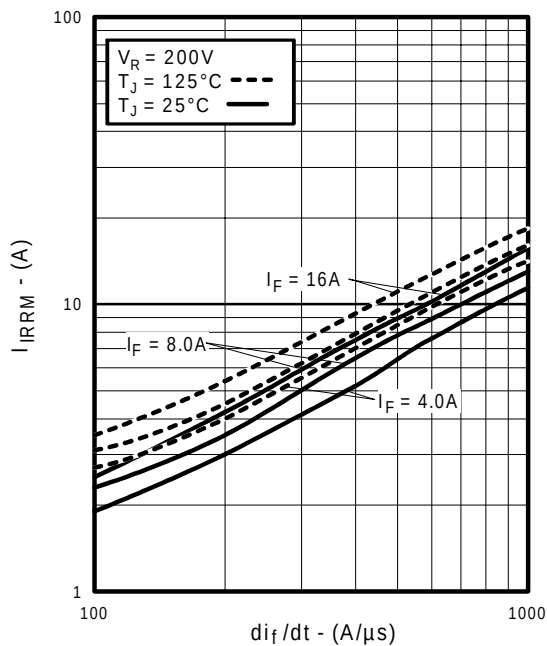
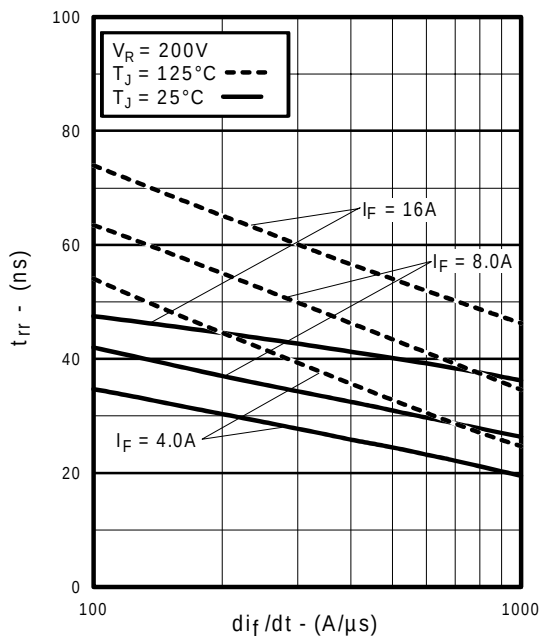


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

Fig. 15 - Typical Recovery Current vs. di_f/dt

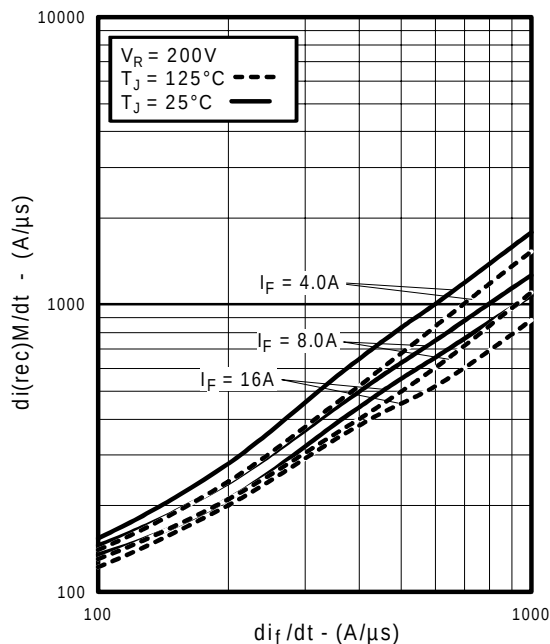
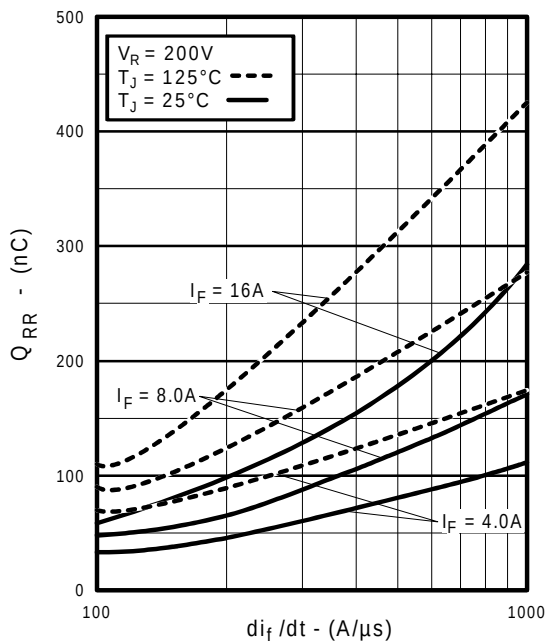


Fig. 16 - Typical Stored Charge vs. di_f/dt
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Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

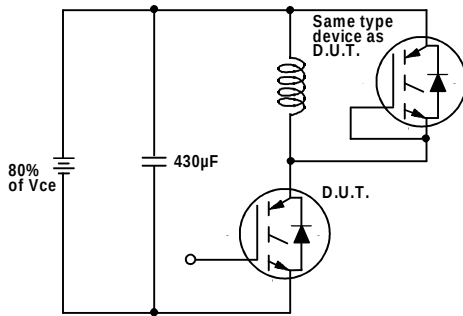


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

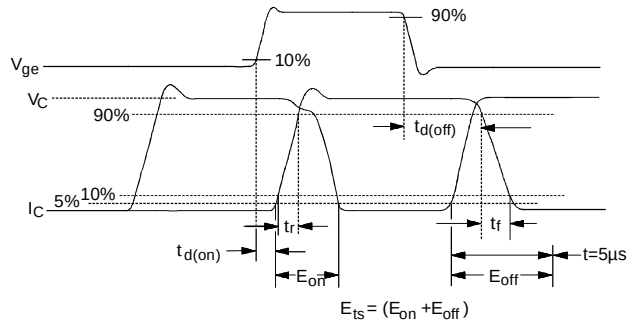


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

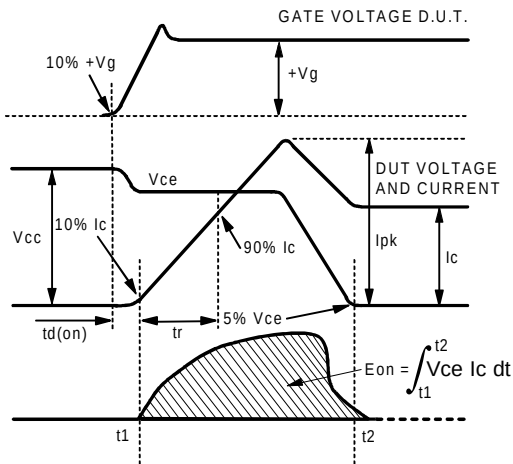


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

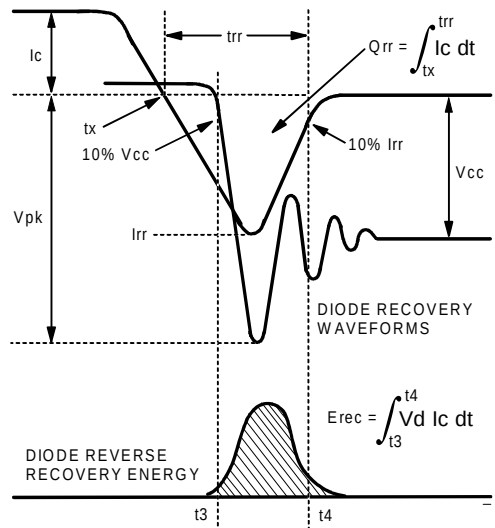


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

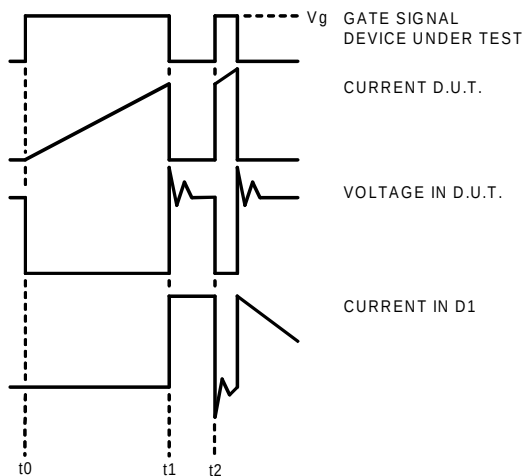


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

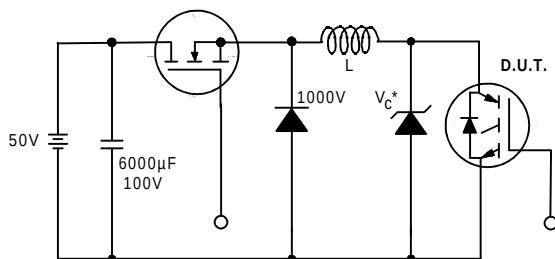


Figure 19. Clamped Inductive Load Test Circuit

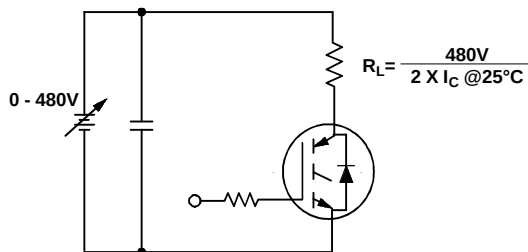
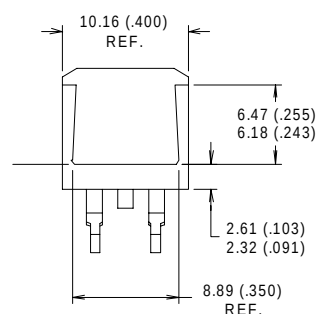
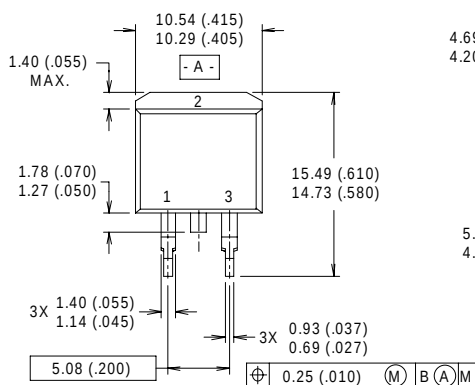


Figure 20. Pulsed Collector Current Test Circuit

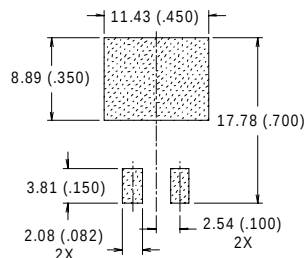
Notes:

- ① Repetitive rating: $V_{GE}=20V$; pulse width limited by maximum junction temperature (figure 20)
- ② $V_{CC}=80\%(V_{CES})$, $V_{GE}=20V$, $L=10\mu H$, $R_G = 50\Omega$ (figure 19)
- ③ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ④ Pulse width $5.0\mu s$, single shot.

D²Pak Package Outline



MINIMUM RECOMMENDED FOOTPRINT



NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

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