

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Seventh Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

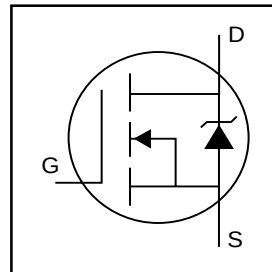
The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRL1404L) is available for low-profile applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	160 ^⑥	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	110 ^⑥	
I_{DM}	Pulsed Drain Current ^①	640	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^②	520	mJ
I_{AR}	Avalanche Current ^①	95	A
E_{AR}	Repetitive Avalanche Energy ^①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ^③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

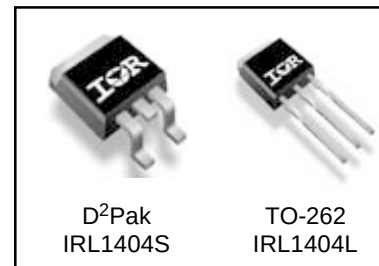
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted) ^⑦	—	40	



$$V_{DSS} = 40\text{V}$$

$$R_{DS(on)} = 0.004\Omega$$

$$I_D = 160\text{A}^{\text{⑥}}$$



D²Pak
IRL1404S

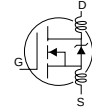
TO-262
IRL1404L

IRL1404S/IRL1404L

International
IR Rectifier

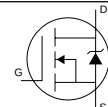
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.038	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.004	Ω	V _{GS} = 10V, I _D = 95A ④
				0.0059		V _{GS} = 4.3V, I _D = 40A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	93	—	—	S	V _{DS} = 25V, I _D = 95A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20 250	μA	V _{DS} = 40V, V _{GS} = 0V V _{DS} = 32V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage Gate-to-Source Reverse Leakage	—	—	200 -200	nA	V _{GS} = 20V V _{GS} = -20V
Q _g	Total Gate Charge	—	—	140	nC	I _D = 95A V _{DS} = 32V V _{GS} = 5.0V, See Fig. 6 ④
Q _{gs}	Gate-to-Source Charge	—	—	48		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	60		
t _{d(on)}	Turn-On Delay Time	—	18	—	ns	V _{DD} = 20V I _D = 95A R _G = 2.5Ω V _{GS} = 4.5V R _D = 0.25Ω ④
t _r	Rise Time	—	270	—		
t _{d(off)}	Turn-Off Delay Time	—	38	—		
t _f	Fall Time	—	130	—		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	6600	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1700	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	350	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	6700	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	1500	—		V _{GS} = 0V, V _{DS} = 32V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤	—	1500	—		V _{GS} = 0V, V _{DS} = 0V to 32V



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	160⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	640		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 95A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	63	94	ns	T _J = 25°C, I _F = 95A
Q _{rr}	Reverse Recovery Charge	—	170	250	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				



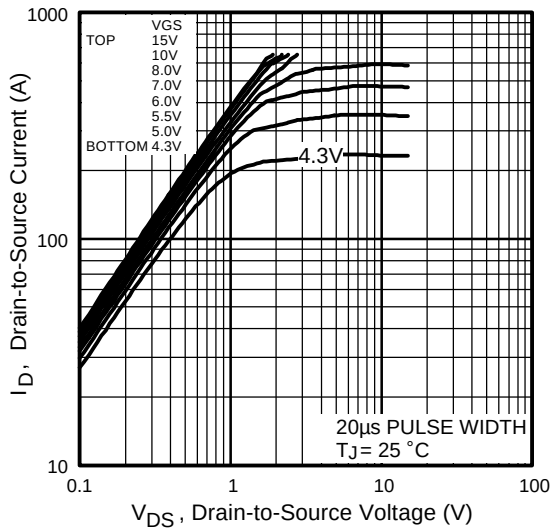


Fig 1. Typical Output Characteristics

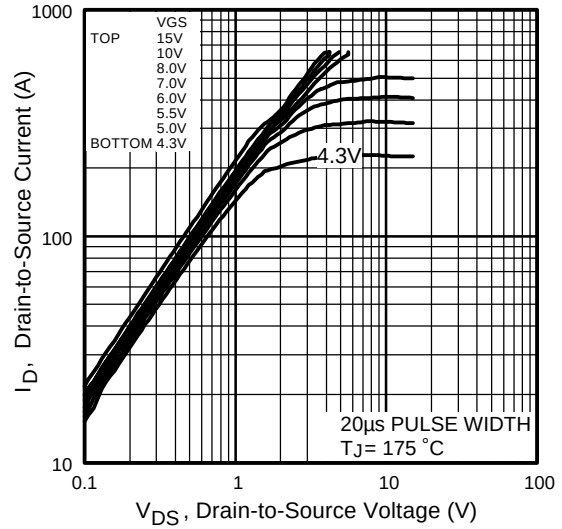


Fig 2. Typical Output Characteristics

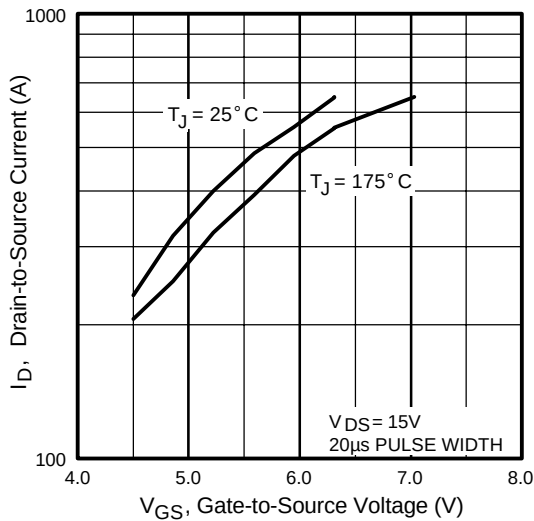


Fig 3. Typical Transfer Characteristics

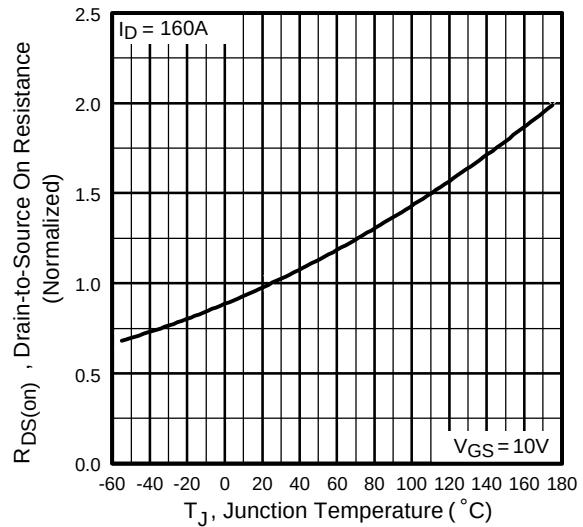


Fig 4. Normalized On-Resistance Vs. Temperature

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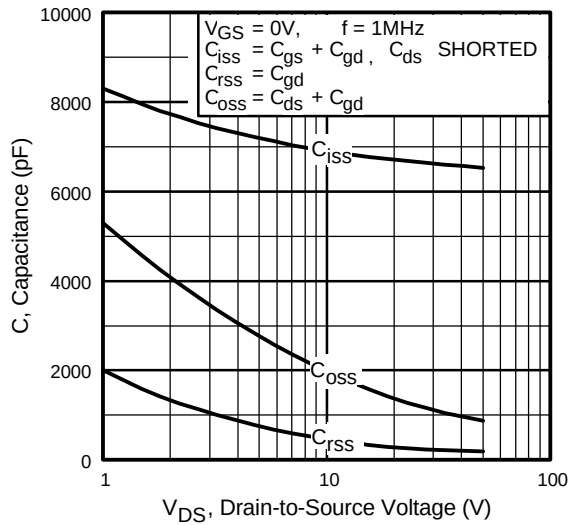


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

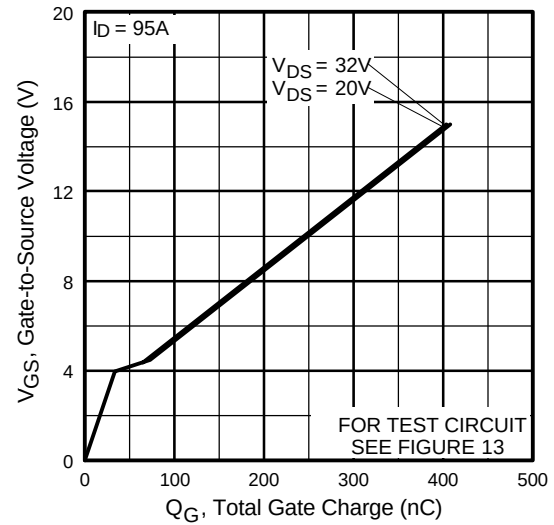


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

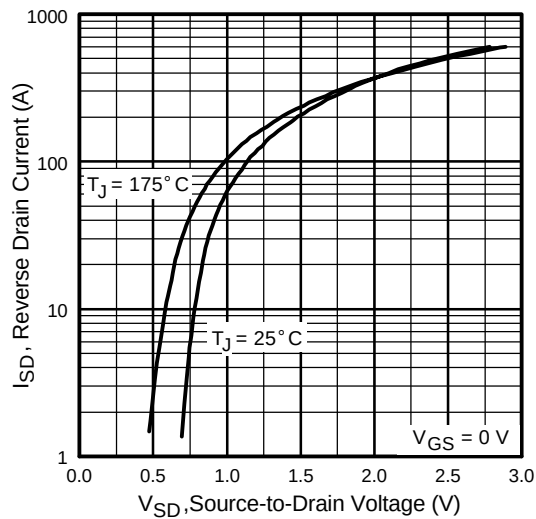


Fig 7. Typical Source-Drain Diode Forward Voltage

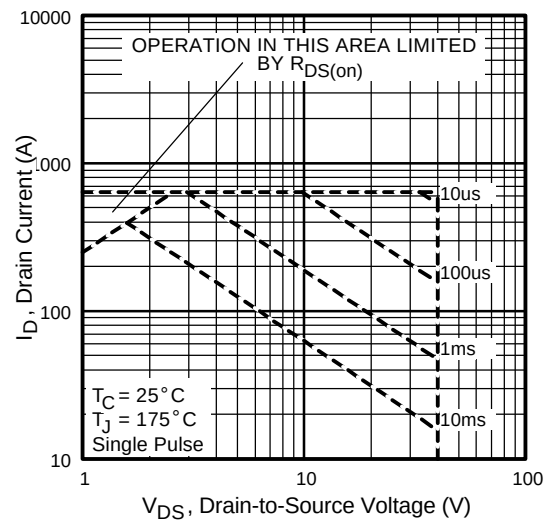


Fig 8. Maximum Safe Operating Area

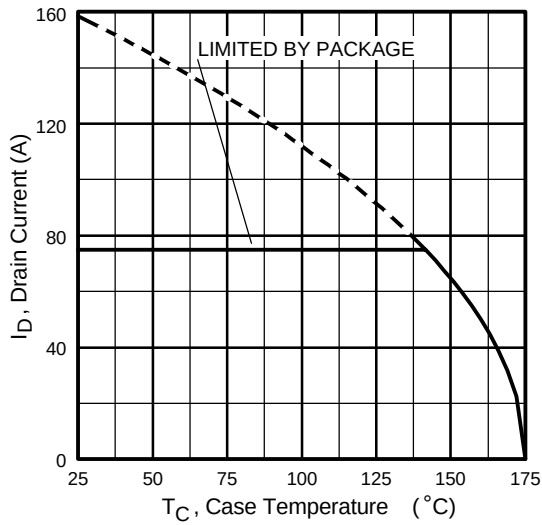


Fig 9. Maximum Drain Current Vs. Case Temperature

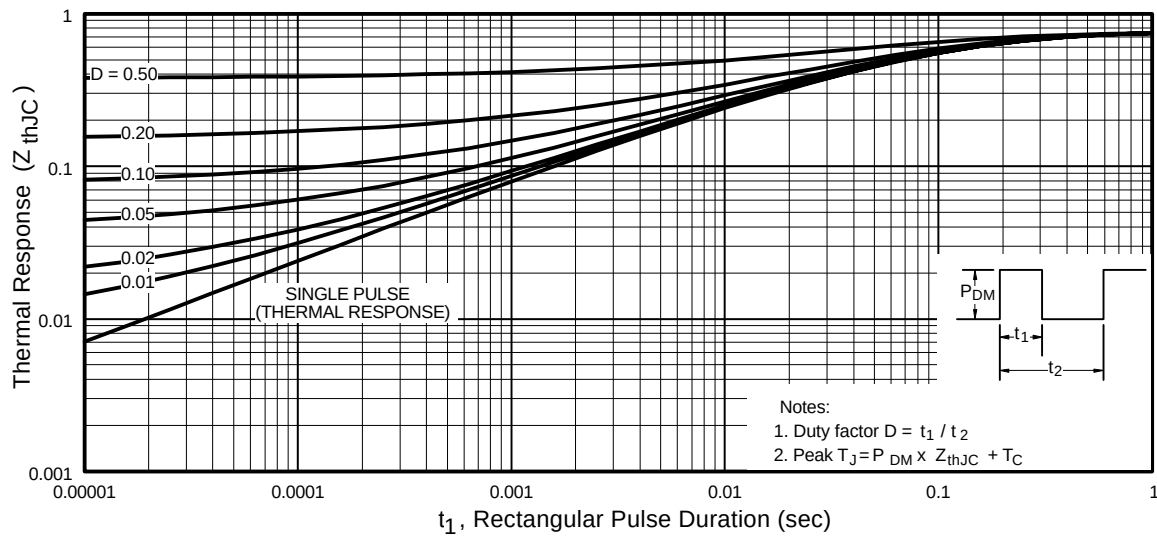
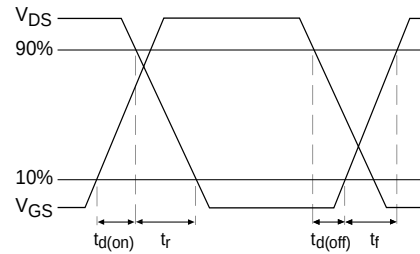
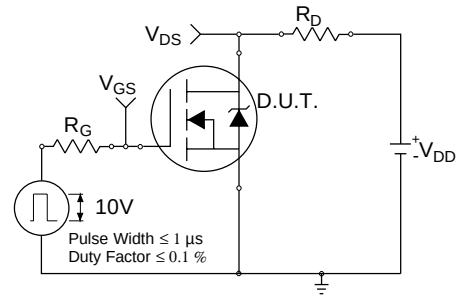


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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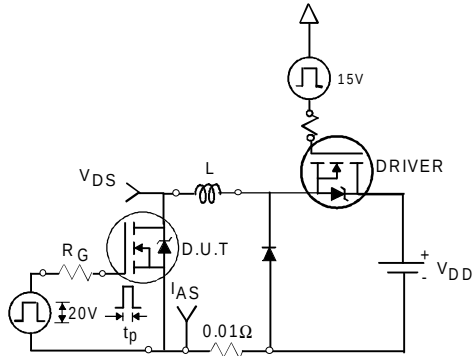


Fig 12a. Unclamped Inductive Test Circuit

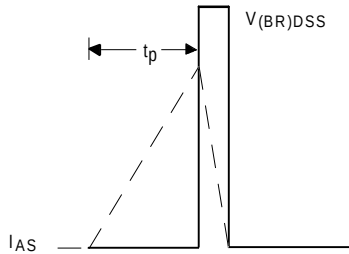


Fig 12b. Unclamped Inductive Waveforms

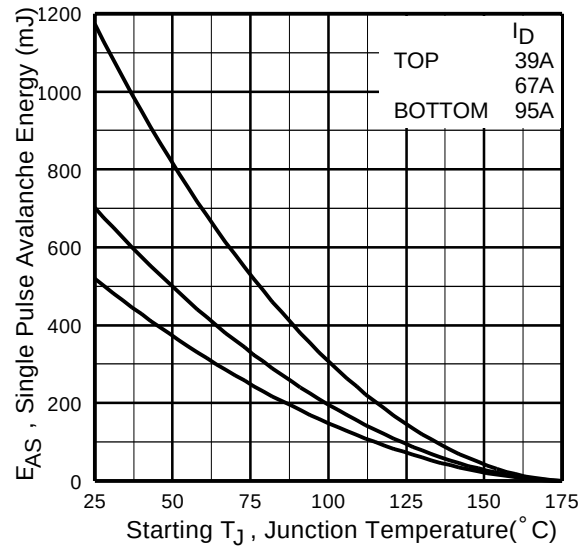


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

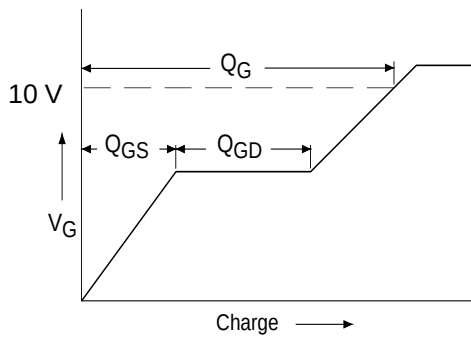


Fig 13a. Basic Gate Charge Waveform

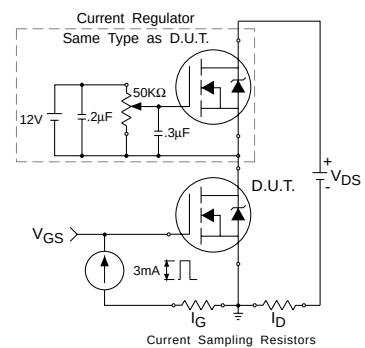
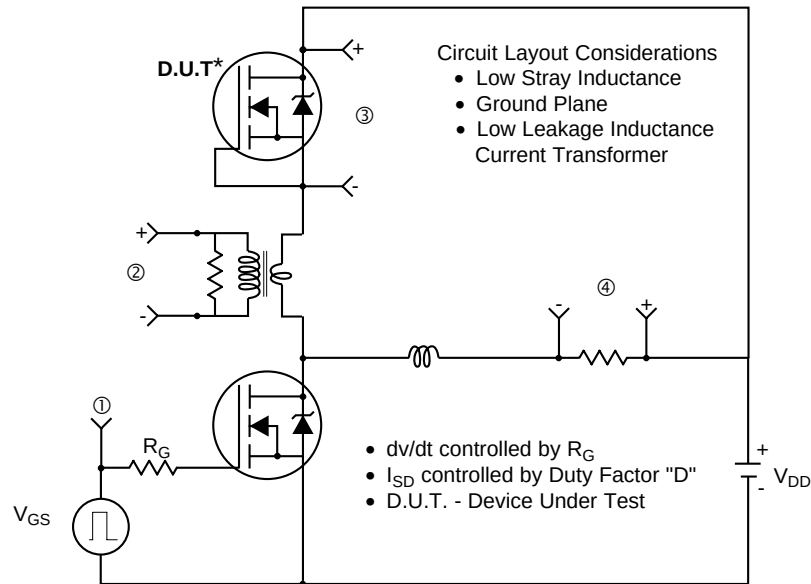
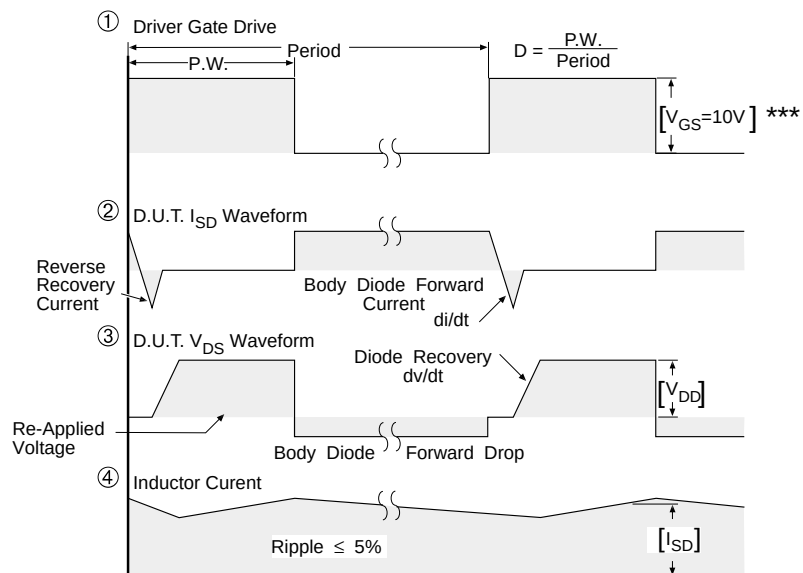


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

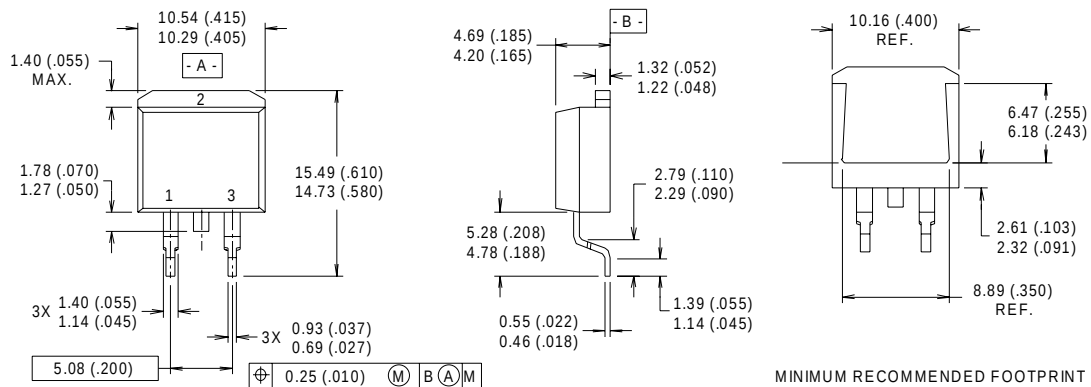
Fig 14. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



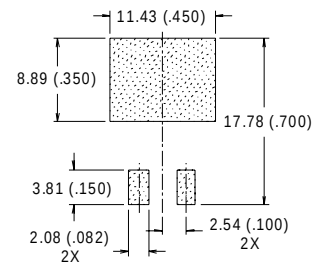
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

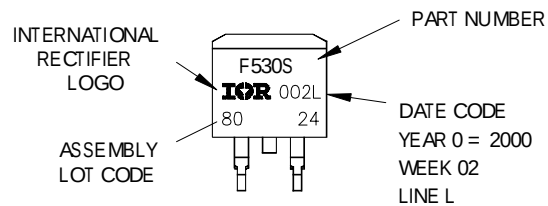
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



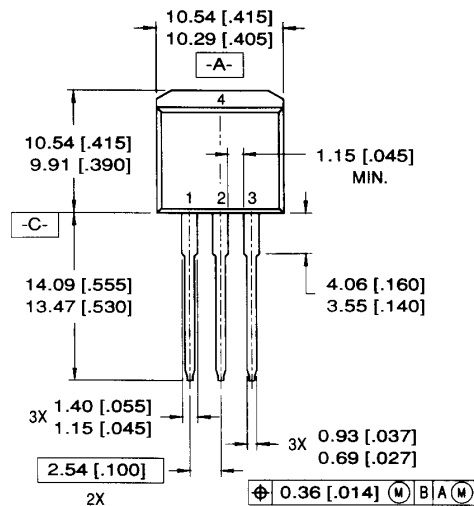
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"



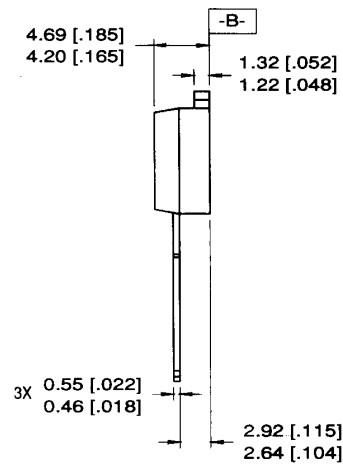
TO-262 Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

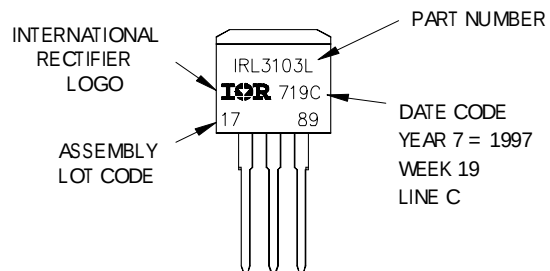


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON VW 19, 1997
IN THE ASSEMBLY LINE "C"

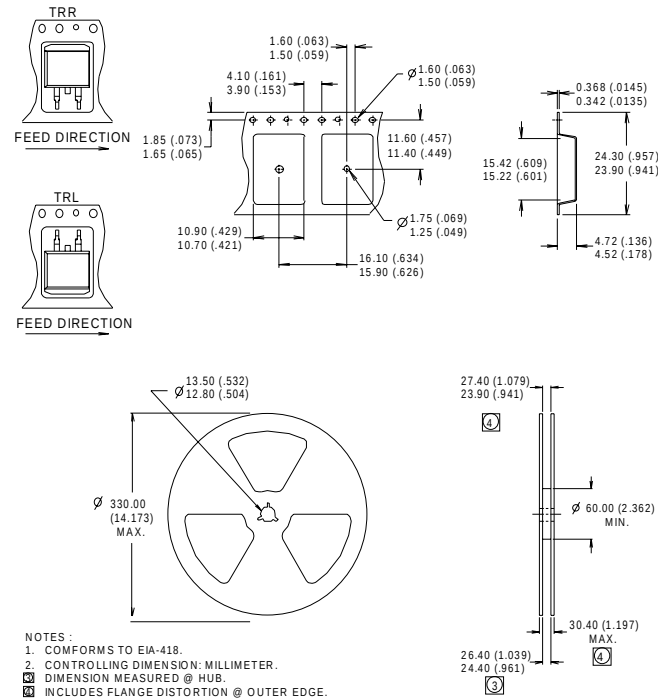


IRL1404S/IRL1404L

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D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.35\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 95\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 95\text{A}$, $di/dt \leq 160\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time
as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4.
- ⑦ This is applied to D²Pak, When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.

This product has been designed and qualified for the Industrial market.

Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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