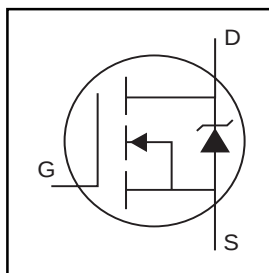


- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching



$$V_{DSS} = 20V$$

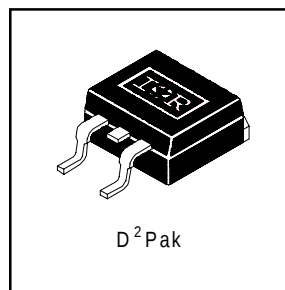
$$R_{DS(on)} = 0.013\Omega$$

$$I_D = 61A$$

Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 4.5V⑤	61	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 4.5V⑤	39	
I_{DM}	Pulsed Drain Current ①⑤	240	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	89	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy②⑤	220	mJ
I_{AR}	Avalanche Current①	35	A
E_{AR}	Repetitive Avalanche Energy①	8.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{JC}	Junction-to-Case	—	1.4	°C/W
R_{JA}	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V _{GS} = 0V, I _D = 250μA
DV _{(BR)DSS/DT_J}	Breakdown Voltage Temp. Coefficient	—	0.016	—	V/°C	Reference to 25°C, I _D = 1mA⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.015	W	V _{GS} = 4.5V, I _D = 37A ④
		—	—	0.013		V _{GS} = 7.0V, I _D = 37A ④
V _{GS(th)}	Gate Threshold Voltage	0.70	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	36	—	—	S	V _{DS} = 16V, I _D = 35A⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 20V, V _{GS} = 0V
		—	—	250		V _{DS} = 10V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 10V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -10V
Q _g	Total Gate Charge	—	—	58	nC	I _D = 35A
Q _{gs}	Gate-to-Source Charge	—	—	14		V _{DS} = 16V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	21		V _{GS} = 4.5V, See Fig. 6 ④⑤
t _{d(on)}	Turn-On Delay Time	—	10	—	ns	V _{DD} = 10V
t _r	Rise Time	—	130	—		I _D = 35A
t _{d(off)}	Turn-Off Delay Time	—	80	—		R _G = 9.0Ω, V _{GS} = 4.5V
t _f	Fall Time	—	110	—		R _D = 0.28Ω ④⑤
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	2500	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1000	—		V _{DS} = 15V
C _{rss}	Reverse Transfer Capacitance	—	360	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	61	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	240		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 37A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	59	88	ns	T _J = 25°C, I _F = 35A
Q _{rr}	Reverse Recovery Charge	—	110	160	nC	di/dt = 100A/μs ④⑤
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.36mH
R_G = 25Ω, I_{AS} = 35A.

③ I_{SD} ≤ 35A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 150°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRL3102 data and test conditions

** When mounted on FR-4 board using minimum recommended footprint.

For recommended footprint and soldering techniques refer to application note #AN-994.

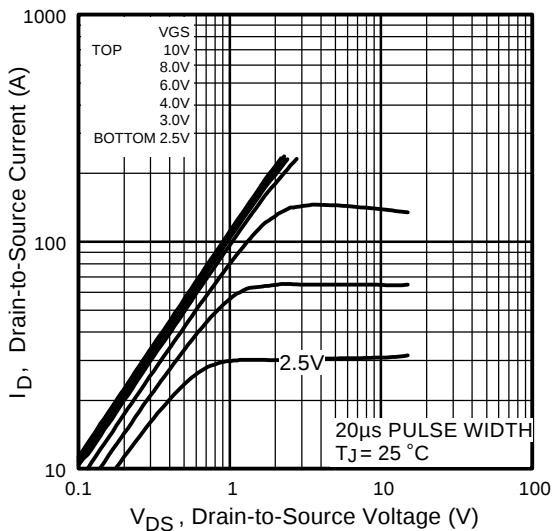


Fig 1. Typical Output Characteristics

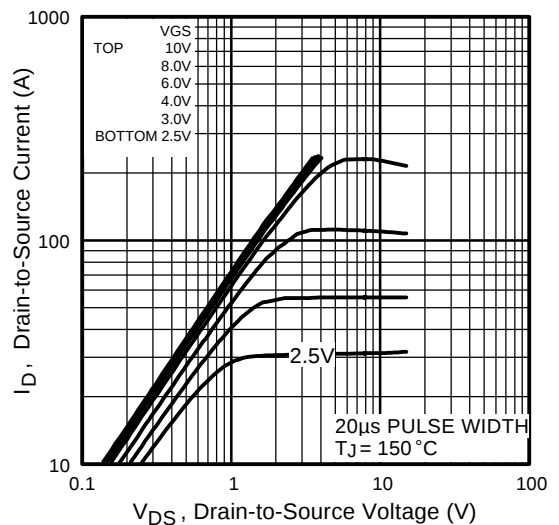


Fig 2. Typical Output Characteristics

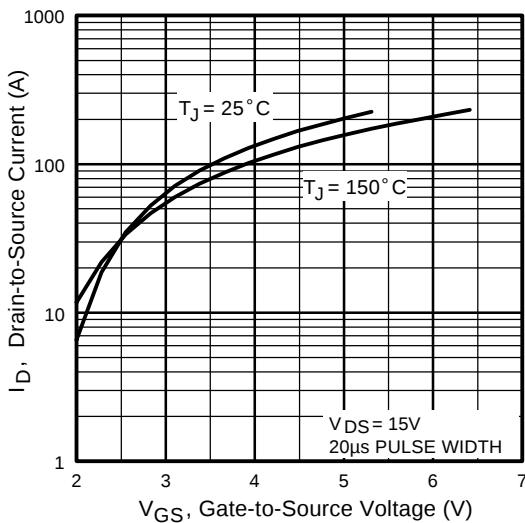


Fig 3. Typical Transfer Characteristics

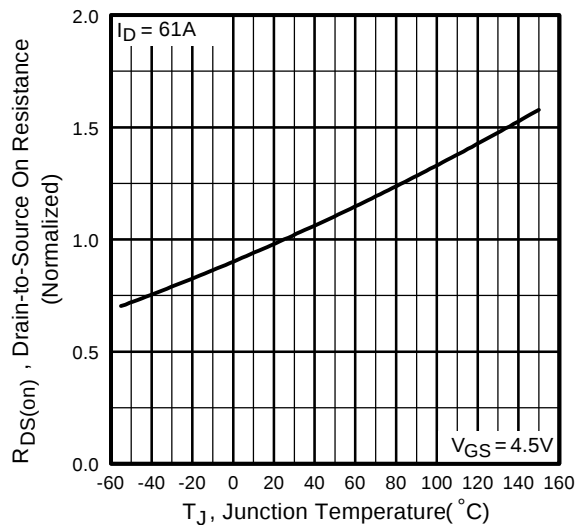


Fig 4. Normalized On-Resistance Vs. Temperature

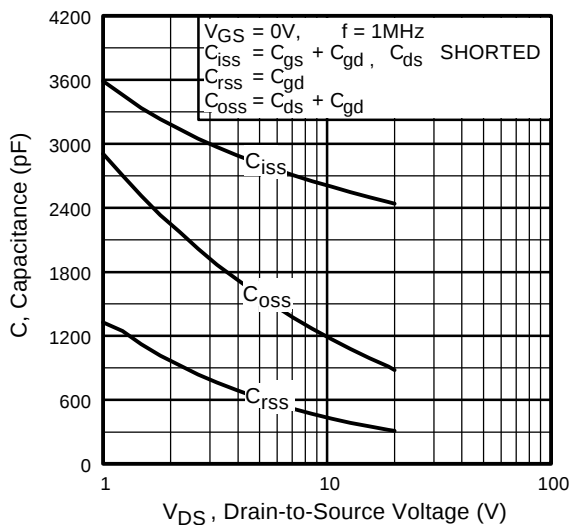


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

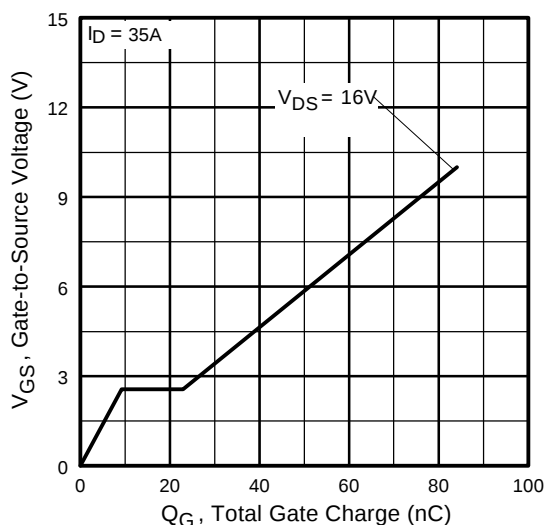


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

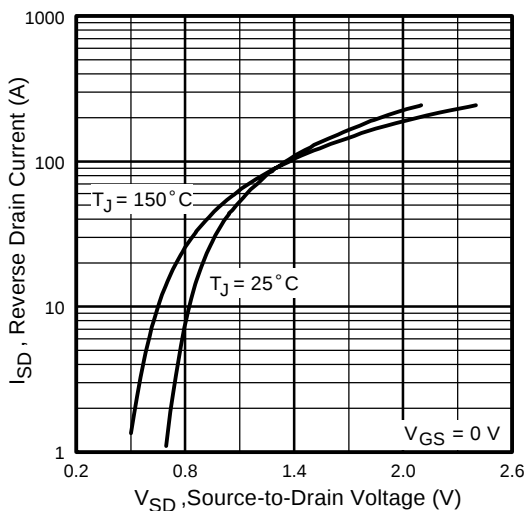


Fig 7. Typical Source-Drain Diode Forward Voltage

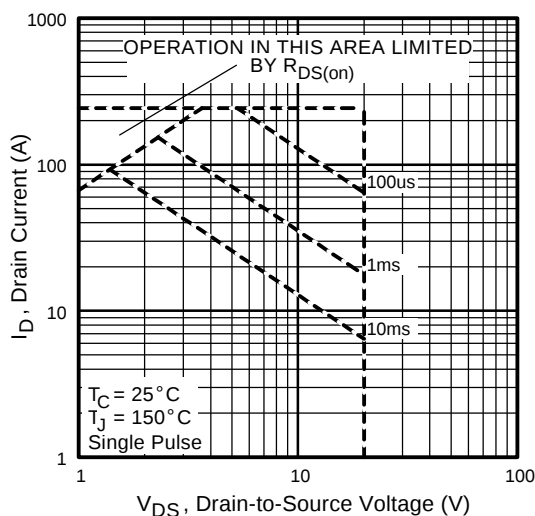


Fig 8. Maximum Safe Operating Area

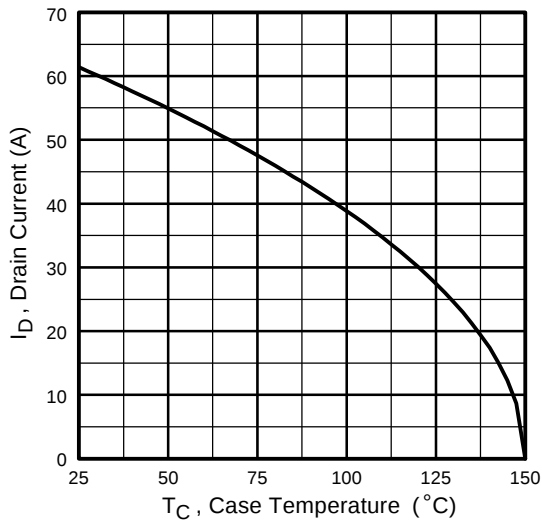


Fig 9. Maximum Drain Current Vs. Case Temperature

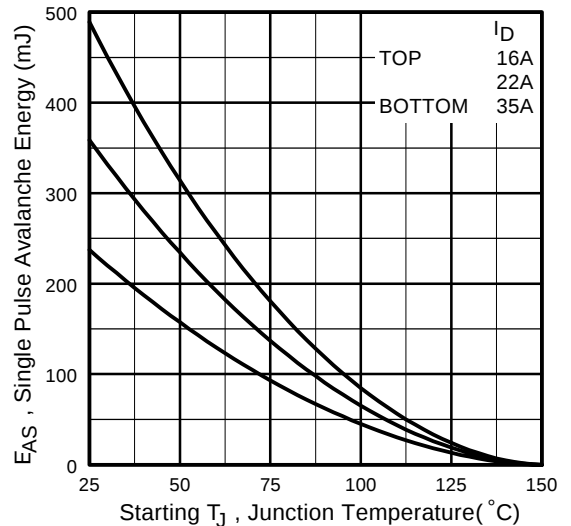


Fig 10. Maximum Avalanche Energy Vs. Drain Current

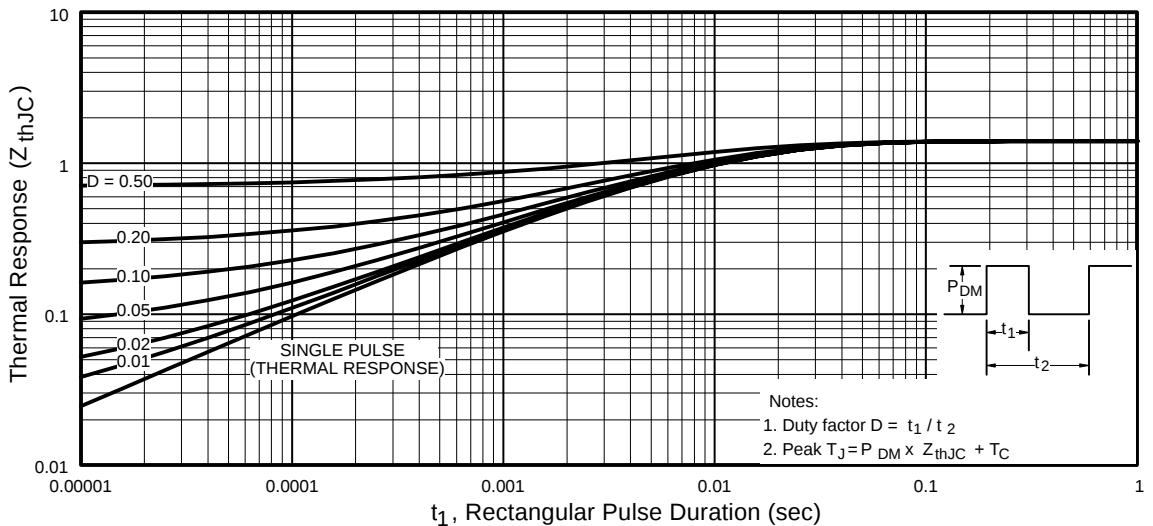


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

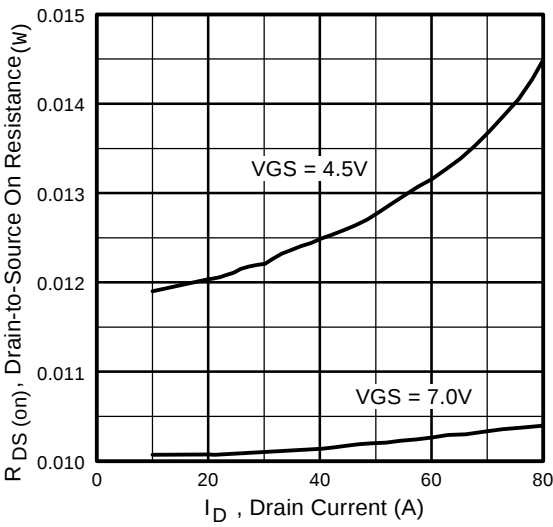


Fig 12. On-Resistance Vs. Drain Current

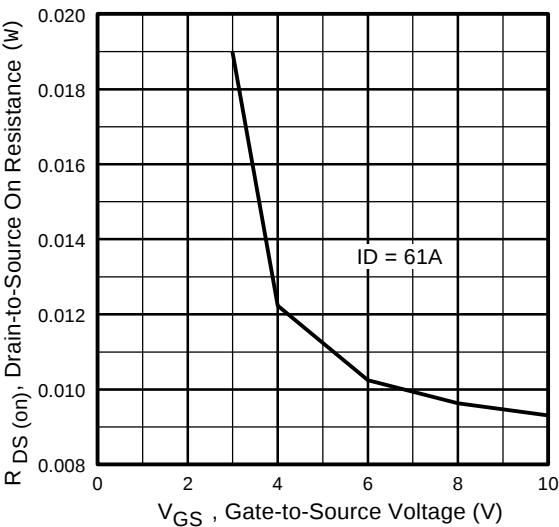
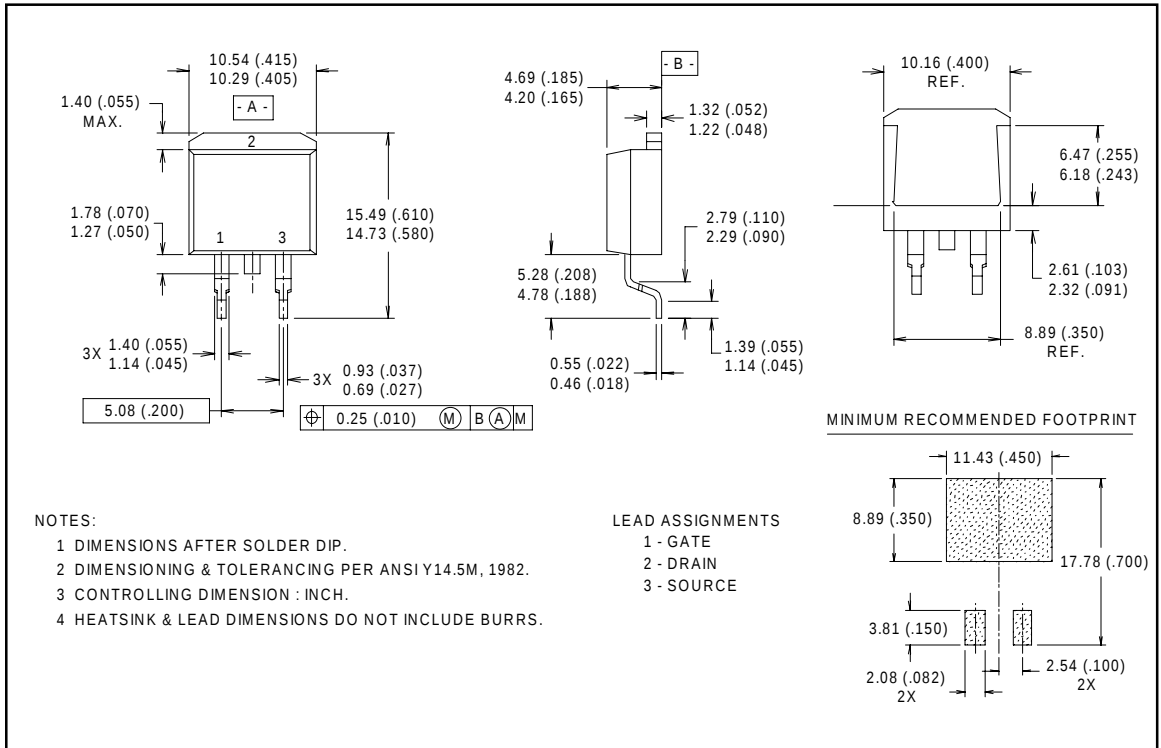


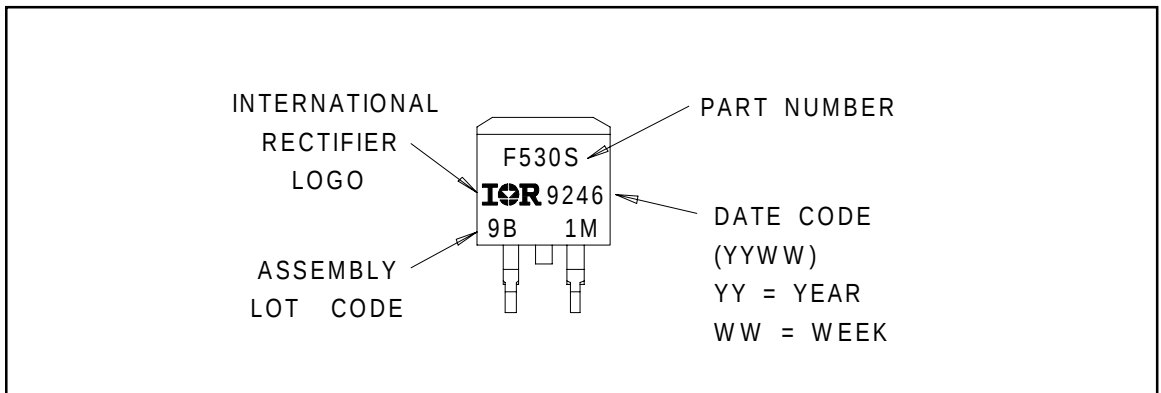
Fig 13. On-Resistance Vs. Gate Voltage

D²Pak Package Outline



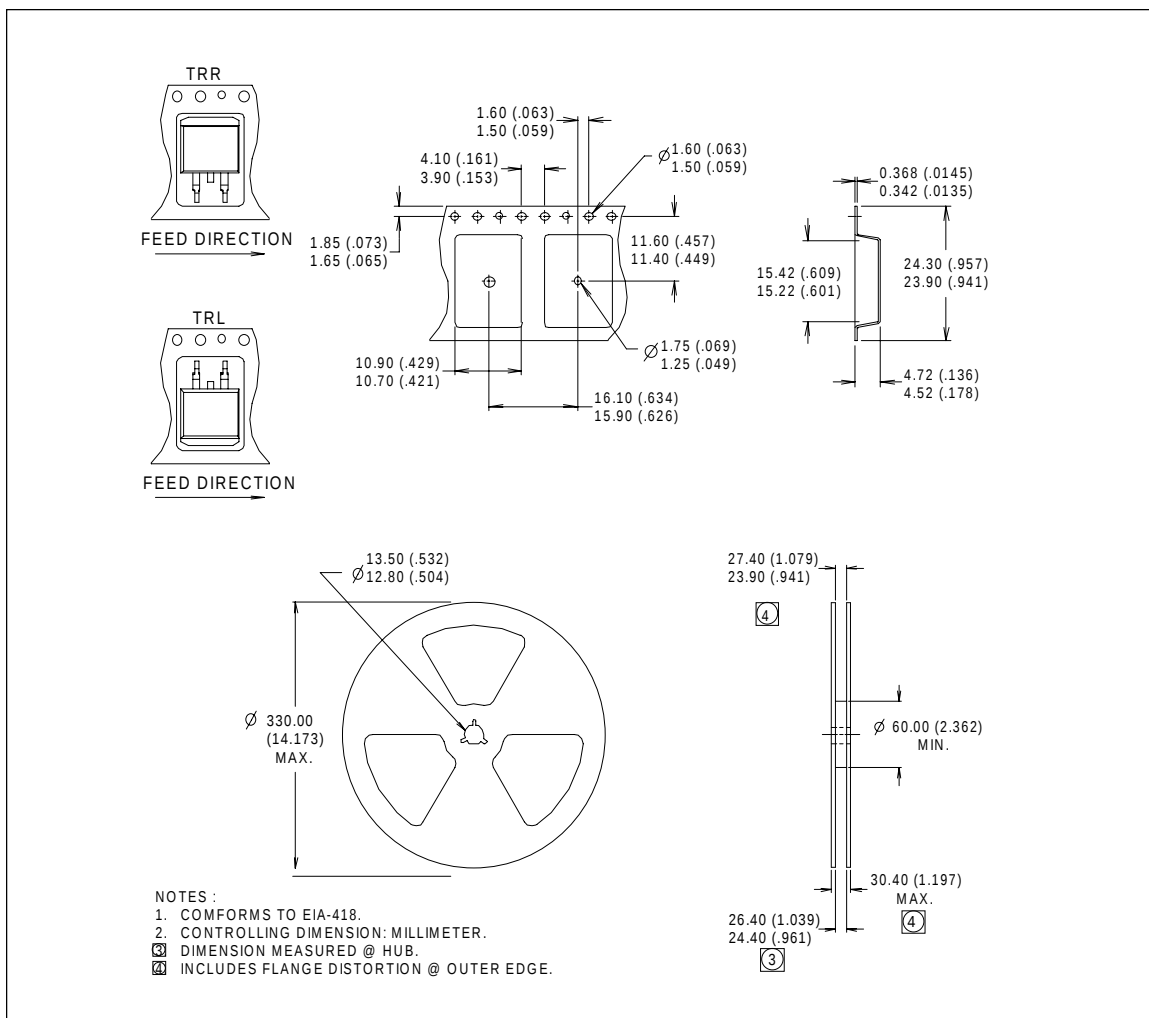
Part Marking Information

D²Pak



Tape & Reel Information

D²Pak



International
IR Rectifier

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