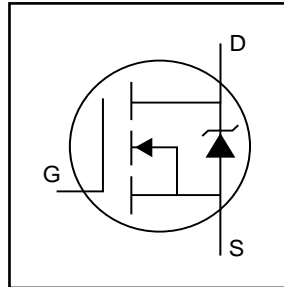


- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated

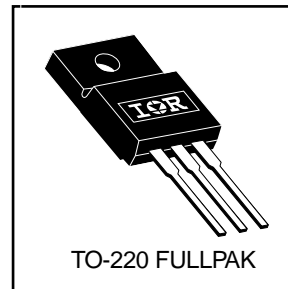


| |
|----------------------------|
| $V_{DSS} = 55V$ |
| $R_{DS(on)} = 0.008\Omega$ |
| $I_D = 58A$ |

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

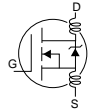
| | Parameter | Max. | Units |
|---------------------------|---|-----------------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 58 | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 41 | |
| I_{DM} | Pulsed Drain Current ①⑥ | 360 | |
| $P_D @ T_C = 25^\circ C$ | Power Dissipation | 63 | W |
| | Linear Derating Factor | 0.42 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 16 | V |
| E_{AS} | Single Pulse Avalanche Energy ②⑥ | 500 | mJ |
| I_{AR} | Avalanche Current ①⑥ | 54 | A |
| E_{AR} | Repetitive Avalanche Current ① | 6.3 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③⑥ | 5.0 | V/ns |
| T_J T_{STG} | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 screw. | 10 lbf•in (1.1N•m) | |

Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|-----------------|---------------------|------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 2.4 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | — | — | 65 | |

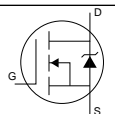
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|-------|-------|---------------------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 55 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.035 | — | V/ $^\circ\text{C}$ | Reference to 25°C , $I_D = 1\text{mA}$ Ⓒ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.008 | Ω | $V_{GS} = 10V, I_D = 31A$ ④ |
| | | — | — | 0.010 | | $V_{GS} = 5.0V, I_D = 31A$ ④ |
| | | — | — | 0.013 | | $V_{GS} = 4.0V, I_D = 26A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 2.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 59 | — | — | S | $V_{DS} = 25V, I_D = 54A$ ⑥ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 55V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 16V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -16V$ |
| Q_g | Total Gate Charge | — | — | 130 | nC | $I_D = 54A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 25 | | $V_{DS} = 44V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 67 | | $V_{GS} = 5.0V$, See Fig. 6 and 13 ④Ⓒ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 12 | — | ns | $V_{DD} = 28V$ |
| t_r | Rise Time | — | 160 | — | | $I_D = 54A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 43 | — | | $R_G = 1.3\Omega, V_{GS} = 5.0V$ |
| t_f | Fall Time | — | 84 | — | | $R_D = 0.50\Omega$, See Fig. 10 ④Ⓒ |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 7.5 | — | | |
| C_{iss} | Input Capacitance | — | 5000 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 1100 | — | | $V_{DS} = 25V$ |
| C_{riss} | Reverse Transfer Capacitance | — | 390 | — | | $f = 1.0\text{MHz}$, See Fig. 5Ⓒ |
| C | Drain to Sink Capacitance | — | 12 | — | | $f = 1.0\text{MHz}$ |



Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|---|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 58 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 360 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 31A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 140 | 210 | ns | $T_J = 25^\circ\text{C}, I_F = 54A$ |
| Q_{rr} | Reverse Recovery Charge | — | 650 | 970 | nC | $di/dt = 100A/\mu s$ ④ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D) | | | | |



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 240\mu H$
 $R_G = 25\Omega, I_{AS} = 54A$. (See Figure 12)
- ③ $I_{SD} \leq 54A, di/dt \leq 230A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $t = 60s, f = 60\text{Hz}$
- ⑥ Use IRL2505 data and test conditions

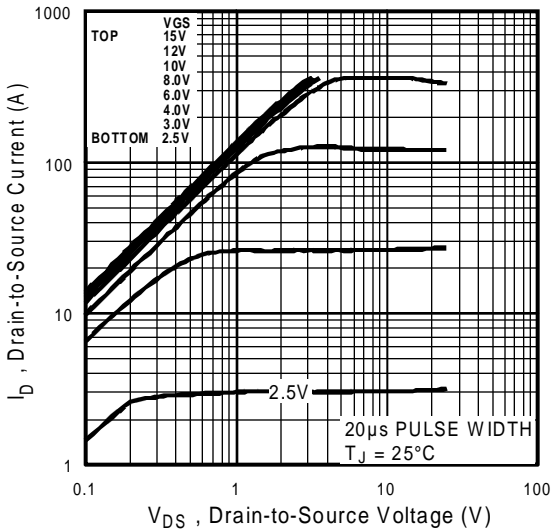


Fig 1. Typical Output Characteristics

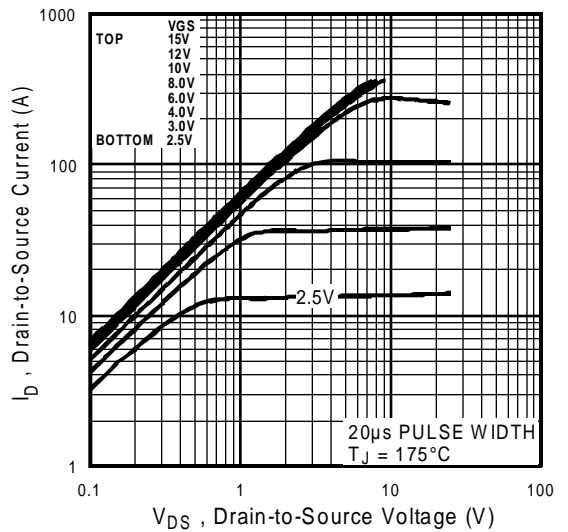


Fig 2. Typical Output Characteristics

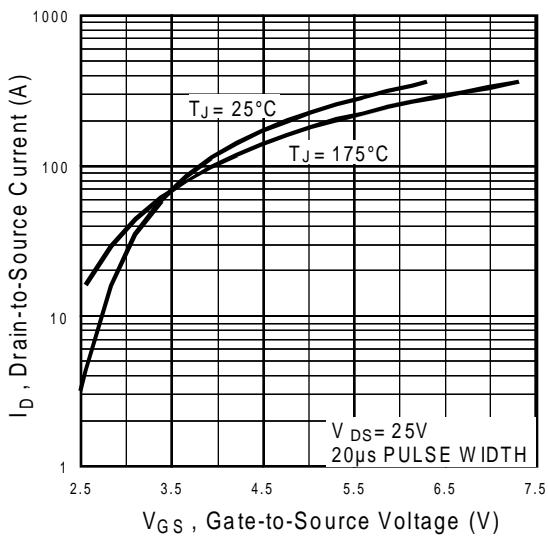


Fig 3. Typical Transfer Characteristics

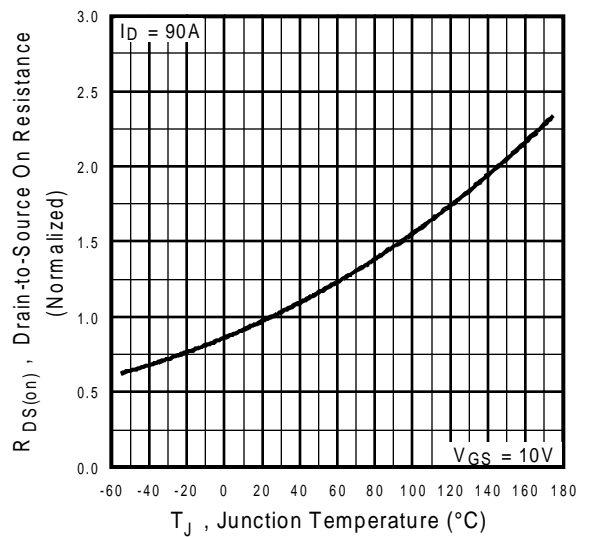


Fig 4. Normalized On-Resistance Vs. Temperature

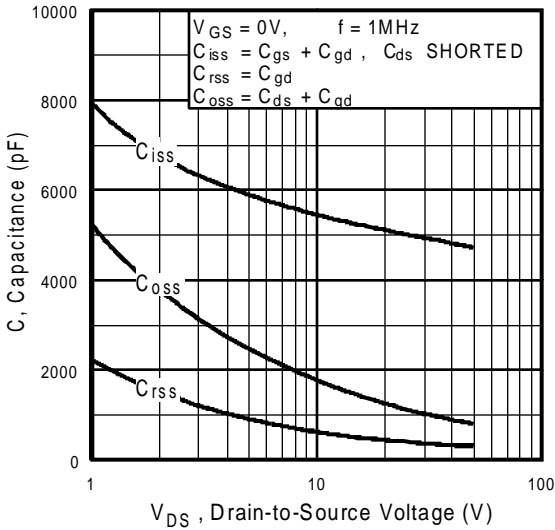


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

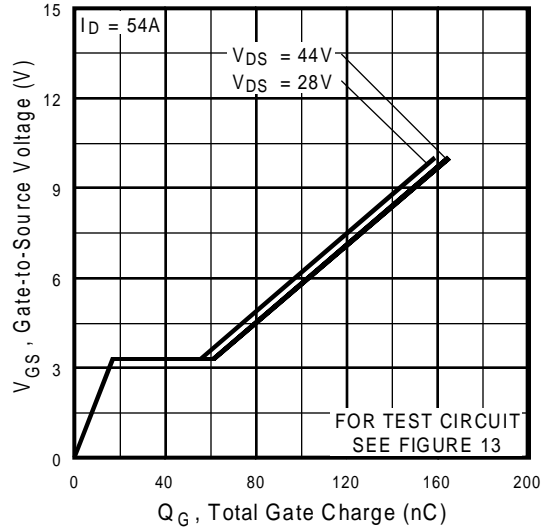


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

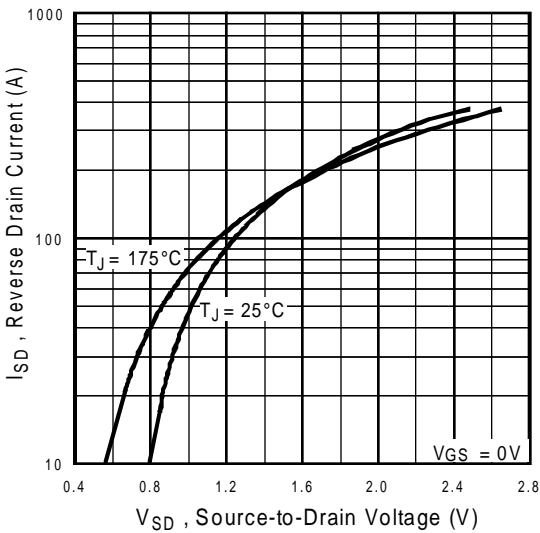


Fig 7. Typical Source-Drain Diode Forward Voltage

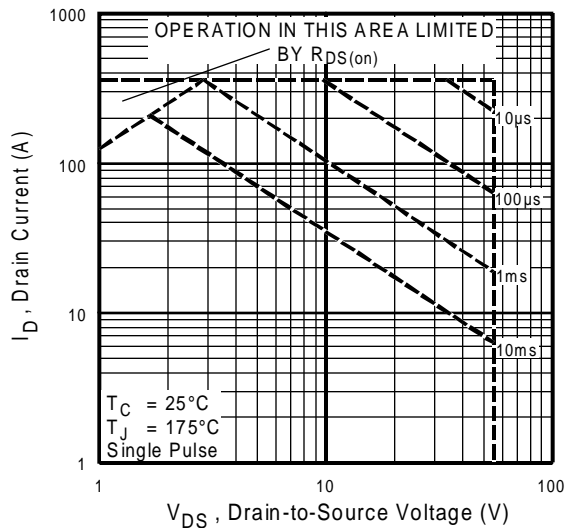


Fig 8. Maximum Safe Operating Area

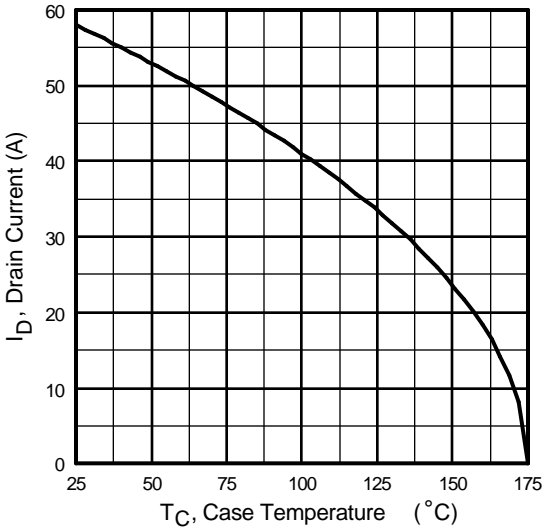


Fig 9. Maximum Drain Current Vs. Case Temperature

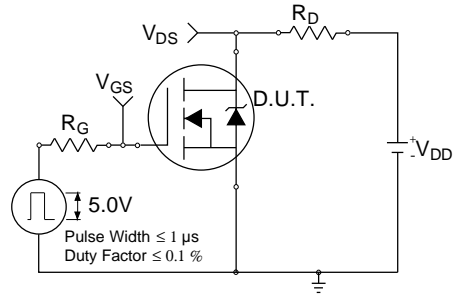


Fig 10a. Switching Time Test Circuit

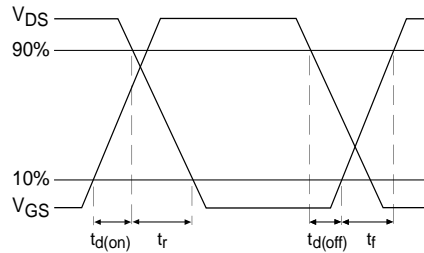


Fig 10b. Switching Time Waveforms

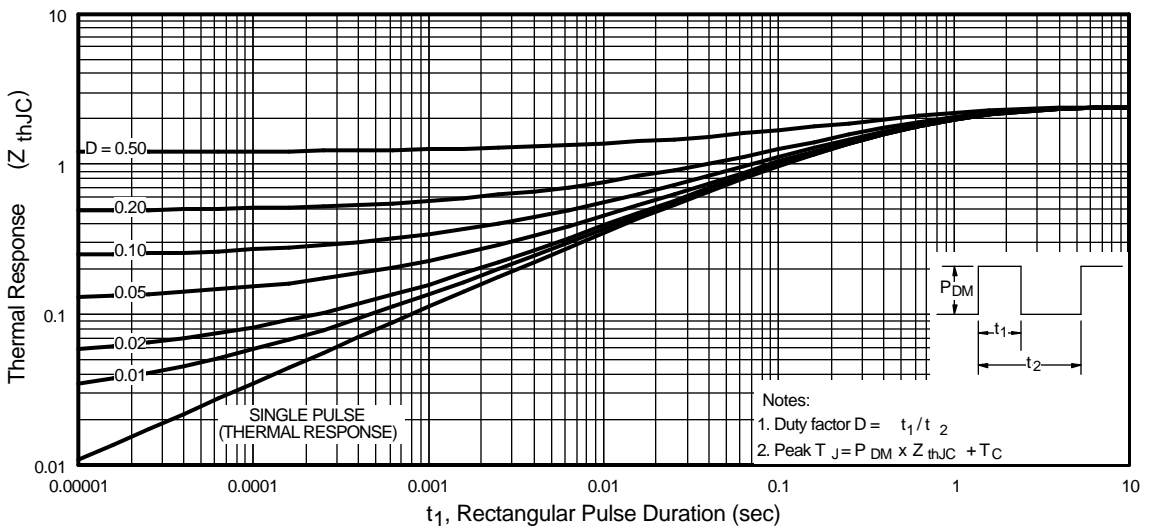


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

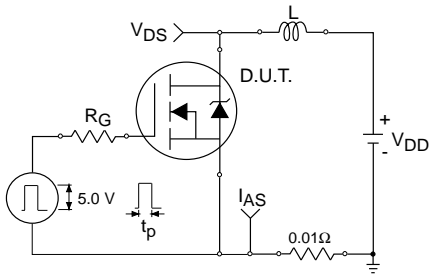


Fig 12a. Unclamped Inductive Test Circuit

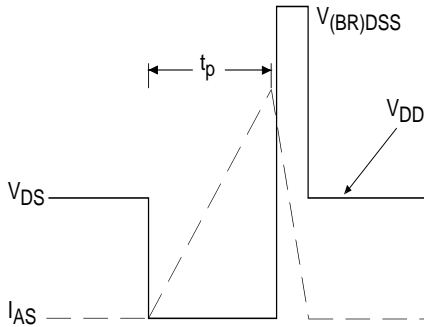


Fig 12b. Unclamped Inductive Waveforms

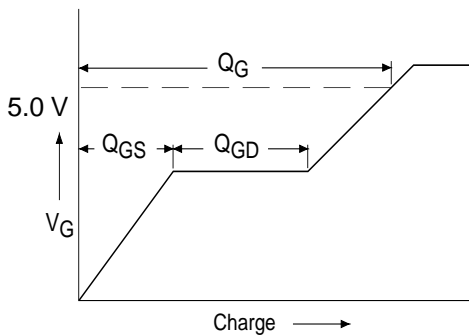


Fig 13a. Basic Gate Charge Waveform

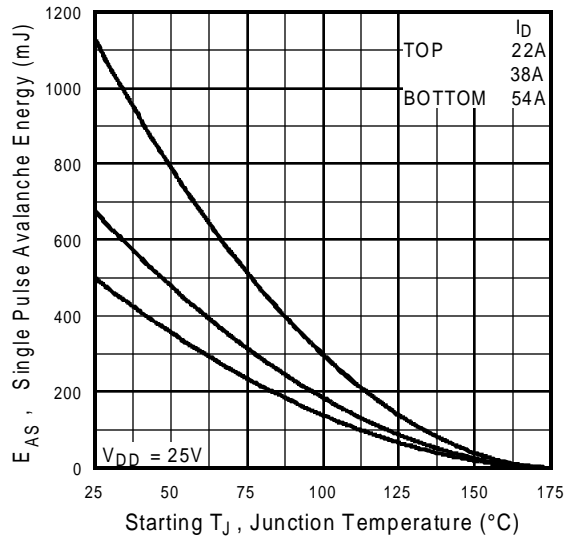


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

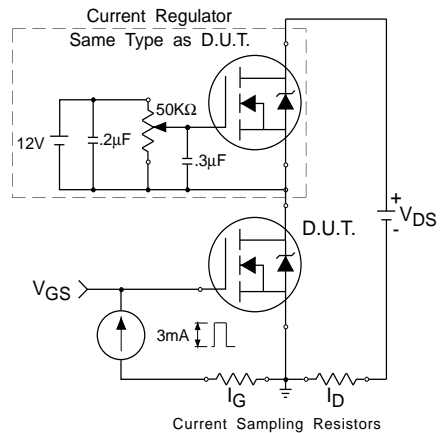
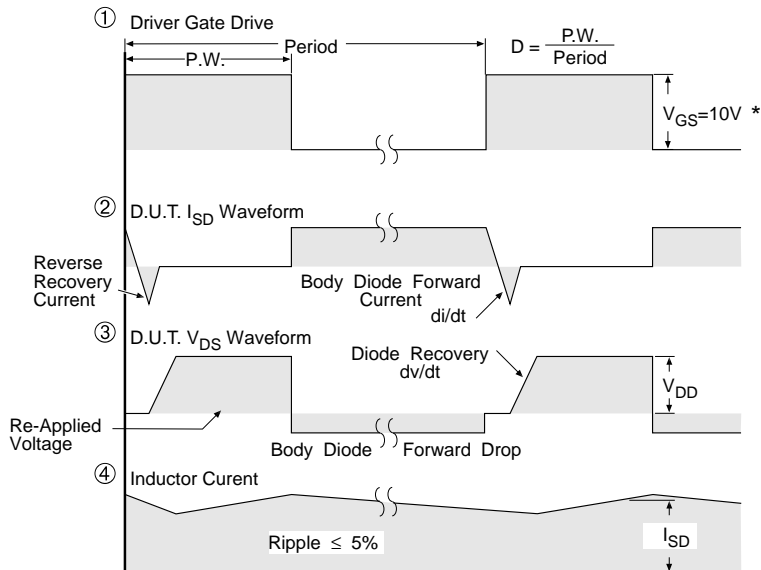
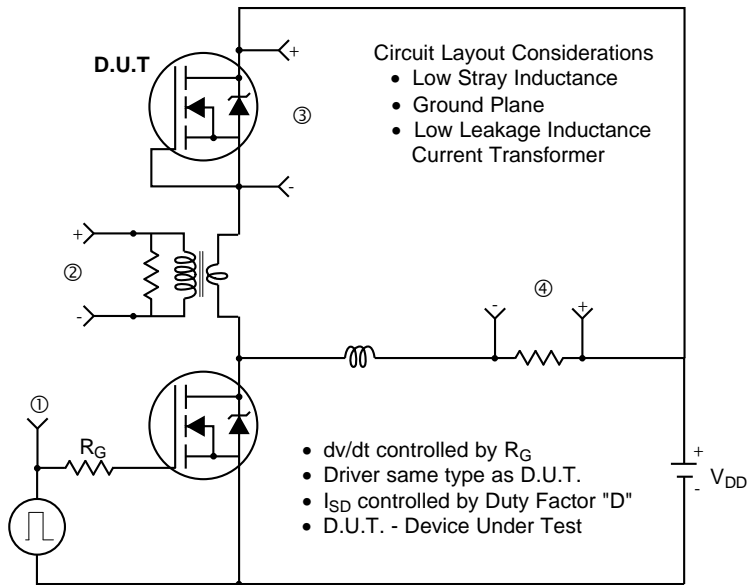


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



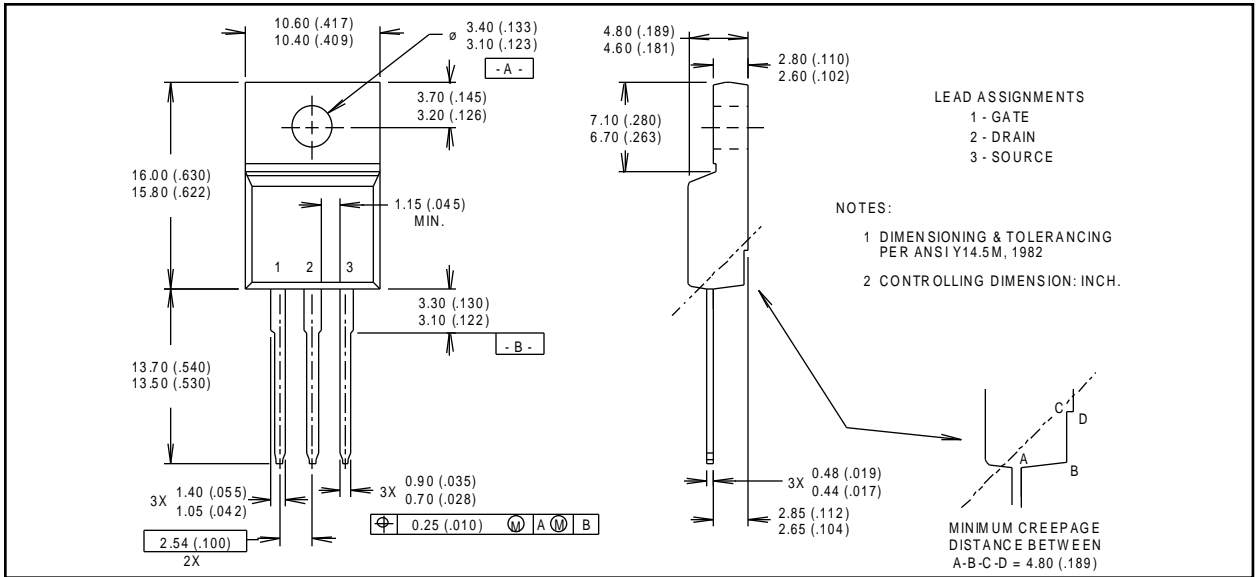
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220 FullPak Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

TO-220 FullPak

EXAMPLE : THIS IS AN IRFI840G
 WITH ASSEMBLY
 LOT CODE E401

