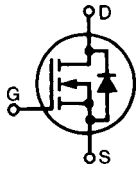
IXYS

HiPerFET™ Power MOSFET

IXFH 22N55

V_{DSS} = 550 V
$I_{D (cont)}$ = 22 A
$R_{DS(on)}$ = 0.27 Ω
t_{rr} ≤ 250 ns

N-Channel Enhancement Mode
Avlanche Rated, High dv/dt, Low t_{rr}

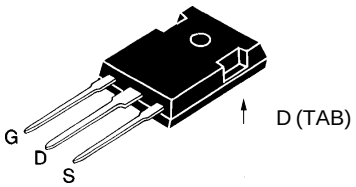


Preliminary data

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	550	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	550	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	22	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	88	A
I_{AR}	T_C = 25°C	22	A
E_{AR}	T_C = 25°C	30	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 2 Ω	5	V/ns
P_D	T_C = 25°C	300	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.063 in) from case for 10 s	300	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		6	g

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA	550			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	2		4.5	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$, V_{GS} = 0 V; T_J = 25°C			250	μA
	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \cdot I_{D25}$, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			0.27	Ω

TO-247 AD



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard packages JEDEC TO-247 AD
- Low $R_{DS (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance (< 5 nH) - easy to drive and to protect
- Fast intrinsic Rectifier

Applications

- Power Factor Control Circuits
- Uninterruptible Power Supplies (UPS)
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls
- Low voltage relays

Advantages

- Easy to mount with 1 screw (isolated mounting screw hole)
- Space savings
- High power density

IXYS reserves the right to change limits, test conditions, and dimensions.

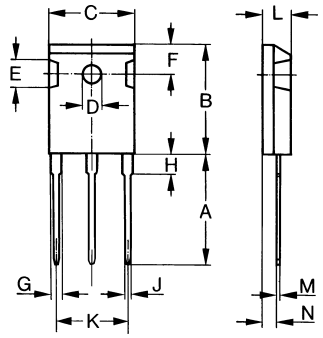
94527A (10/95)

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 I_{D25}, pulse test	11	18		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4200		pF
C_{oss}			450		pF
C_{rss}			135		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}, R_G = 2 Ω (External)		20	40	ns
t_r			43	60	ns
$t_{d(off)}$			70	90	ns
t_f			40	60	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		150	170	nC
Q_{gs}			29	40	nC
Q_{gd}			60	85	nC
R_{thJC}				0.42	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V			22	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			88	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle δ ≤ 2 %			1.5	V
t_{rr}	$I_F = I_S$, -di/dt = 100 A/μs, V_R = 100 V			250	ns
	T_J = 125°C			400	ns

TO-247 AD Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	19.81	20.32	0.780	0.800
B	20.80	21.46	0.819	0.845
C	15.75	16.26	0.610	0.640
D	3.55	3.65	0.140	0.144
E	4.32	5.49	0.170	0.216
F	5.4	6.2	0.212	0.244
G	1.65	2.13	0.065	0.084
H	-	4.5	-	0.177
J	1.0	1.4	0.040	0.055
K	10.8	11.0	0.426	0.433
L	4.7	5.3	0.185	0.209
M	0.4	0.8	0.016	0.031
N	1.5	2.49	0.087	0.102

Fig. 1 Output Characteristics

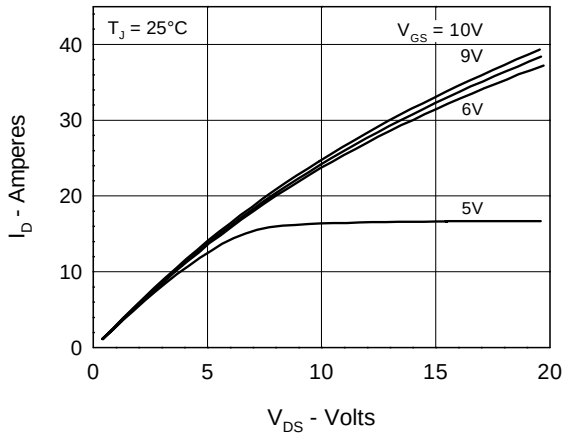


Fig. 2 Input Admittance

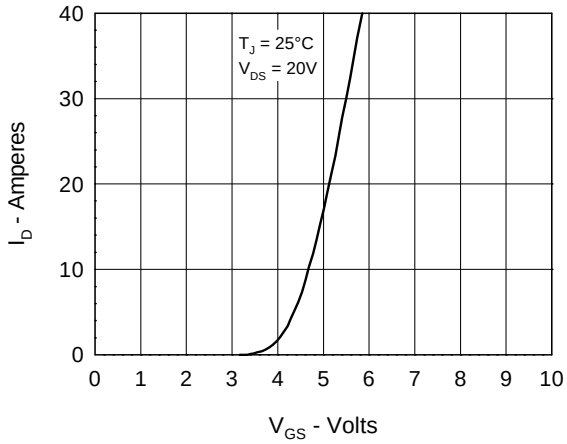


Fig. 3 $R_{DS(on)}$ vs. Drain Current

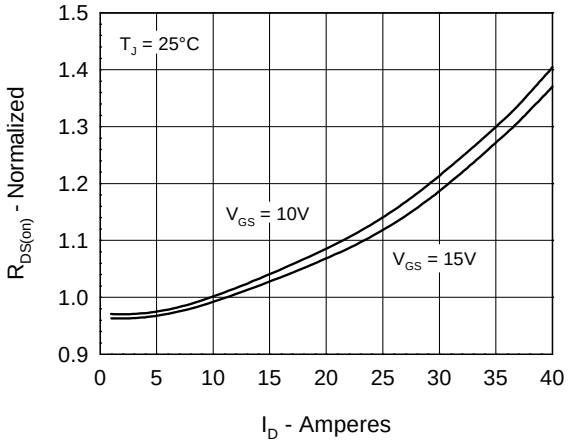


Fig. 4 Temperature Dependence of Drain to Source Resistance

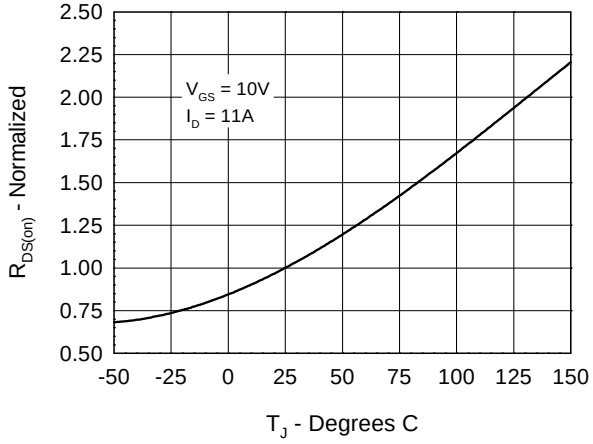


Fig. 5 Drain Current vs. Case Temperature

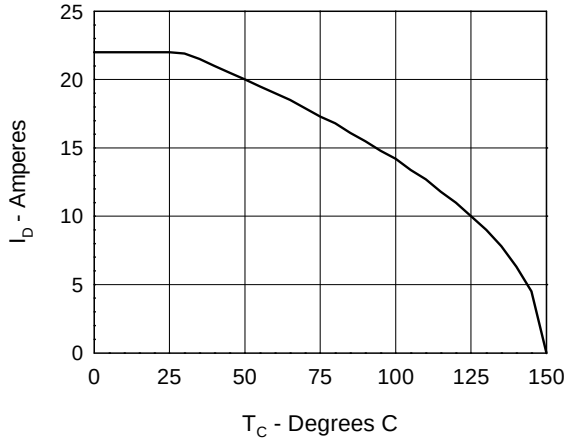


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

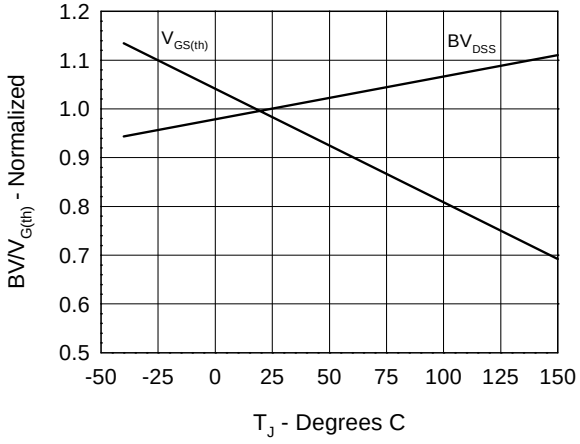


Fig.7 Gate Charge Characteristic Curve

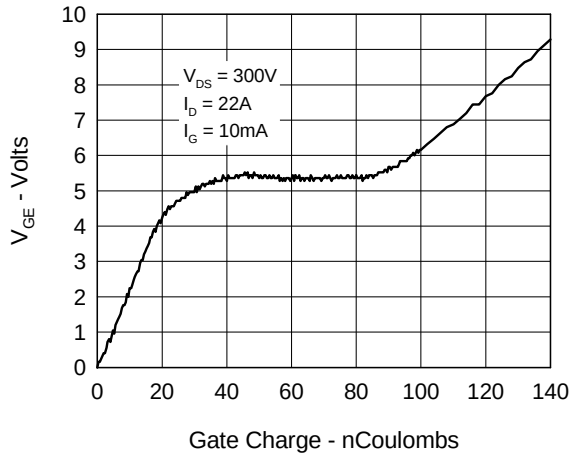


Fig.8 Forward Bias Safe Operating Area

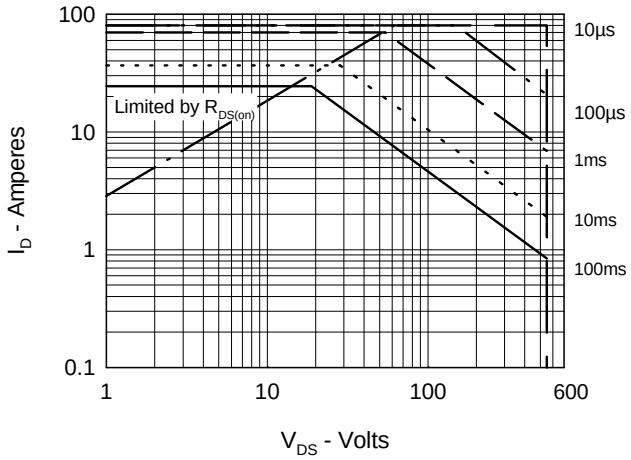


Fig.9 Capacitance Curves

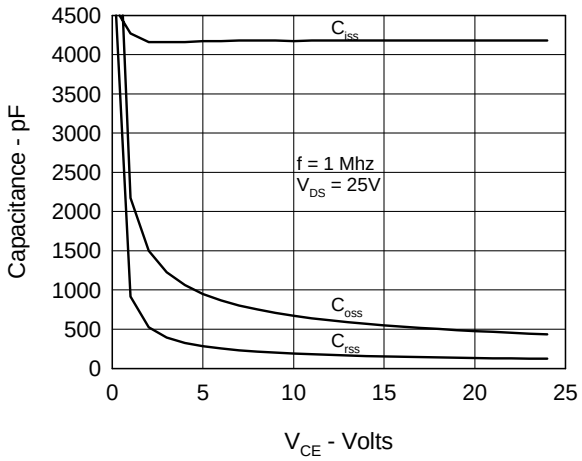


Fig.10 Source Current vs. Source to Drain Voltage

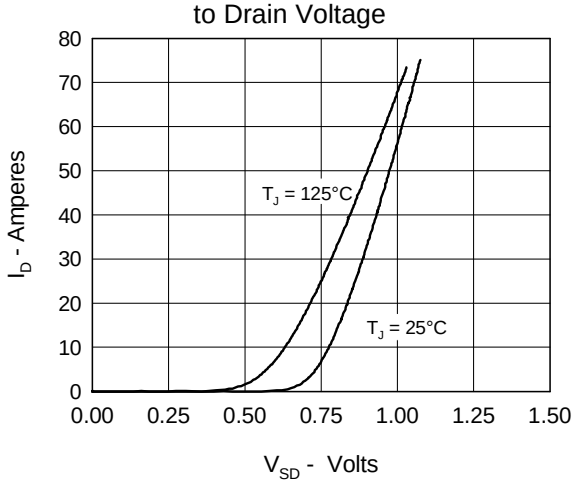


Fig.11 Transient Thermal Impedance