

## Features

- Compatible with MCS<sup>®</sup>-51 Products
- 2K Bytes of Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- 2.7V to 6V Operating Range
- Fully Static Operation: 0 Hz to 16 MHz
- Two-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 15 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial UART Channel
- Direct LED Drive Outputs
- On-chip Analog Comparator
- Low-power Idle and Power-down Modes
- 6 Clocks per Machine Cycle Operation

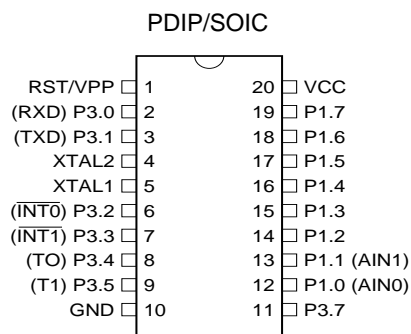
## Description

The AT89C2051x2 is a low-voltage, high-performance CMOS 8-bit microcontroller with 2K bytes of Flash programmable memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C2051x2 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89C2051x2 provides the following standard features: 2K bytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five-vector, two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051x2 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Furthermore, the AT89C2051x2 executes one machine cycle in 6 clock cycles, providing twice the speed of the AT89C2051 device. The user gains the flexibility to divide input frequency crystals by 2 (using less expensive components), while keeping the same CPU power. Alternatively, the user can save on power consumption while keeping the same CPU power (oscillator power saving).

## Pin Configuration

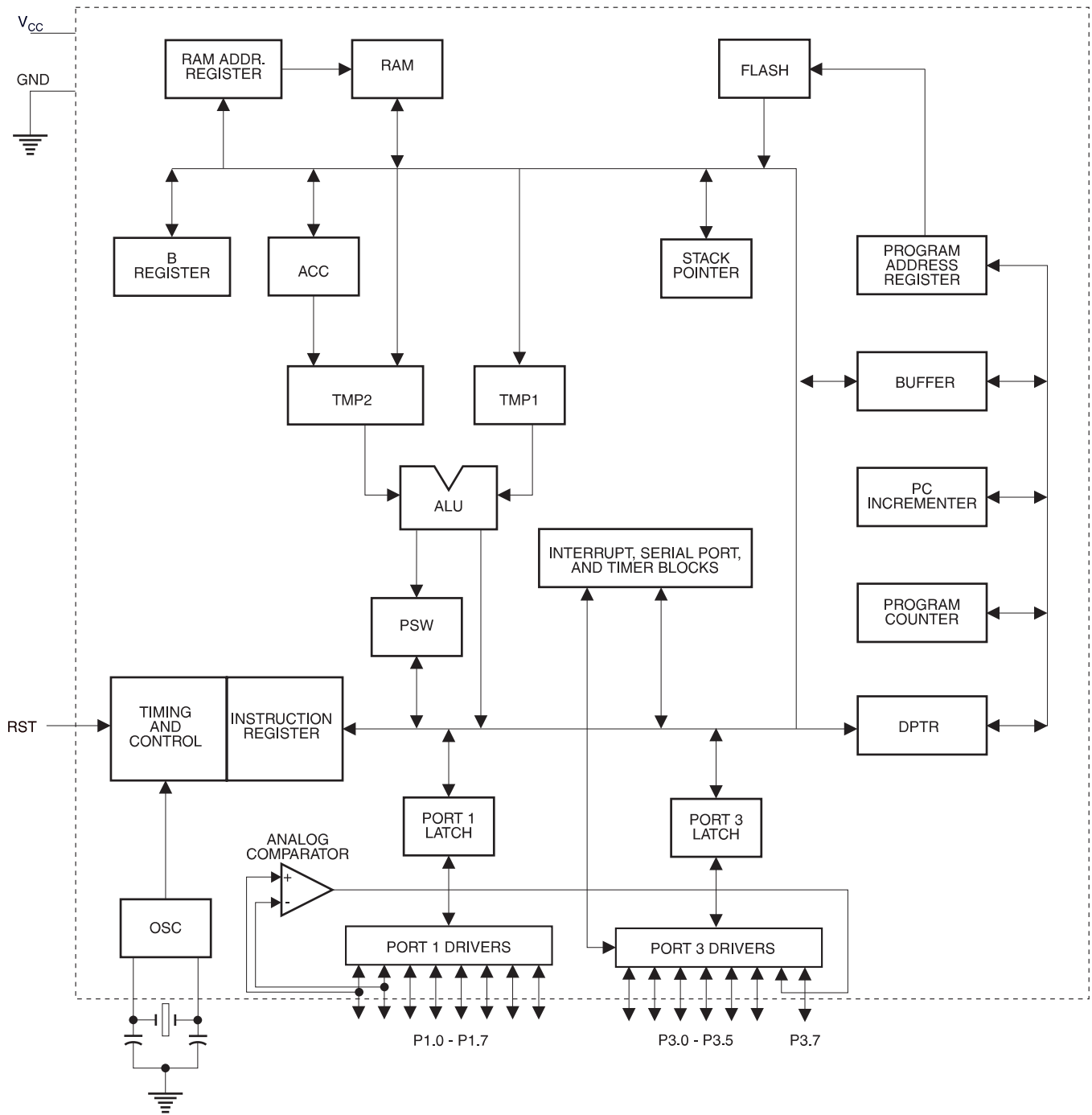


## 8-bit Microcontroller with 2K Bytes Flash

## AT89C2051x2



# Block Diagram



## Pin Description

**VCC** Supply voltage.

**GND** Ground.

**Port 1** Port 1 is an 8-bit bi-directional I/O port. Port pins P1.2 to P1.7 provide internal pull-ups. P1.0 and P1.1 require external pull-ups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current ( $I_{IL}$ ) because of the internal pull-ups.

Port 1 also receives code data during Flash programming and verification.

**Port 3** Port 3 pins P3.0 to P3.5, P3.7 are seven bi-directional I/O pins with internal pull-ups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the pull-ups.

Port 3 also serves the functions of various special features of the AT89C2051x2 as listed below:

| Port Pin | Alternate Functions                             |
|----------|---|
| P3.0     | RXD (serial input port)                         |
| P3.1     | TXD (serial output port)                        |
| P3.2     | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3     | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4     | T0 (timer 0 external input)                     |
| P3.5     | T1 (timer 1 external input)                     |

Port 3 also receives some control signals for Flash programming and verification.

**RST** Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

Each machine cycle takes 6 oscillator or clock cycles.

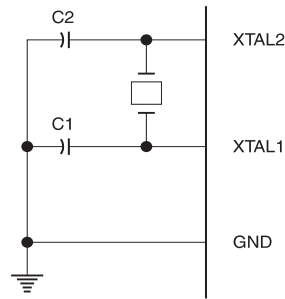
**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**XTAL2** Output from the inverting oscillator amplifier.

## Oscillator Characteristics

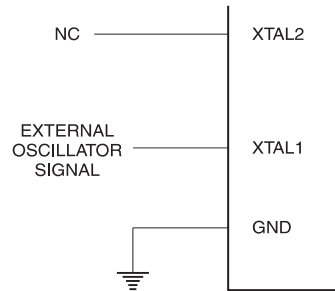
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

**Figure 1.** Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals  
= 40 pF ± 10 pF for Ceramic Resonators

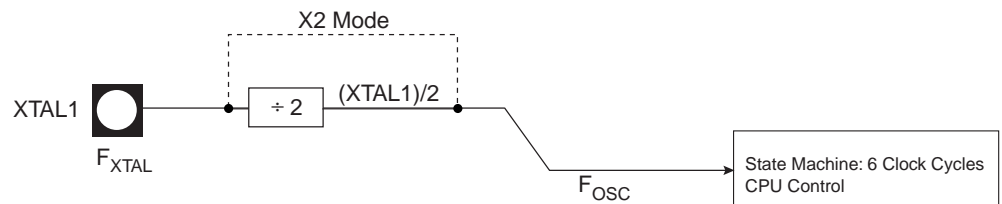
**Figure 2.** External Clock Drive Configuration



## X2 Mode Description

The clock for the entire circuit and peripherals is normally divided by 2 before being used by the CPU core and peripherals. This allows any cyclic ratio (duty cycle) to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio (duty cycle) between 40% to 60%. Figure 3 shows the clock generation block diagram.

**Figure 3.** Clock Generation Block Diagram



## Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the table below.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

**Table 1. AT89C2051x2 SFR Map and Reset Values**

|      |                  |                  |                 |                 |                 |                 |                  |      |
|------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|------------------|------|
| 0F8H |                  |                  |                 |                 |                 |                 |                  | 0FFH |
| 0F0H | B<br>00000000    |                  |                 |                 |                 |                 |                  | 0F7H |
| 0E8H |                  |                  |                 |                 |                 |                 |                  | 0EFH |
| 0E0H | ACC<br>00000000  |                  |                 |                 |                 |                 |                  | 0E7H |
| 0D8H |                  |                  |                 |                 |                 |                 |                  | 0DFH |
| 0D0H | PSW<br>00000000  |                  |                 |                 |                 |                 |                  | 0D7H |
| 0C8H |                  |                  |                 |                 |                 |                 |                  | 0CFH |
| 0C0H |                  |                  |                 |                 |                 |                 |                  | 0C7H |
| 0B8H | IP<br>XXX00000   |                  |                 |                 |                 |                 |                  | 0BFH |
| 0B0H | P3<br>11111111   |                  |                 |                 |                 |                 |                  | 0B7H |
| 0A8H | IE<br>0XX00000   |                  |                 |                 |                 |                 |                  | 0AFH |
| 0A0H |                  |                  |                 |                 |                 |                 |                  | 0A7H |
| 98H  | SCON<br>00000000 | SBUF<br>XXXXXXXX |                 |                 |                 |                 |                  | 9FH  |
| 90H  | P1<br>11111111   |                  |                 |                 |                 |                 |                  | 97H  |
| 88H  | TCON<br>00000000 | TMOD<br>00000000 | TL0<br>00000000 | TL1<br>00000000 | TH0<br>00000000 | TH1<br>00000000 |                  | 8FH  |
| 80H  |                  | SP<br>00000111   | DPL<br>00000000 | DPH<br>00000000 |                 |                 | PCON<br>0XXX0000 | 87H  |



## Restrictions on Certain Instructions

The AT89C2051x2 is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 2K bytes of Flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K for the AT89C2051x2. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89C2051x2 (with 2K of memory), whereas LJMP 900H would not.

### Branching Instructions

LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR

These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 7FFH for the AT89C2051x2). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ

With these conditional branching instructions, the same rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts, the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

### MOVX-related Instructions, Data Memory

The AT89C2051x2 contains 128 bytes of internal data memory. Thus, in the AT89C2051x2, the stack depth is limited to 128 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

## Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

### Lock Bit Protection Modes<sup>(1)</sup>

| Program Lock Bits |     |     | Protection Type                               |
|-------------------|-----|-----|---|
|                   | LB1 | LB2 |   |
| 1                 | U   | U   | No program lock features.                     |
| 2                 | P   | U   | Further programming of the Flash is disabled. |
| 3                 | P   | P   | Same as mode 2, also verify is disabled.      |

Note: 1. The Lock Bits can only be erased with the Chip Erase operation.

## Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

**P1.0 and P1.1 should be set to “0” if no external pull-ups are used, or set to “1” if external pull-ups are used.**

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

## Power-down Mode

In the power-down mode the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before  $V_{CC}$  is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

**P1.0 and P1.1 should be set to “0” if no external pull-ups are used, or set to “1” if external pull-ups are used.**

## Programming the Flash

The AT89C2051x2 is shipped with the 2K bytes of on-chip Flash code memory array in the erased state (i.e., contents = FFH) and ready to be programmed. The code memory array is programmed one byte at a time. *Once the array is programmed, to re-program any non-blank byte, the entire memory array needs to be erased electrically.*

**Internal Address Counter:** The AT89C2051x2 contains an internal memory address counter which is always reset to 000H on the rising edge of RST and is advanced by applying a positive going pulse to pin XTAL1.

**Programming Algorithm:** To program the AT89C2051x2, the following sequence is recommended.

1. Power-up sequence:  
Apply power between  $V_{CC}$  and GND pins  
Set RST and XTAL1 to GND
2. Set pin RST to “H”  
Set pin P3.2 to “H”
3. Apply the appropriate combination of “H” or “L” logic levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.

To Program and Verify the Array:

1. Apply data for Code byte at location 000H to P1.0 to P1.7.
2. Raise RST to 12V to enable programming.
3. Pulse P3.2 once to program a byte in the program memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.2 ms.

4. To verify the programmed data, lower RST from 12V to logic “H” level and set pins P3.3 to P3.7 to the appropriate levels. Output data can be read at the port P1 pins.
5. To program a byte at the next address location, pulse XTAL1 pin once to advance the internal address counter. Apply new data to the port P1 pins.
6. Repeat steps 6 through 8, changing data and advancing the address counter for the entire 2-Kbyte array or until the end of the object file is reached.
7. Power-off sequence:
  - set XTAL1 to “L”
  - set RST to “L”
  - Turn  $V_{CC}$  power off

**Data Polling:** The AT89C2051x2 features  $\overline{\text{Data}}$  Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P1.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin.  $\overline{\text{Data}}$  Polling may begin any time after a write cycle has been initiated.

**Ready/Busy:** The Progress of byte programming can also be monitored by the RDY/ $\overline{\text{BSY}}$  output signal. Pin P3.1 is pulled low after P3.2 goes High during programming to indicate BUSY. P3.1 is pulled High again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed code data can be read back via the data lines for verification:

1. Reset the internal address counter to 000H by bringing RST from “L” to “H”.
2. Apply the appropriate control signals for Read Code data and read the output data at the port P1 pins.
3. Pulse pin XTAL1 once to advance the internal address counter.
4. Read the next code data byte at the port P1 pins.
5. Repeat steps 3 and 4 until the entire array is read.

The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase:** The entire program memory array (2K bytes) and the two Lock Bits are erased electrically by using the proper combination of control signals and by holding P3.2 low for 10 ms. The code array is written with all “1”s in the Chip Erase operation and must be executed before any non-blank memory byte can be re-programmed.

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 000H, 001H, and 002H, except that P3.5 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel  
 (001H) = 22H indicates AT89C2051x2

## Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

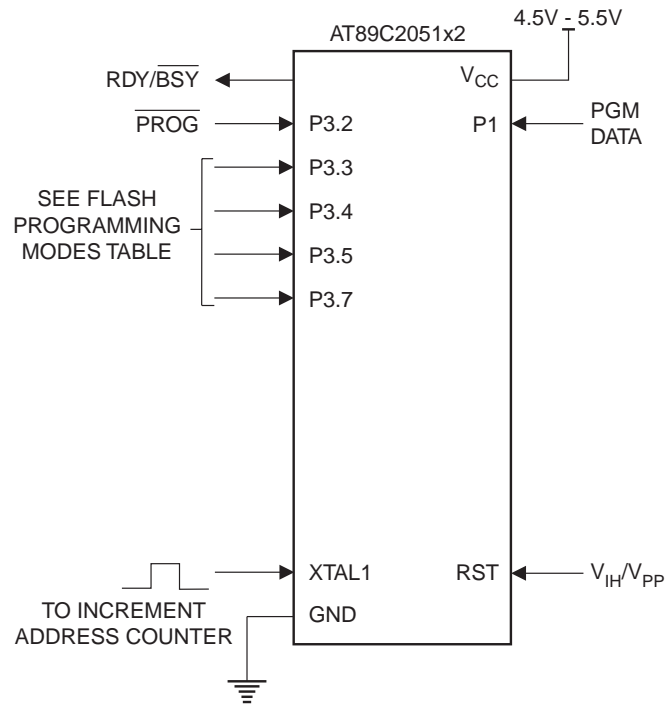


## Flash Programming Modes

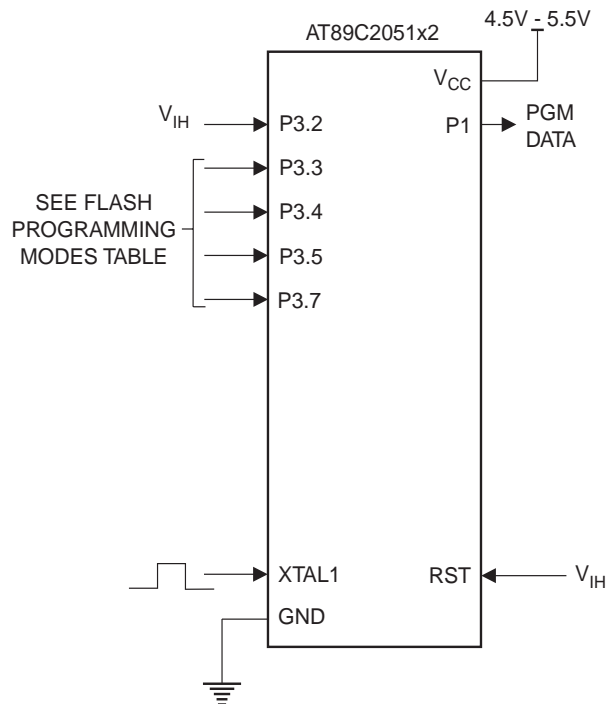
| Mode                              |         | RST/VPP | P3.2/ $\overline{\text{PROG}}$ | P3.3 | P3.4 | P3.5 | P3.7 |
|-----------------------------------|---------|---------|--------------------------------|------|------|------|------|
| Write Code Data <sup>(1)(3)</sup> |         | 12V     |                                | L    | H    | H    | H    |
| Read Code Data <sup>(1)</sup>     |         | H       | H                              | L    | L    | H    | H    |
| Write Lock                        | Bit - 1 | 12V     |                                | H    | H    | H    | H    |
|                                   | Bit - 2 | 12V     |                                | H    | H    | L    | L    |
| Chip Erase                        |         | 12V     | (2)                            | H    | L    | L    | L    |
| Read Signature Byte               |         | H       | H                              | L    | L    | L    | L    |

- Notes:
1. The internal memory address counter is reset to 000H on the rising edge of RST and is advanced by a positive pulse at XTAL1 pin.
  2. Chip Erase requires a 10 ms  $\overline{\text{PROG}}$  pulse.
  3. P3.1 is pulled Low during programming to indicate RDY/ $\overline{\text{BSY}}$ .

**Figure 4.** Programming the Flash Memory



**Figure 5.** Verifying the Flash Memory



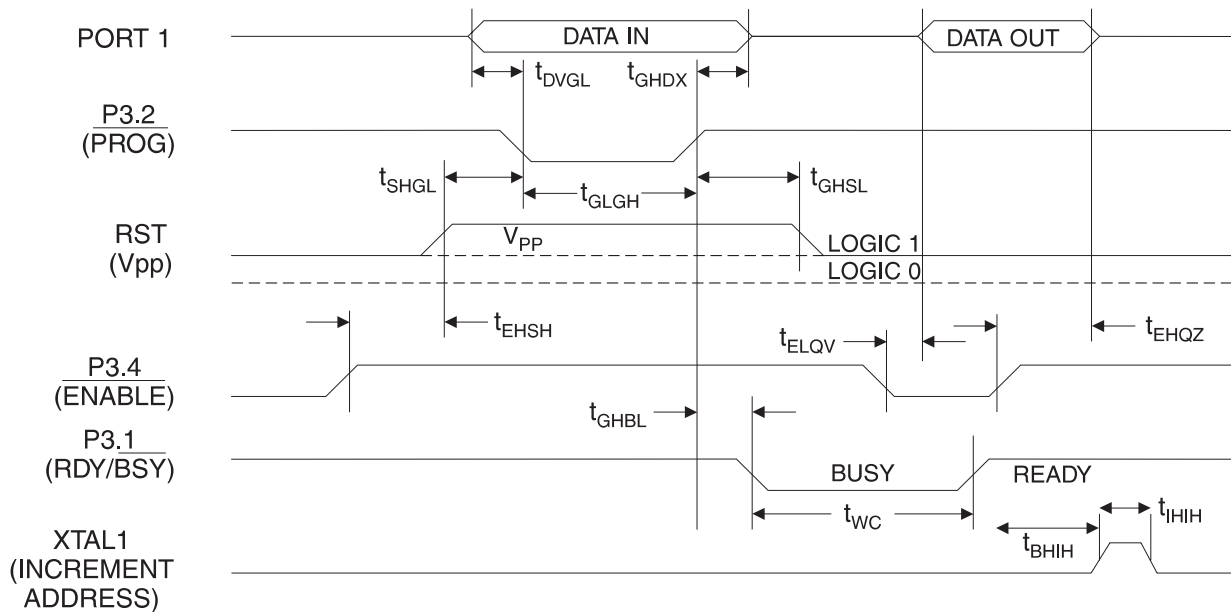
## Flash Programming and Verification Characteristics

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{CC} = 5.0 \pm 10\%$

| Symbol     | Parameter   | Min  | Max  | Units         |
|------------|---|------|------|---------------|
| $V_{PP}$   | Programming Enable Voltage                                    | 11.5 | 12.5 | V             |
| $I_{PP}$   | Programming Enable Current                                    |      | 250  | $\mu\text{A}$ |
| $t_{DVGL}$ | Data Setup to $\overline{\text{PROG}}$ Low                    | 1.0  |      | $\mu\text{s}$ |
| $t_{GHDX}$ | Data Hold after $\overline{\text{PROG}}$                      | 1.0  |      | $\mu\text{s}$ |
| $t_{EHS}$  | P3.4 ( $\overline{\text{ENABLE}}$ ) High to $V_{PP}$          | 1.0  |      | $\mu\text{s}$ |
| $t_{SHGL}$ | $V_{PP}$ Setup to $\overline{\text{PROG}}$ Low                | 10   |      | $\mu\text{s}$ |
| $t_{GHSL}$ | $V_{PP}$ Hold after $\overline{\text{PROG}}$                  | 10   |      | $\mu\text{s}$ |
| $t_{GLGH}$ | $\overline{\text{PROG}}$ Width                                | 1    | 110  | $\mu\text{s}$ |
| $t_{ELQV}$ | $\overline{\text{ENABLE}}$ Low to Data Valid                  |      | 1.0  | $\mu\text{s}$ |
| $t_{EHQZ}$ | Data Float after $\overline{\text{ENABLE}}$                   | 0    | 1.0  | $\mu\text{s}$ |
| $t_{GHBL}$ | $\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low |      | 50   | ns            |
| $t_{WC}$   | Byte Write Cycle Time   |      | 2.0  | ms            |
| $t_{BHIH}$ | $\text{RDY}/\overline{\text{BSY}}$ to Increment Clock Delay   | 1.0  |      | $\mu\text{s}$ |
| $t_{IHIL}$ | Increment Clock High  | 200  |      | ns            |

Note: 1. Only used in 12-volt programming mode.

## Flash Programming and Verification Waveforms



## Absolute Maximum Ratings\*

|  |                 |
|--|-----------------|
| Operating Temperature .....                        | -55°C to +125°C |
| Storage Temperature .....                          | -65°C to +150°C |
| Voltage on Any Pin<br>with Respect to Ground ..... | -1.0V to +7.0V  |
| Maximum Operating Voltage .....                    | 6.6V            |
| DC Output Current.....                             | 25.0 mA         |

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $6.0\text{V}$  (unless otherwise noted)

| Symbol    | Parameter   | Condition  | Min                | Max                | Units            |
|-----------|---|--|--------------------|--------------------|------------------|
| $V_{IL}$  | Input Low-voltage                                 |  | -0.5               | $0.2 V_{CC} - 0.1$ | V                |
| $V_{IH}$  | Input High-voltage                                | (Except XTAL1, RST)  | $0.2 V_{CC} + 0.9$ | $V_{CC} + 0.5$     | V                |
| $V_{IH1}$ | Input High-voltage                                | (XTAL1, RST)   | $0.7 V_{CC}$       | $V_{CC} + 0.5$     | V                |
| $V_{OL}$  | Output Low-voltage <sup>(1)</sup><br>(Ports 1, 3) | $I_{OL} = 20\text{ mA}$ , $V_{CC} = 5\text{V}$<br>$I_{OL} = 10\text{ mA}$ , $V_{CC} = 2.7\text{V}$ |                    | 0.5                | V                |
| $V_{OH}$  | Output High-voltage<br>(Ports 1, 3)               | $I_{OH} = -80\ \mu\text{A}$ , $V_{CC} = 5\text{V} \pm 10\%$  | 2.4                |                    | V                |
|           |   | $I_{OH} = -30\ \mu\text{A}$  | $0.75 V_{CC}$      |                    | V                |
|           |   | $I_{OH} = -12\ \mu\text{A}$  | $0.9 V_{CC}$       |                    | V                |
| $I_{IL}$  | Logical 0 Input Current<br>(Ports 1, 3)           | $V_{IN} = 0.45\text{V}$  |                    | -50                | $\mu\text{A}$    |
| $I_{TL}$  | Logical 1 to 0 Transition Current<br>(Ports 1, 3) | $V_{IN} = 2\text{V}$ , $V_{CC} = 5\text{V} \pm 10\%$   |                    | -750               | $\mu\text{A}$    |
| $I_{LI}$  | Input Leakage Current<br>(Port P1.0, P1.1)        | $0 < V_{IN} < V_{CC}$  |                    | $\pm 10$           | $\mu\text{A}$    |
| $V_{OS}$  | Comparator Input Offset Voltage                   | $V_{CC} = 5\text{V}$   |                    | 20                 | mV               |
| $V_{CM}$  | Comparator Input Common<br>Mode Voltage           |  | 0                  | $V_{CC}$           | V                |
| RRST      | Reset Pull-down Resistor                          |  | 50                 | 300                | $\text{K}\Omega$ |
| $C_{IO}$  | Pin Capacitance                                   | Test Freq. = 1 MHz, $T_A = 25^\circ\text{C}$   |                    | 10                 | pF               |
| $I_{CC}$  | Power Supply Current                              | Active Mode, 12 MHz, $V_{CC} = 6\text{V}/3\text{V}$  |                    | 15/5.5             | mA               |
|           |   | Idle Mode, 12 MHz, $V_{CC} = 6\text{V}/3\text{V}$<br>P1.0 & P1.1 = 0V or $V_{CC}$                  |                    | 5/1                | mA               |
|           | Power-down Mode <sup>(2)</sup>                    | $V_{CC} = 6\text{V}$ , P1.0 & P1.1 = 0V or $V_{CC}$  |                    | 100                | $\mu\text{A}$    |
|           |   | $V_{CC} = 3\text{V}$ , P1.0 & P1.1 = 0V or $V_{CC}$  |                    | 20                 | $\mu\text{A}$    |

Notes: 1. Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:

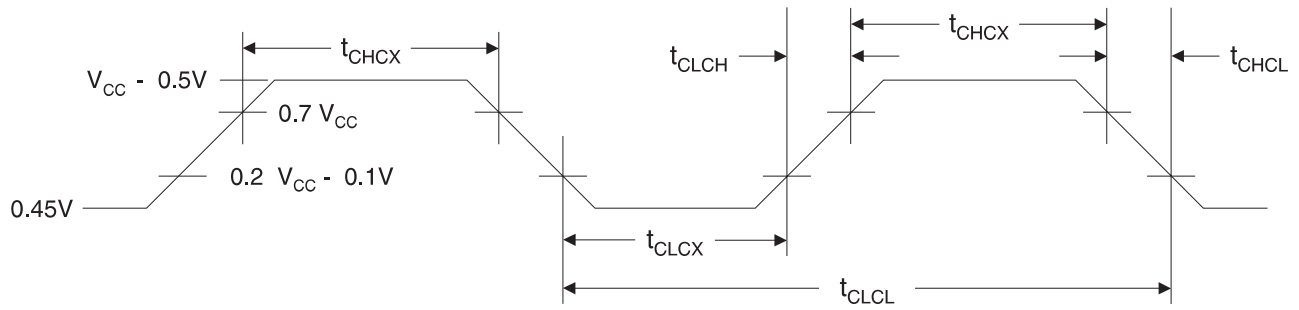
Maximum  $I_{OL}$  per port pin: 20 mA

Maximum total  $I_{OL}$  for all output pins: 80 mA

If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum  $V_{CC}$  for Power-down is 2V.

### External Clock Drive Waveforms



### External Clock Drive

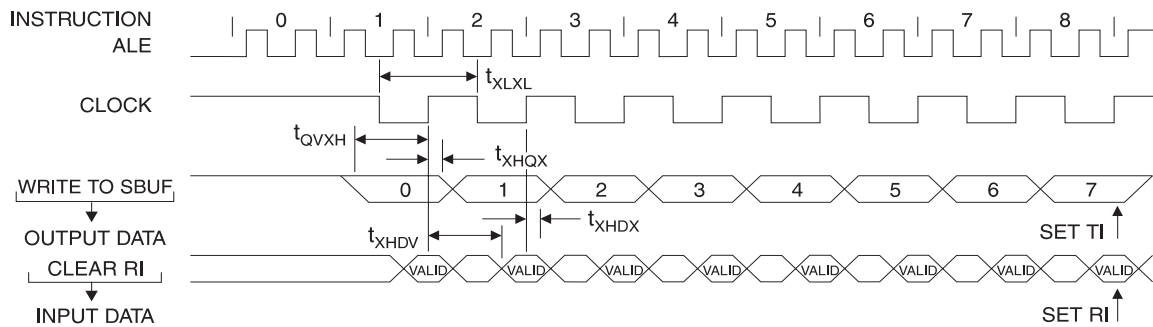
| Symbol              | Parameter                 | $V_{CC} = 2.7V \text{ to } 6.0V$ |     | $V_{CC} = 4.0V \text{ to } 6.0V$ |     | Units |
|---------------------|---------------------------|----------------------------------|-----|----------------------------------|-----|-------|
|                     |                           | Min                              | Max | Min                              | Max |       |
| $1/t_{CLCL}$        | Oscillator Frequency      | 0                                | 8   | 0                                | 16  | MHz   |
| $t_{CLCL}$          | Clock Period              | 12.5                             |     | 62.5                             |     | ns    |
| $t_{CHCX}$          | High Time                 | 45                               |     | 22.5                             |     | ns    |
| $t_{CLCX}$          | Low Time                  | 45                               |     | 22.5                             |     | ns    |
| $t_{CLCH}$          | Rise Time                 |                                  | 10  |                                  | 10  | ns    |
| $t_{CHCL}$          | Fall Time                 |                                  | 10  |                                  | 10  | ns    |
| $t_{CHCX}/t_{CLCX}$ | Cyclic Ratio (duty cycle) | 40                               | 60  | 40                               | 60  | %     |

## Serial Port Timing: Shift Register Mode Test Conditions

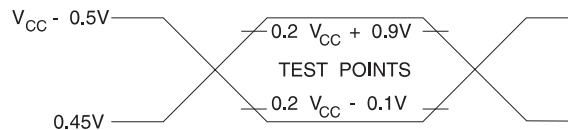
$V_{CC} = 5.0V \pm 20\%$ ; Load Capacitance = 80 pF

| Symbol     | Parameter                                | 12 MHz Osc |     | Variable Oscillator |                  | Units   |
|------------|--|------------|-----|---------------------|------------------|---------|
|            |  | Min        | Max | Min                 | Max              |         |
| $t_{XLXL}$ | Serial Port Clock Cycle Time             | 1.0        |     | $12t_{CLCL}$        |                  | $\mu s$ |
| $t_{QVXH}$ | Output Data Setup to Clock Rising Edge   | 700        |     | $10t_{CLCL}-133$    |                  | ns      |
| $t_{XHGX}$ | Output Data Hold after Clock Rising Edge | 50         |     | $2t_{CLCL}-117$     |                  | ns      |
| $t_{XHDX}$ | Input Data Hold after Clock Rising Edge  | 0          |     | 0                   |                  | ns      |
| $t_{XHDV}$ | Clock Rising Edge to Input Data Valid    |            | 700 |                     | $10t_{CLCL}-133$ | ns      |

## Shift Register Mode Timing Waveforms



## AC Testing Input/Output Waveforms<sup>(1)</sup>



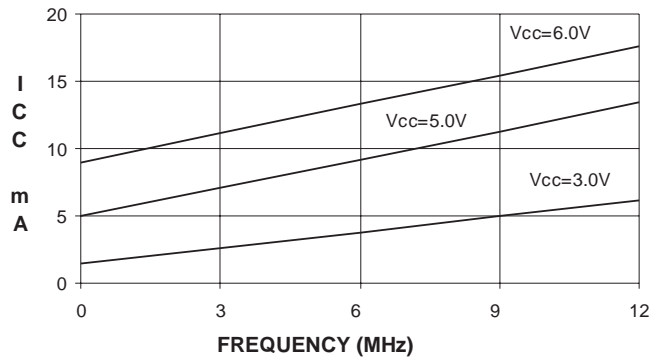
Note: 1. AC Inputs during testing are driven at  $V_{CC} - 0.5V$  for a logic 1 and  $0.45V$  for a logic 0. Timing measurements are made at  $V_{IH}$  min. for a logic 1 and  $V_{IL}$  max. for a logic 0.

## Float Waveforms<sup>(1)</sup>

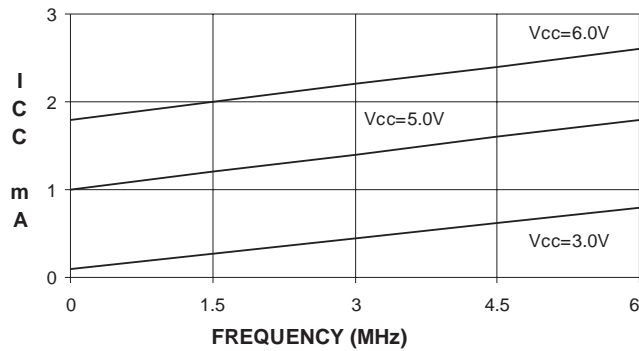


Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.

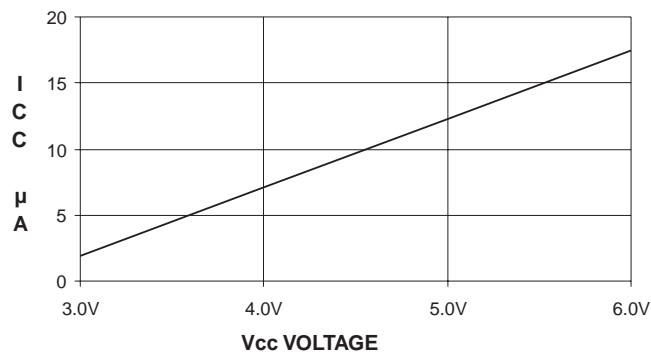
**AT89C2051x2**  
TYPICAL ICC - ACTIVE (85°C)



**AT89C2051x2**  
TYPICAL ICC - IDLE (85°C)



**AT89C2051x2**  
TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



- Notes:
1. XTAL1 tied to GND for  $I_{CC}$  (power-down).
  2. P.1.0 and P.1.1 =  $V_{CC}$  or GND.
  3. Lock bits programmed.



## Ordering Information

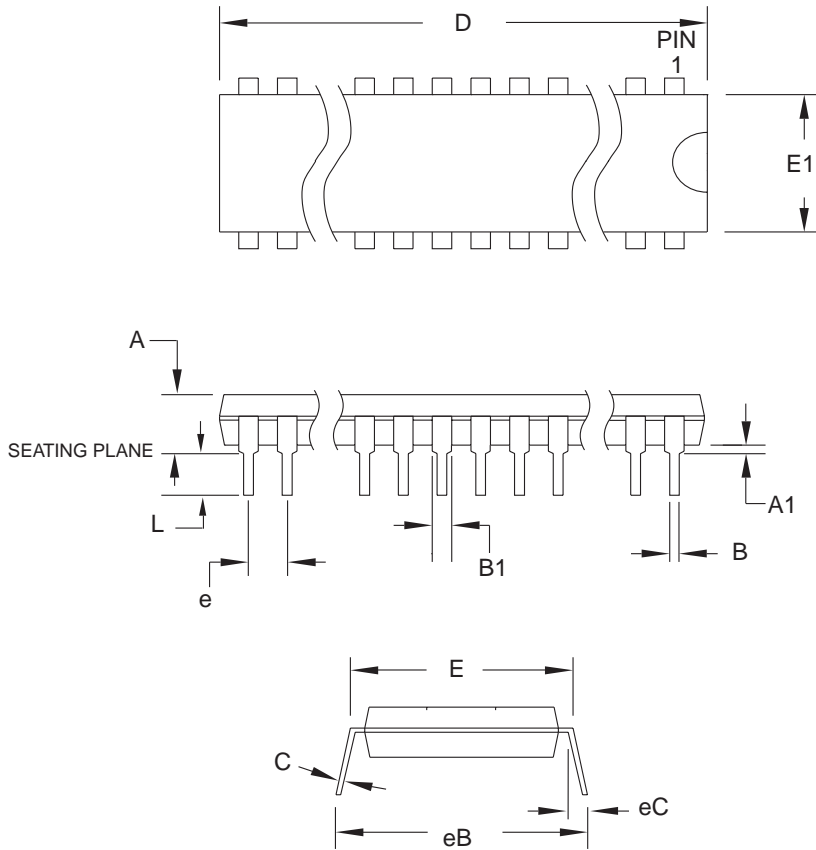
| Speed (MHz) | Power Supply | Ordering Code                        | Package      | Operation Range                 |
|-------------|--------------|--------------------------------------|--------------|---------------------------------|
| 8           | 2.7V to 6.0V | AT89C2051x2-8PC<br>AT89C2051x2-8SC   | 20P3<br>20S2 | Commercial<br>(0° C to 70° C)   |
|             |              | AT89C2051x2-8PI<br>AT89C2051x2-8SI   | 20P3<br>20S2 | Industrial<br>(-40° C to 85° C) |
| 16          | 4.0V to 6.0V | AT89C2051x2-16PC<br>AT89C2051x2-16SC | 20P3<br>20S2 | Commercial<br>(0° C to 70° C)   |
|             |              | AT89C2051x2-16PI<br>AT89C2051x2-16SI | 20P3<br>20S2 | Industrial<br>(-40° C to 85° C) |

| Package Type |  |
|--------------|--|
| <b>20P3</b>  | 20-lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)    |
| <b>20S2</b>  | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |



Package Information

20P3 – PDIP



COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | –         | –   | 5.334  |        |
| A1     | 0.381     | –   | –      |        |
| D      | 25.984    | –   | 25.493 | Note 2 |
| E      | 7.620     | –   | 8.255  |        |
| E1     | 6.096     | –   | 7.112  | Note 2 |
| B      | 0.356     | –   | 0.559  |        |
| B1     | 1.270     | –   | 1.551  |        |
| L      | 2.921     | –   | 3.810  |        |
| C      | 0.203     | –   | 0.356  |        |
| eB     | –         | –   | 10.922 |        |
| eC     | 0.000     | –   | 1.524  |        |
| e      | 2.540 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-001, Variation AD.
  2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

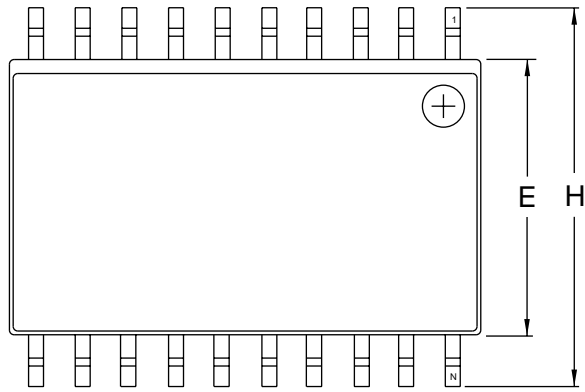
**ATMEL** 2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**  
20P3, 20-lead (0.300"/7.62 mm Wide) Plastic Dual  
Inline Package (PDIP)

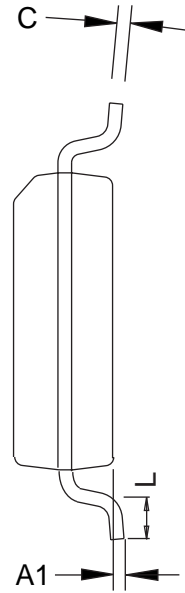
**DRAWING NO.**  
20P3

**REV.**  
B

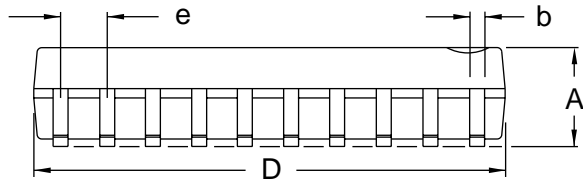
## 20S2 – SOIC



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure = inches)

| SYMBOL | MIN       | NOM | MAX    | NOTE |
|--------|-----------|-----|--------|------|
| A      | 0.0926    |     | 0.1043 |      |
| A1     | 0.0040    |     | 0.0118 |      |
| b      | 0.0130    |     | 0.0200 | 4    |
| C      | 0.0091    |     | 0.0125 |      |
| D      | 0.4961    |     | 0.5118 | 1    |
| E      | 0.2914    |     | 0.2992 | 2    |
| H      | 0.3940    |     | 0.4190 |      |
| L      | 0.0160    |     | 0.050  | 3    |
| e      | 0.050 BSC |     |        |      |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
  2. Dimension "D" does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
  3. Dimension "E" does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
  4. "L" is the length of the terminal for soldering to a substrate.
  5. The lead width "b", as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side. 1/9/02



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**20S2**, 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)

**DRAWING NO.**

20S2

**REV.**

A



## Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## Regional Headquarters

### Europe

Atmel Sarl  
Route des Arsenalux 41  
Case Postale 80  
CH-1705 Fribourg  
Switzerland  
Tel: (41) 26-426-5555  
Fax: (41) 26-426-5500

### Asia

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

### Japan

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Atmel Operations

### Memory

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

### Microcontrollers

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

La Chantrerie  
BP 70602  
44306 Nantes Cedex 3, France  
Tel: (33) 2-40-18-18-18  
Fax: (33) 2-40-18-19-60

### ASIC/ASSP/Smart Cards

Zone Industrielle  
13106 Rousset Cedex, France  
Tel: (33) 4-42-53-60-00  
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park  
Maxwell Building  
East Kilbride G75 0QR, Scotland  
Tel: (44) 1355-803-000  
Fax: (44) 1355-242-743

### RF/Automotive

Theresienstrasse 2  
Postfach 3535  
74025 Heilbronn, Germany  
Tel: (49) 71-31-67-0  
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

### Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine  
BP 123  
38521 Saint-Egreve Cedex, France  
Tel: (33) 4-76-58-30-00  
Fax: (33) 4-76-58-34-80

---

## Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

**Disclaimer:** Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

© Atmel Corporation 2003. All rights reserved. Atmel® and combinations thereof are the registered trademarks of Atmel Corporation or its subsidiaries. MCS® is the registered trademark of Intel Corporation. Other terms and product names may be the trademarks of others.



Printed on recycled paper.