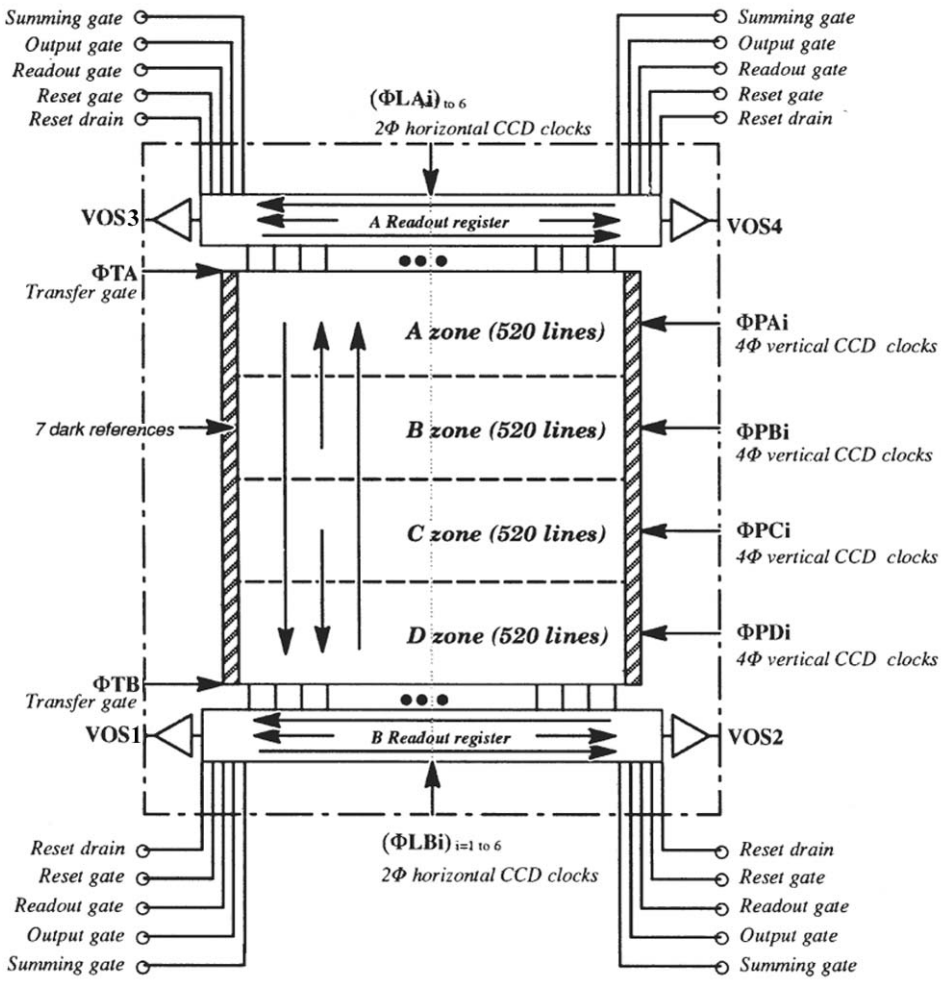
Features

- **Designed for Digital Photography, Graphic Arts, Medical and Scientific Applications**
- **Pixel 14 µm x 14 µm Photomos with 100% Aperture**
- **Image Zone: 28.67 mm x 28.67 mm**
- **Frame Readout Through 1, 2 or 4 Outputs**
- **Data Rates up to 4 x 20 MHz (Compatibility with 15 Frames/Second)**
- **Possible Binning 2 x 2 Pixels (Format 1024 x 1024 with Pixels of 28 µm x 28 µm)**
- **High Dynamic Range (up to 12600:1) even at:**
  - **Room Temperature**
  - **20 MHz/Output**
- **Very Low Dark Current (MPP Mode)**
- **Optimized Resolution and Responsivity in the 400 - 1100 nm Spectrum**
- **Other Possible Full Frame Operating Modes:**
  - **1536 x 2048 Pixels of 14 µm x 14 µm**
  - **768 x 1024 Pixels of 28 µm x 28 µm**
- **Compatible with Fiber Optic Face Plate Coupling**
- **On Request: Frame Transfer Architecture (On-chip Memory Defined by Mechanical Shielding) Featuring:**
  - **1024 (V) x 2048 (H) Active Pixels of 14 µm x 14 µm**
  - **512 (V) x 1024 (H) Active Pixels of 28 µm x 28 µm**
  - **512 (V) x 2048 (H) Active Pixels of 14 µm x 14 µm**

Figure 1. TH7899M Organization



Full Field CCD Image Sensor 2048 x 2048 Pixels

TH7899M

Rev. 2201A–IMAGE–02/02

General Description

The TH7899M sensor is a 2048 x 2048 full frame Charge Couple Device (CCD) designed for a wide range of applications due to both its operating mode flexibility and its high dynamic range combined with its high resolution. The device is 180° symmetrical so if it is not plugged in the right side it will not be damaged.

The nominal photosensitive area is made up of 2048 x 2048 useful pixels split vertically in 4 zones A, B, C and D. Each zone can be driven separately by four-phase clocks (ΦP1 ΦP2 ΦP3 and ΦP4) allowing different operating modes as described in “Image Area” on page 3.

There are two identical horizontal shift registers: one at the top of the image area (register A) and one at the bottom (register B). At each end of the two readout registers, a summing gate is located which can be clocked to allow a horizontal pixel summation in front of the on-chip output amplifier.

Applications

The TH7899M sensor is particularly suited to the following applications:

- Digital photography
- Medical applications
- Graphic arts
- Industrial applications
- Scientific applications

Functional Description

Pixel

The pixel size is 14 µm x 14 µm with 100% aperture. The following figures show the pixel structure.

Figure 2. Front View of a Photoelement

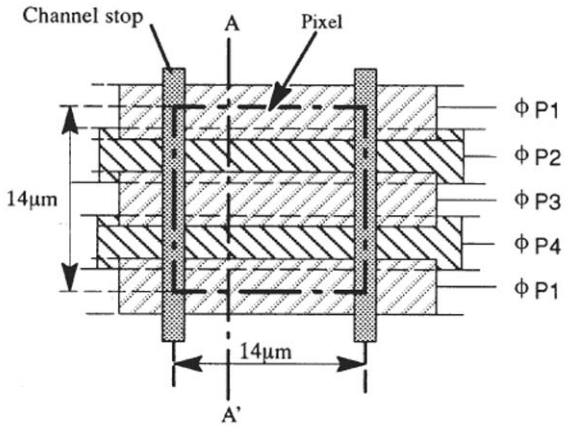


Figure 3. Cross Sectional View (AA') of a Photoelement and Potential Profile During Integration

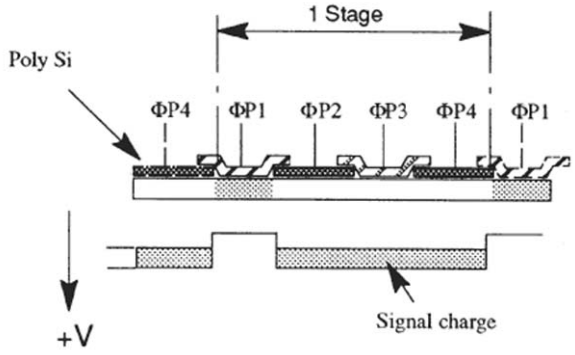


Image Area

The image area consists of an array of 2048 x 2048 useful photoelements for imaging.

The matrix also includes:

- 7 columns of dark reference and 5 isolation columns (half covered) on the right and left sides. The isolation columns are to ensure the 2048 active columns and are 100% photosensitive,
- 8 supplementary lines in each zone A B C and D; these lines are useful when using an optical shield in case of frame transfer architecture with memory zone to correct smearing (digital correction).

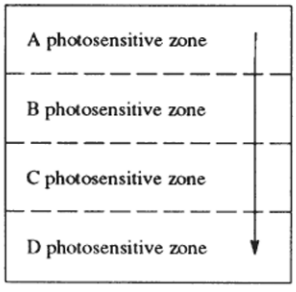
Among these 8 lines in zones A and D, 3 lines at the top and at the bottom of the full image area are masked with aluminium, all the other supplementary lines are photosensitive.

The image area is divided into 4 parts of 520 lines each (electrically but not optically). These 4 parts can be driven independently allowing different operating modes as described hereunder.

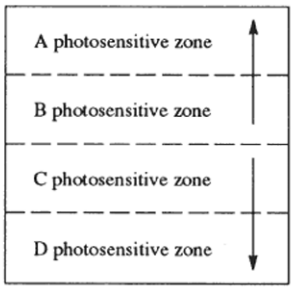
Full Field Modes (No Mechanical Shield On Package)

In such cases a mechanical shutter is needed to shield the array from incident illumination during the readout period to avoid parasitic signal (smearing) particularly at low data rates. Such a shutter is not necessary if no light is coming onto the photosensitive area during the readout time (e.g. in case of pulsed light source).

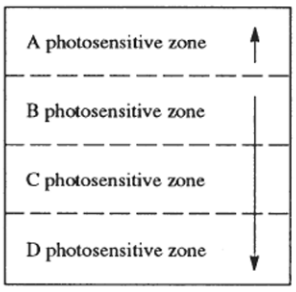
There are mainly three different modes which can square with different optical formats, with readout optimized in speed or with simplified operating conditions.



Configuration 1



Configuration 2



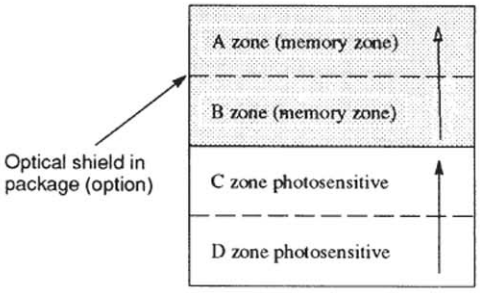
Configuration 3

Active Pixel Number	Image Zone Dimension	Useful Zones	Used Readout Register	Number of Possible Outputs	Configu-ration to be Used	Characteristics
2048 (V) x 2048 (H)	28.67 mm (V) x 28.67 mm (H)	A, B, C and D	B	1 or 2	1	Simplified operating conditions
2048 (V) x 2048 (H)	28.67 mm (V) x 28.67 mm (H)	A, B, C and D	A and B	2 or 4	2	2048 x 2048 optimized data rate
1024 (V) x 2048 (H)	14.34 mm (V) x 28.67 mm (H)	C and D	B	1 or 2	2	Adapted optical format
1536 (V) x 2048 (H) 1365 (V) x 2048 (H)	21.50 mm (V) x 28.67 mm (H) 19.11 mm (V) x 28.67 mm (H)	B, C and D	B	1 or 2	3	Adapted optical format Equivalent 24 x 36mm ratio
512 (V) x 2048 (H)	7.17 mm (V) x 28.67 mm (H)	A	A	1 or 2	3	Adapted optical format

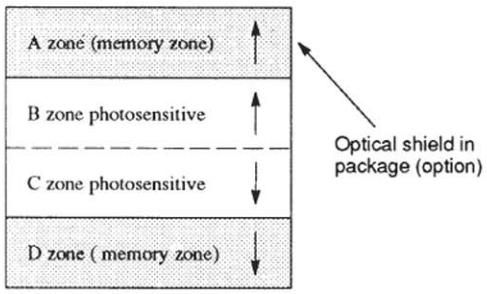
Note: 1. Binned modes (2 x 2 or 2 x 1) can be used which will lead to specific binned formats in particular the format 1024 x 1024 with an equivalent pixel size of 28 µm x 28 µm.

Frame Transfer Modes (Option On Package On Request)

These cases involve placing an optical shield in the package (on request) to define one or two memory zones according to the application shown in the figures below.



Configuration 4



Configuration 5

Active Pixel Number	Image Zone Dimension	Useful Zones	Used Readout Register	Number of Possible Outputs	Configu-ration to be Used	Characteristics
1024 (V) x 2048 (H)	14.34 mm (V) x 28.67 mm (H)	C and D	B	1 or 2	4	1024 x 2048 simplified operating conditions
1024 (V) x 2048 (H)	14.34 mm (H) x 28.67 mm (H)	B and C	A and B	2 or 4	5	1024 x 2048 optimized data rate
512 (V) x 2048 (H)	7.17 mm (V) x 28.67 mm (H)	A	A	1 or 2	5	Adapted optical format

Note: 1. Binned modes (2 x 2 or 2 x 1) can be used, this will lead to specific binned formats, in particular, the format 512 x 1024 with an equivalent pixel size of 28 µm x 28 µm.

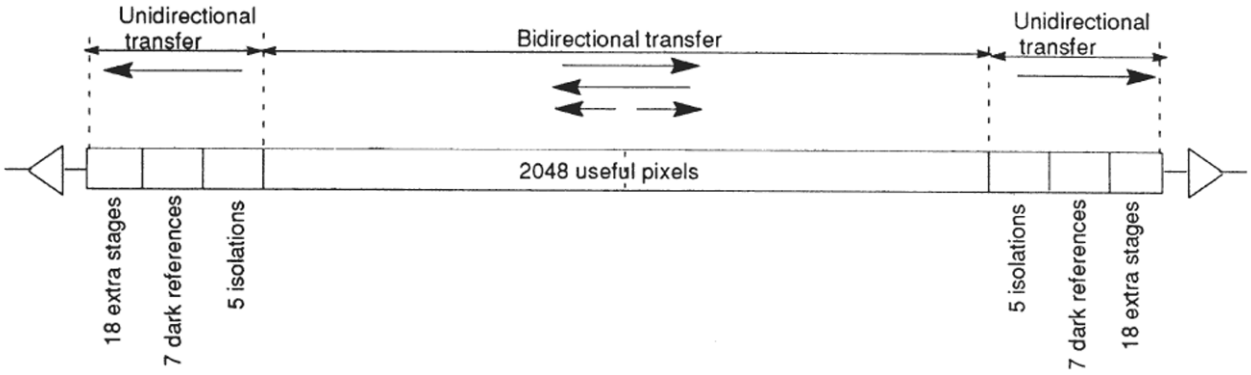
Horizontal Registers

The sensor has two readout registers located at the top (register A) and at the bottom (register B) of the image area. They can be driven independently by two phase clocks. Nevertheless to allow a multiple charge transfer direction for the useful pixels (left, right or half left and half right), the two clocks are split into 6 clocks ($\Phi LA_{i=1\ to\ 6}$ for the A register and $\Phi LB_{i=1\ to\ 6}$ for the register B). The transfer direction is fixed by the connection mode of the six clocks into 2 clocks.

The description of the connection with the transfer direction is described in “” on page 9.

The readout register has 2072 stages, with a further 18 extra stages at each end. Whatever the chosen transfer direction for the useful pixels, the 18 extra pixels, the 7 dark references and the 5 isolations are always transferred to the nearest output as shown in the figure hereunder.

Figure 4. A and B Readout Register Structure



The readout register can be driven in the MPP mode if necessary.

Binned Modes

Two types of summation can be performed:

- Vertical summation in each stage of the serial register (A or B)
- Horizontal summation in an output summing well driven by ΦS clock and located at each end of the readout registers (A and B).

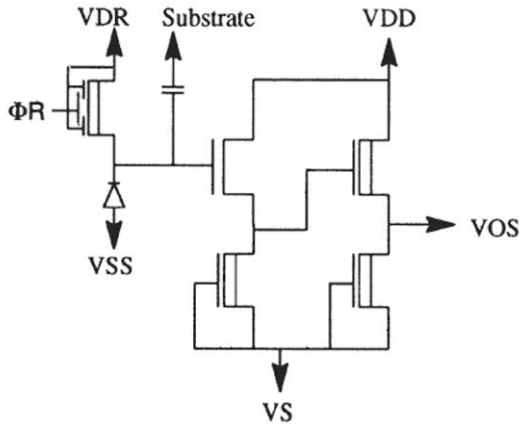
Nevertheless, one summation can be performed in both the register and the output summing, allowing in this way, to have a resulting signal of (2 x 2) contiguous pixels from the image area. Thus, the sensor is equivalent to a 1024 x 1024 array of a 28 µm x 28 µm pixel. When using the binned mode with a charge level, after summation, smaller than 300 ke- (typical value) it is better (optimization of dynamic and linearity) to keep the conversion factor at 7 µV/e- (with VGL = 1V and VDR = 13.5V). But for summing mode with charge level, after binning, higher than 300 ke-, the conversion factor should be reduced by increasing the VGL gate to 12V and the VDR reset drain to 15V. With such a method, the saturation charge is optimized for the binning mode.

This summing technique leads to an increased signal to noise ratio, larger pixel size, higher frame rates (for vertical binning only) but at the expense of a loss in resolution.

Output Amplifiers

The TH7899M sensor has four output amplifiers. These are located in each corner of the device at the ends of the readout register. Charge packets are clocked to a pre-charge capacitor (floating diffusion) whose potential varies linearly with the quantity of charge in each packet. This potential is applied to the input gate of a two stage source follower amplifier and the output signal is read. Then, the reset clock ΦR removes the charge from the floating diffusion via the reset drain VDR which imposes its reference level.

Figure 5. On-chip Output Amplifier Structure



Multi-Pinned-Phase (MPP) Mode

The TH7899M sensor operates in the MPP mode in order to substantially decrease dark current (typically from 0.6 nA/cm^2 to 25 pA/cm^2 at 25°C). Compared to standard technology, the MPP mode allows, while keeping all other performances unchanged, either to increase exposure time, or to operate at higher temperature.

Dark current is due to thermal generation in the substrate of the CCD. The different generation sources are as follows:

- surface states at the Si-SiO_2 interface which is the main contribution
- generation and diffusion in the bulk
- generation in the depleted zone

If the gates are biased with adequate negative biases, holes appear at the Si-SiO_2 interface and fill in the interface states suppressing their dark current contribution. As a result, only the minor bulk and depleted zone contributions remain.

Absolute Maximum Ratings*

Storage temperature..... -55°C to + 150°C Operating temperature ..... -40°C to + 85°C Temperature cycling .....15°C/mn	*NOTICE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionally at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

Maximum Applied Voltage	
Pins A3 A8 A13 A14 B3 B13 G1 G15 J1 J15 P3 P8 P13 R2 R3 R8 R13	0V (ground)
Maximum voltage applied (VGB) with respect to the substrate VSS	
Pins B5 B4 P12 P11 P4 P5 P6 P7 B12 B11 B10 B9 H15 H1 R6 R5 A10 A11 A5 A4 R12 R11 R4 R7 A9 A12 R1	|VGB| = 15V
Pins B6 A6 B7 A7 P9 R9 P10 R10	|VGB| = 12V
Pins R1 R15 A1 A15 A2 R14 P2 P14 B2 B14 P1 P15 B1 B15 K1 K15 F1 F15 L1 L15 E1 E15	VGB = -0.3 to 15.5V
Pins M1 M15 D1 D15	VGB = -0.3 to 12V
Maximum voltage difference ΔV between two pins of each group	
Pin group: R6 R5 P4 P5 P6 P7 H1 R4 R7	$\lvert\Delta V\rvert$ =15V
Pin group: A10 A11 B12 B11 B10 B9 H15 A9 A12	$\lvert\Delta V\rvert$ =15V
Pin group: B5 B6 A5 A6 B4 B7 A4 A7 P12 P9 R12 R9 P11 P10 R11 R10 H1 H15	$\lvert\Delta V\rvert$ =15V

Operating Range

Operating range defines the limits between which the functioning is guaranteed.

Electrical limits of applied signals are given in the operating condition section.

Operating Precautions

Shorting one of the video outputs to one of the input pins even temporarily, can permanently damage the output amplifier.

Due to MPP mode or negative voltages, image zone clocks and readout registers do not include ESD protection. To avoid degradation, the TH7899M device should be handled with a grounded bracelet and stored on a conductive layer used for shipment.

Operating Conditions

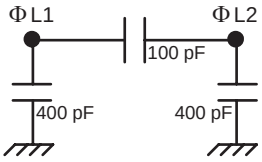
See “Pin-out/Pin Designation” on page 23.

Table 1. DC Characteristics

Parameter	Min.	Typ.	Max.	Notes
$V_{S\ (1\ to\ 4)}$		0V		
$V_{DD\ (1\ to\ 4)}$	14.5V	15V	15.5V	
V_{SS}	0V	0V		
$V_{GS\ (1\ to\ 4)}$	3.7	4V	4.3V	2V for MPP mode (option)
$V_{DR\ (1\ to\ 4)}$	13V/14.5V(1)	13.5V/15V(1)	14V/15.5V(1)	
$V_{DE\ (A\ and\ B)}$	5.5V	6V	6.5V	
$V_{GL\ (1\ to\ 4)}$	0.7V/11.7V(1)	1V/12V(1)	1.3V/12.3V(1)	0V/12V for MPP mode (option)

Note: 1. $V_{G\,L}$ = 12V and V_{DR} = 15V is only when using a summing mode to optimize saturation level.
The reference level (V_S) of an unused output amplifier can be disconnected to avoid the consumption of this amplifier.

Table 2. Drive Clock Characteristics

Parameter	Min.	Typ.	Max.	Notes
$\Phi_{P1,2,4}$				For each A,B,C and D zones, the capacitances to drive are: CΦP1 = CΦP3 = 10 nF CΦP2 = CΦP4 = 13 nF
Low	-11V	-9V	-8.5V	
High	+3.5V	+4V	+4.5V	
Φ_{P3}				
Low	-11V	-9V	-8.5V	
High	0V	0.3V	0.6V	
ΦT (A and B)				CΦTA = CΦTB < 100 pF
Low	-11V	-9V	-8.5V	
High	+3.5V	+4V	+5V	
ΦL				-8V for MPP mode (option) +3V for MPP mode (option) For each A and B readout register and after having tied the different clocks in two clocks ΦL1 and ΦL2 and in the non MPP mode (in the MPP mode the ΦL clock capacitances are roughly 30% higher) 
Low	-2.5V	-3V	-3.5V	
High	+5.5V	+6V	+6.5V	
ΦS (1 to 4)				-8V for MPP mode (option) +3V for MPP mode (option) For each summing gate: CΦS < 50 pF
Low	-2.5V	-3V	3.5V	
High	+5.5V	+6V	+6.5V	
ΦR (1 to 4)				For each reset gate: CΦR < 20 pF
Low	0V	0.3V	0.6V	
High	+9V	+10V	+11V	

Main Operating Modes and Selection Table for Vertical Transfer Number (vnb) and for Horizontal Transfer Number (hnb)

VERTICAL TRANSFERS

2080 TRANSFERS MINIMUM	2080 TRANSFERS MINIMUM	1040 TRANSFERS MINIMUM	1560 TRANSFERS MINIMUM	1040 TRANSFERS MINIMUM	520 TRANSFERS MINIMUM
vnb=2080	vnb=2080	vnb=1040	vnb=1560	vnb=1040	vnb=520
MODES 1-2-13 : PA1= PB1= PC1= PD1= A PA2= PB2= PC2= PD2= B PA3= PB3= PC3= PD3= C PA4= PB4= PC4= PD4= D TA=Low level TB= A	MODES 3-4-14 : PA1= PB1= PC1= PD1= A PA2= PB2= PC2= PD2= D PA3= PB3= PC3= PD3= C PA4= PB4= PC4= PD4= B TA= A TB=Low level	MODES 5-6-15 : PA1= PB1= PC1= PD1= A PA4= PB4= PC2= PD2= B PA3= PB3= PC3= PD3= C PA2= PB2= PC4= PD4= D TA= A TB= A	MODES 7-8-16 : PA1= PB1= PC1= PD1= A PA4= PB2= PC2= PD2= B PA3= PB3= PC3= PD3= C PA2= PB4= PC4= PD4= D TA= A TB= A	MODES 9-10-17 : PA1= PB1= MA PC1= PD1= PA **PA4= PB4= MB** **PC4= PD4= PB** PA3= PB3= MC PC3= PD3= PC **PA2= PB2= MD** **PC2= PD2= PD** TA= MA TB= PA (or low level)	MODES 11-12-18 : PA1= PD1= MA PC1= PB1= PA **PA4= PD2= MB** **PC2= PD4= PB** PA3= PD3= MC PC3= PB3= PC **PA2= PD4= MD** **PC4= PB2= PD** TA= MA TB= MA

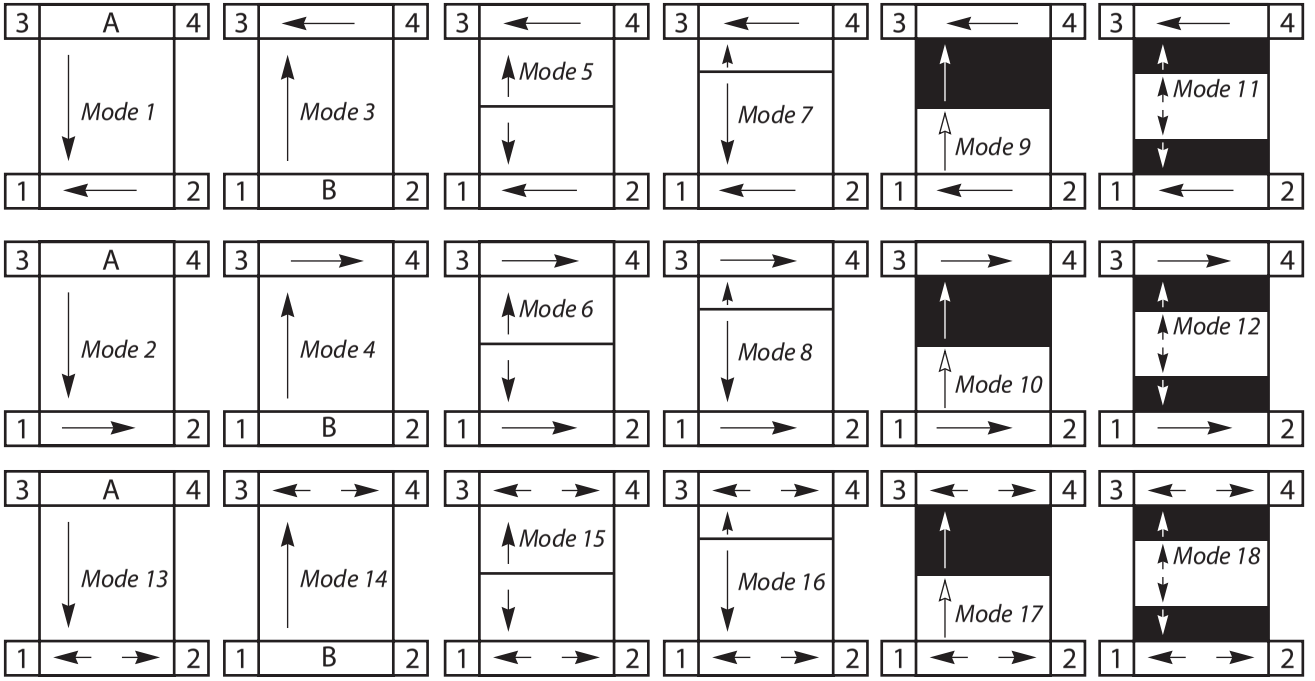
A, B, C, and D correspond to the clocks described in the timing diagram page 10 in case of full frame timing.

PA, PB, PC, PD, MA, MB, MC, MD correspond to the clocks described in the timing diagram page 13 in case of frame transfer timing with memory zone.

L1, L2, correspond to the clocks described in the timing diagram page 10.

vnb and hnb are respectively the vertical transfer number and the horizontal transfer number which shall be repeated in the timing diagram described page 10.

The unused horizontal clocks (L, S, R) shall be stated to their high level.



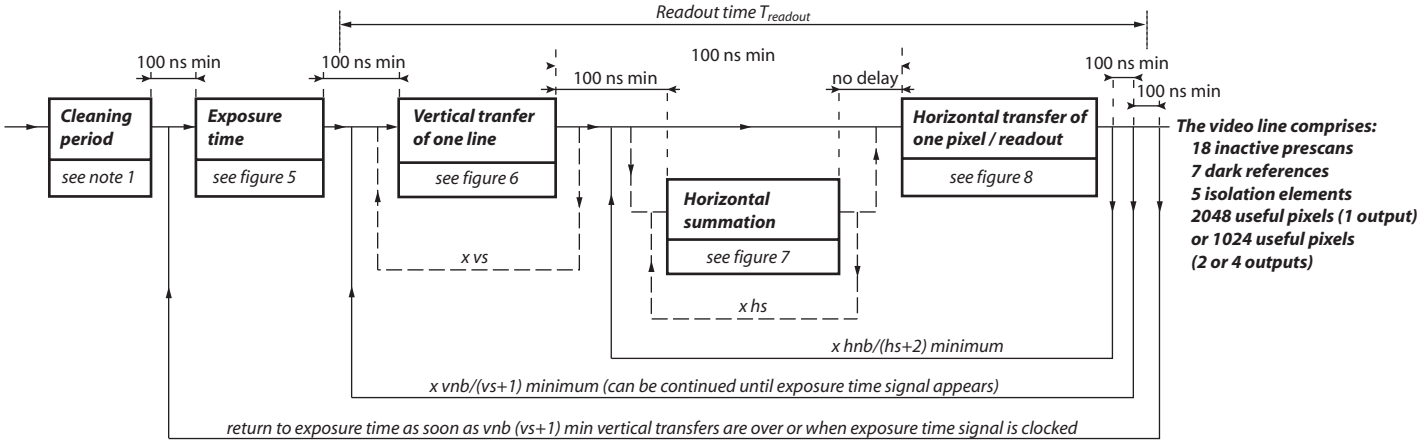
Only when using specific device with optical shield (on request)

2078 PIXEL PERIODS	2078 PIXEL PERIODS	1054 PIXEL PERIODS
hnb=2078	hnb=2078	hnb=1054
MODES 3-5-7-9-11 : LA1= LA4= LA5= L1 LA2= LA3= LA6= L2 MODES 1-5-7-9-11 : LB1= LB4= LB5= L1 LB2= LB3= LB6= L2	MODES 4-6-8-10-12 : LA1= LA3= LA6= L1 LA2= LA4= LA5= L2 MODES 2-6-8-10-12 : LB1= LB3= LB6= L1 LB2= LB4= LB5= L2	MODES 14-15-16-17-18 : LA1= LA3= LA5= L1 LA2= LA4= LA6= L2 MODES 13-15-16-17-18 : LB1= LB4= LB6= L1 LB2= LB3= LB5= L2

HORIZONTAL TRANSFERS

Timing Diagram

Full Frame Timing Diagram (Without Memory Zone)



Summation options:

vs = number of vertical summation (vs = 1 to sum 2 lines in the readout register),

hs = number of horizontal summation (hs = 0 to sum 2 pixels in the ϕS gate, only add the timing diagram once of figure 10),

vnb and hnb are defined according to the chosen operating mode in “” on page 9.

Note: 1. Cleaning period consists of emptying the image zone of all charges created by thermal generation. To achieve such cleaning, the readout time Treadout defined in the above diagram shall be used. Nevertheless, it is possible to reduce cleaning time of the image zone by accumulating several lines in the output register (Figure 7) before reading out the resulting signal (Figure 9). The number of accumulated lines is limited by the readout register saturation level.

Figure 6. Exposure Time

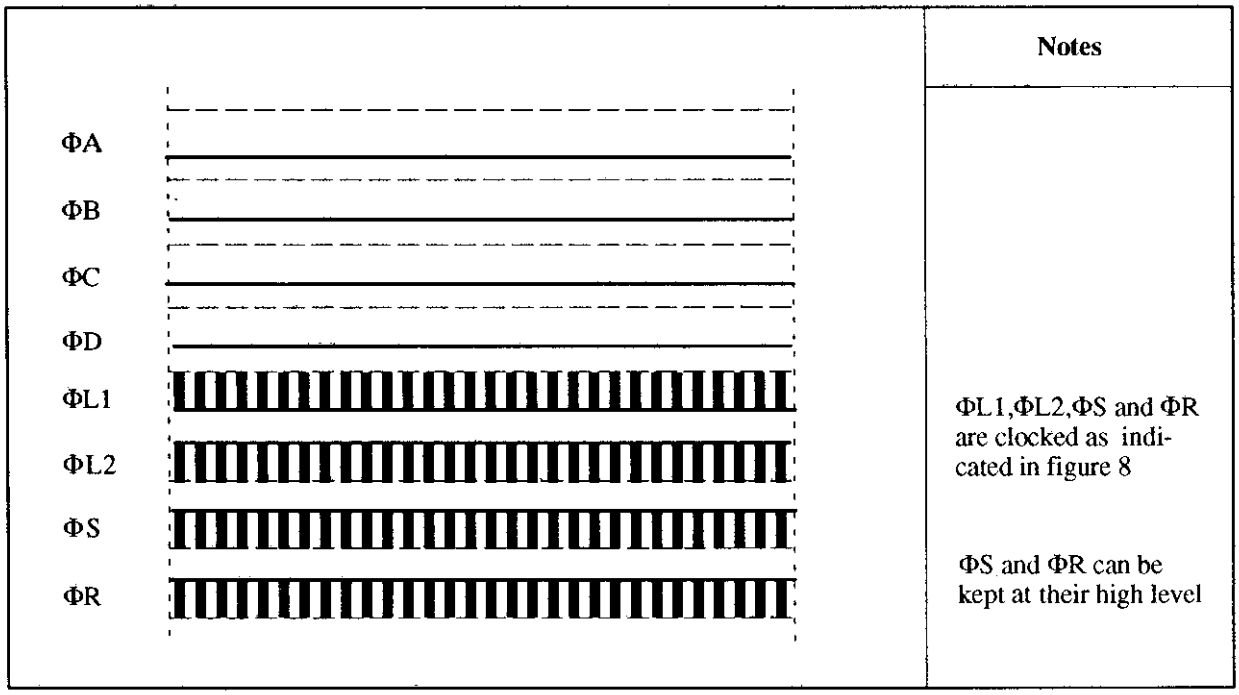


Figure 7. Vertical Transfer of One Line

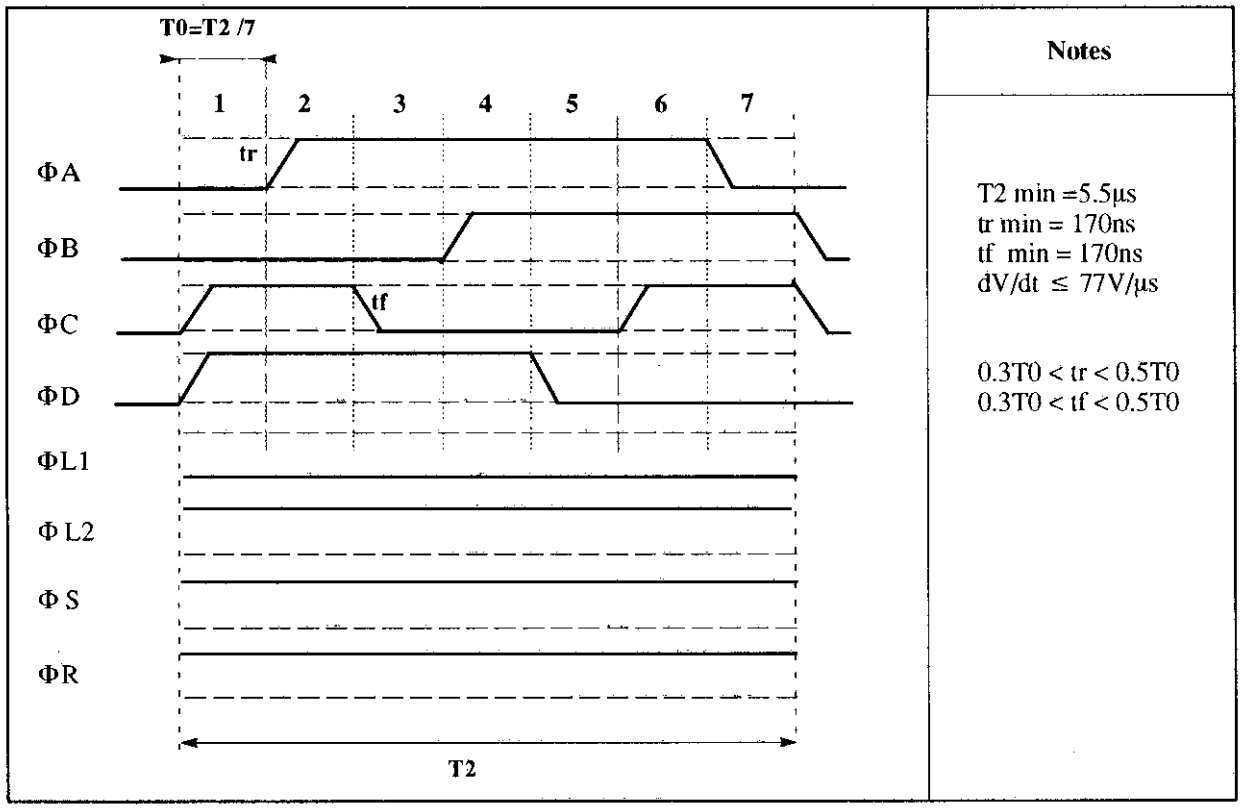


Figure 8. Horizontal Pixel Summation on ΦS Gate (Two Adjacent Pixel Summation)

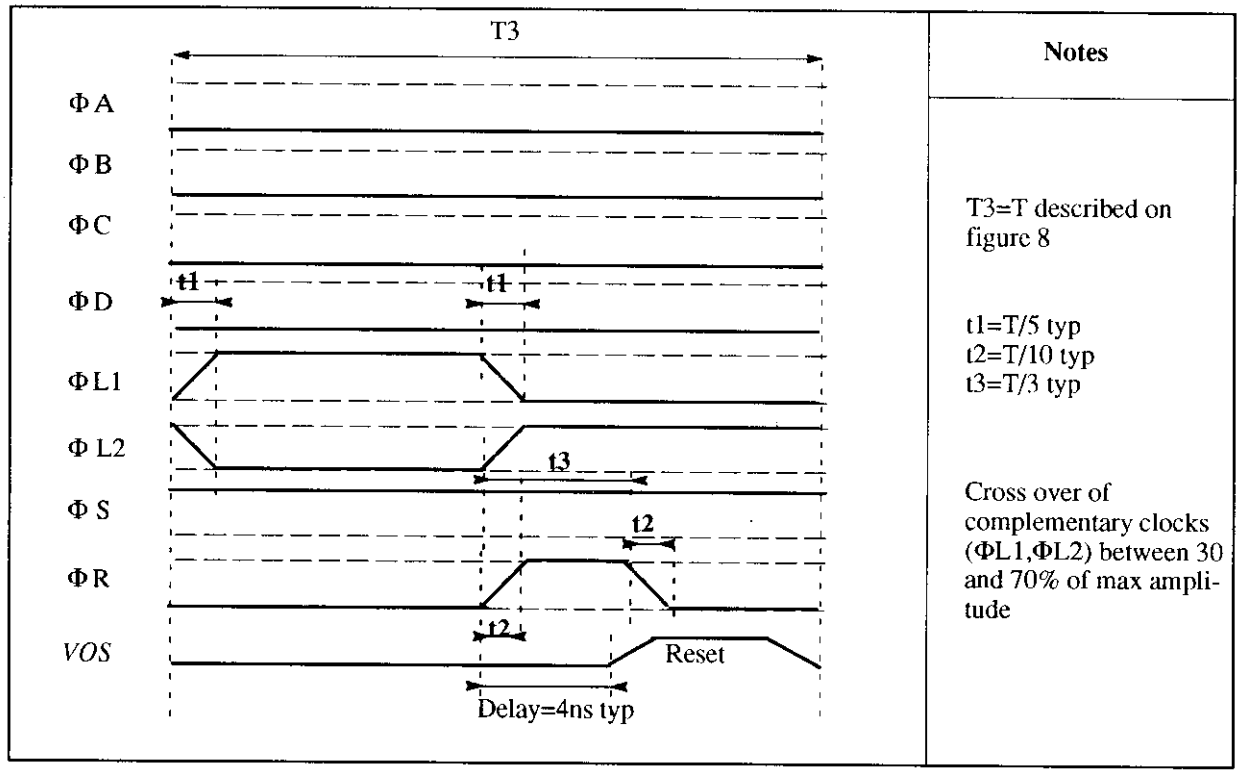
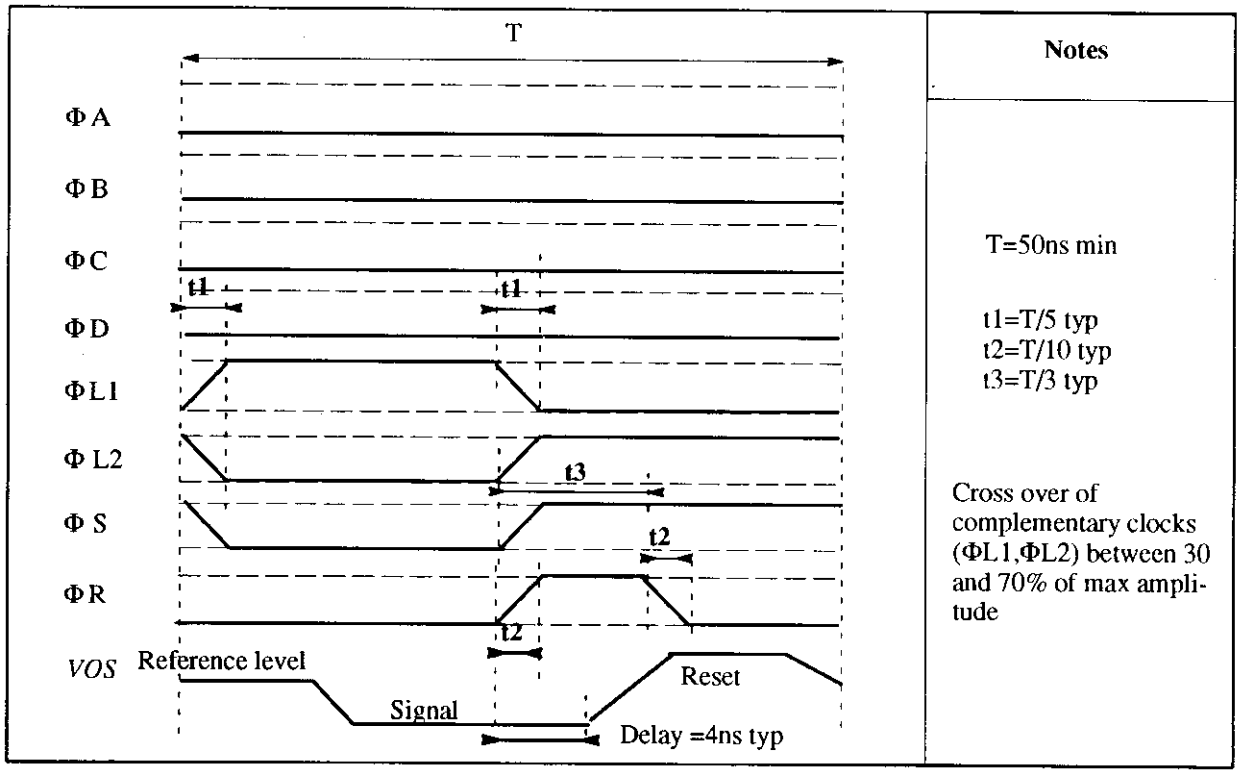
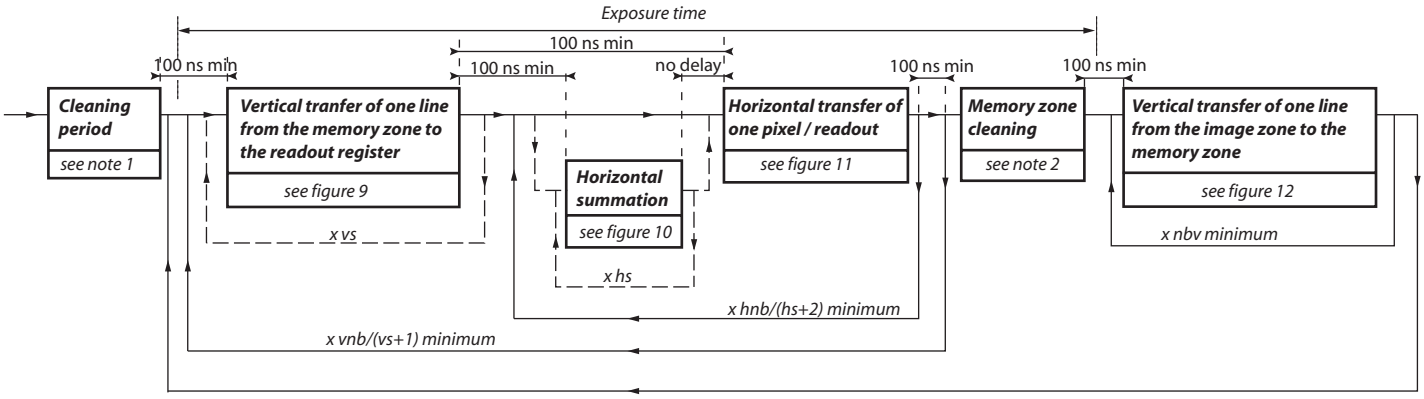


Figure 9. Horizontal Transfer Period and Readout



Frame Transfer Timing (With Memory Zone(s))



The video line comprises:

- 18 inactive prescans
- 7 dark references
- 5 isolation elements
- 2048 useful pixels (readout through one output) or 1024 useful pixels (readout through 2 or 4 outputs)

Summation options:

vs = number of vertical summation (vs = 1 to sum 2 lines in the readout register),

hs = number of horizontal summation (hs = 0 to sum 2 pixels in the ϕS gate, only add the timing diagram once of figure 10),

vnb and hnb are defined according to the chosen operating mode in “” on page 9.

Notes:
1. Cleaning period consists of emptying the image zone of all charges created by thermal generation. To achieve such cleaning, the vertical transfer of all of the image zone to the memory zone shall be clocked according to the diagram shown in figure 12.
2. Memory zone cleaning period consists of emptying the memory zone of all charges created by thermal generation. To achieve such cleaning, the vertical transfer from the memory zone to the readout register shall be clocked according to the diagram shown in figure 9. Nevertheless, it is possible to reduce cleaning time of the memory zone by accumulating several lines in the readout register (figure 9) before reading out the resulting line signal (see figure 11). The number of accumulated lines is limited by the output register saturation level.

Figure 10. Vertical Transfer of One Line From the Memory Zone to the Readout Register

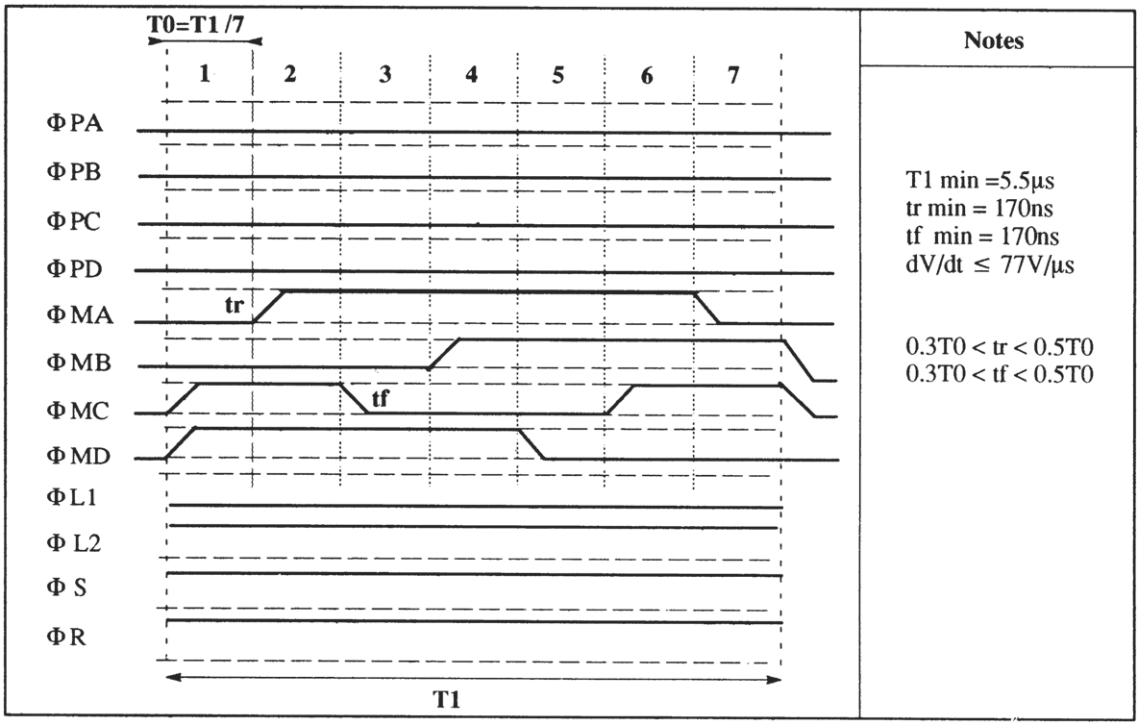


Figure 11. Horizontal Pixel Summation on ΦS Gate (Two Adjacent Pixel Summation)

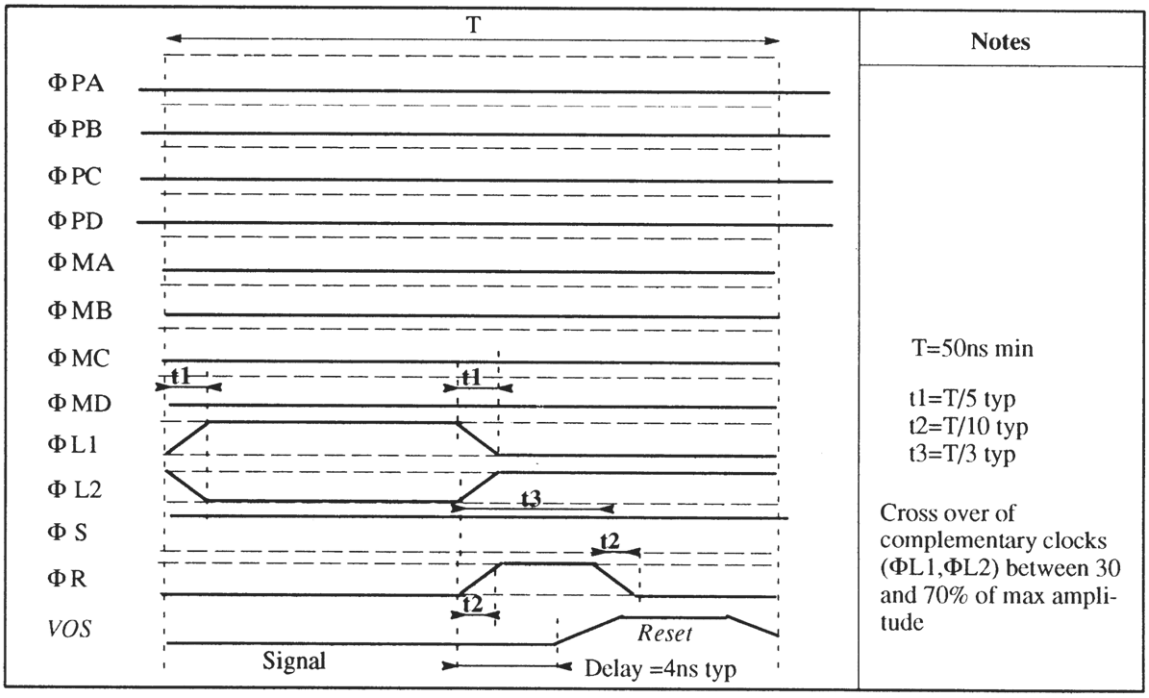


Figure 12. Horizontal Transfer Period and Readout

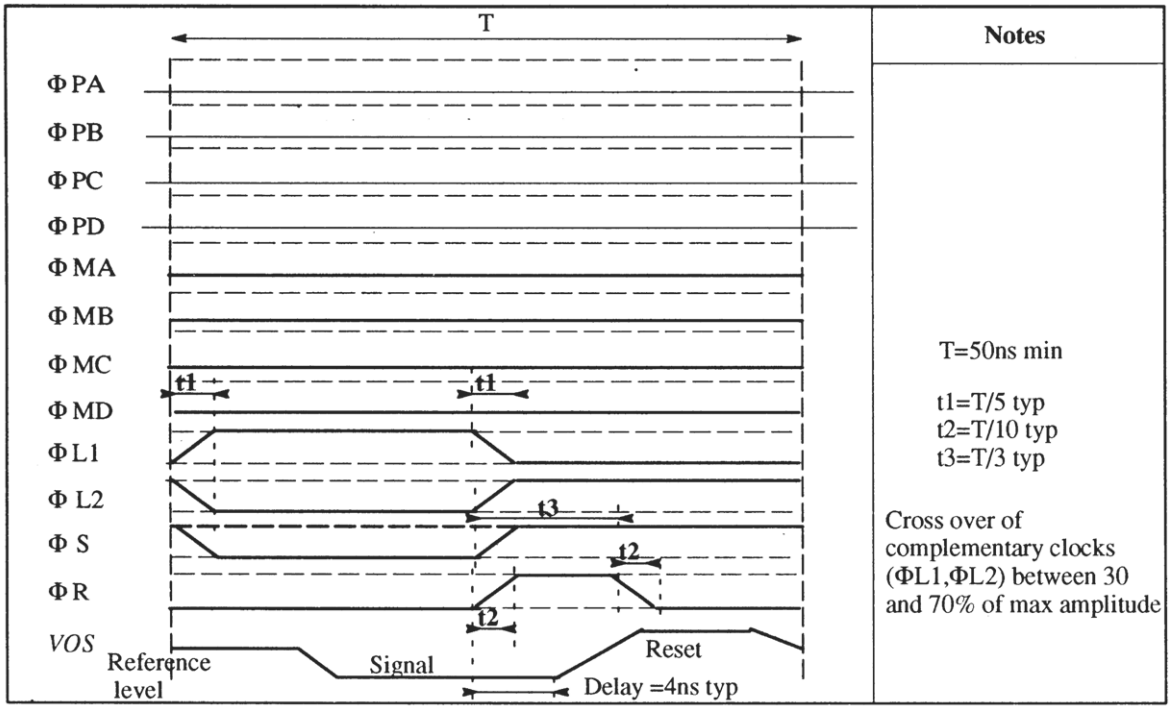
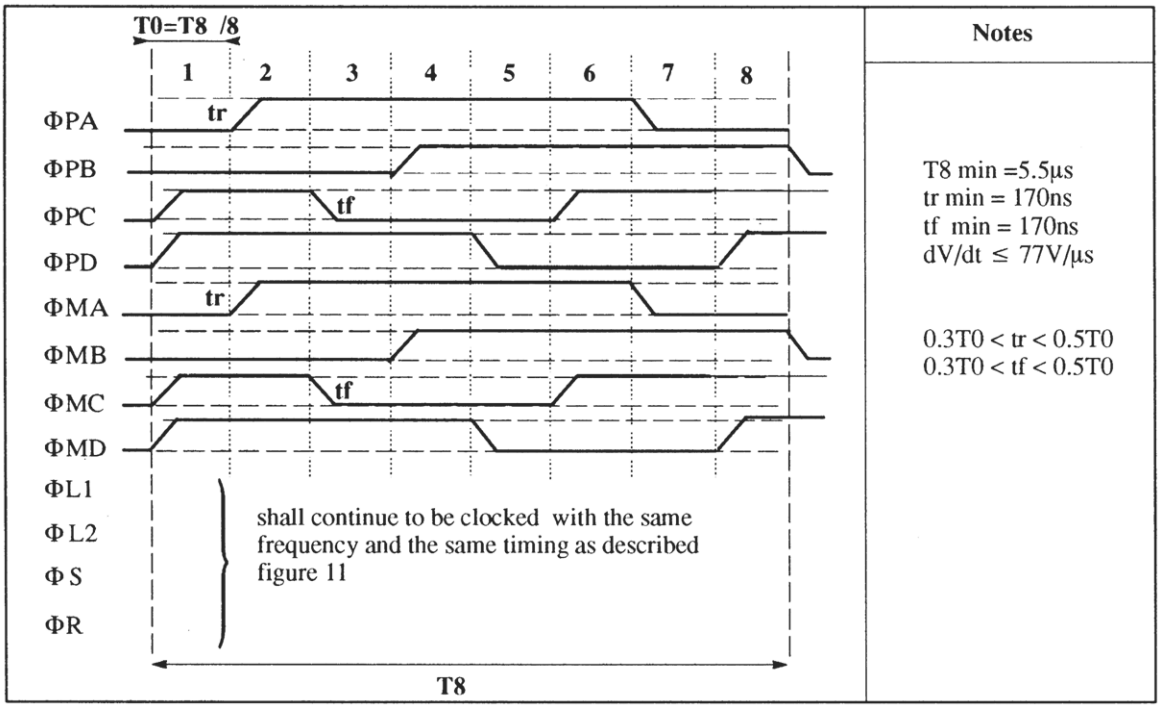


Figure 13. Vertical Transfer of One Line from the Image Zone to the Memory Zone



Electrical Performance

Table 3. Static And Dynamic Electrical Characteristics

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
DC Output Level(1)	Vref		10.5		V	VDR = 13.5V; VS = 0V
Output Impedance(1)	Zout	200	230	250	Ω	
Output Amplifier Supply Current(2)	IDD		10		mA	VDD = 15V; VDR = 13.5V; VS = 0V
Charge to Voltage Conversion Factor						
With VGL = 1V and VDR = 13.5V	CVF1	6.6	7	7.4	µ V/e-	For Standard Mode
With VGL = 12V and VDR = 15V	CVF2	4.2	4.5	4.7	µ V/e-	For Binning Mode
Image Zone To Readout Register Frequency	FV		100	180	kHz	Without Reduction Of Saturation Charge
Readout Register And Reset Frequency	FH		5	20	MHz	

Notes: 1. Measured on VOS1 VOS2 VOS3 and VOS4.
2. Measured in each VDD pin.

Electrooptical Performance

General measurement conditions (unless specified):

- TC = 25°C (package temperature).
- Vertical transfer frequency FV = 100 kHz.
- Horizontal transfer frequency and output frequency FH = 5 MHz.

Illumination conditions:

- 3200K halogen lamp + 2 mm BG38 filter + F/3.5 aperture.

Table 4. Electro-optical Performance Characteristics

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Saturation Output Voltage						
Without Binning	VSAT	1.4	1.9		V	(1)
Saturation Charge of Elementary Pixel						
Without Binning	QSAT	220	270		ke-	(1)
Saturation Charge of Readout Registers		320	360		ke-	(2)
Saturation Charge of Summing Gates ΦS		550	630		ke-	(2)
Saturation Level on the Output Node						(3)
With VGL = 1V and VDR = 13.5V		280	300		ke-	For Standard Mode
With VGL = 12V and VDR = 15V		530	570		ke-	For Binning Mode

Table 4. Electro-optical Performance Characteristics (Continued)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Rms Output Amplifier Noise						(4)
With a Bandwidth of 80MHz	N1		20		e-	Output Frequency = 20 MHz
With a Bandwidth < 5MHz	N2		5		e-	Output Frequency < 1 MHz
Dark Current						
MPP Mode	I01		25	30	pA/cm^2	T = 25°C
Non MPP Mode	I02		0.6	1	nA/cm^2	T = 25°C
Dynamic Range Exposure Time =10 ms Readout Time = 2s, FV = 100 kHz Readout Through One Output	SNR		9800			T = 25°C, Without Binning(5)
Photo-response Non Uniformity, σ	PRNU		1	2.5	% $\overline{VOS}$	
Dark Signal Non Uniformity, σ Exposure Time = 10 ms, Readout Time = 2s, FV = 100 kHz Readout Through One Output	DSNU		2.2	3	mV	T = 25°C
Horizontal Transfer Efficiency	1 -εH	0.99993	0.99997			(6)
Vertical Transfer Efficiency	1 -εV	0.99998	0.99999			
Contrast Transfer Function at Nyquist Frequency	CTF		67		%	
Responsivity	R		8.5		V/µJ/cm^2	With BG38 Filter
Linearity Error	LE		< 1		%	Without Binning
Flatness (Peak To Peak)			13	20	µm	

Notes:
1. Saturation level is the maximum charge level before vertical transfer efficiency degradation (out of specification).
2. Saturation level is the maximum charge level before horizontal transfer efficiency degradation (out of specification).
3. Saturation level on output node can be optimized by running the readout register in MPP mode. Nevertheless, such a method implies that the capacitances of the ΦL clocks are roughly 30% higher.
4. Measured with the Correlated Double Sampling (CDS).
5. Dynamic range is defined by the ratio of the saturation level to the temporal rms noise in darkness.
6. With a horizontal frequency maximum of 20 MHz, this value will be improved when decreasing this frequency.

Figure 14. Typical Spectral Response

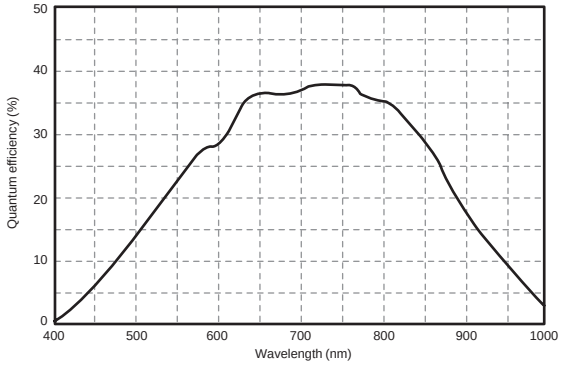
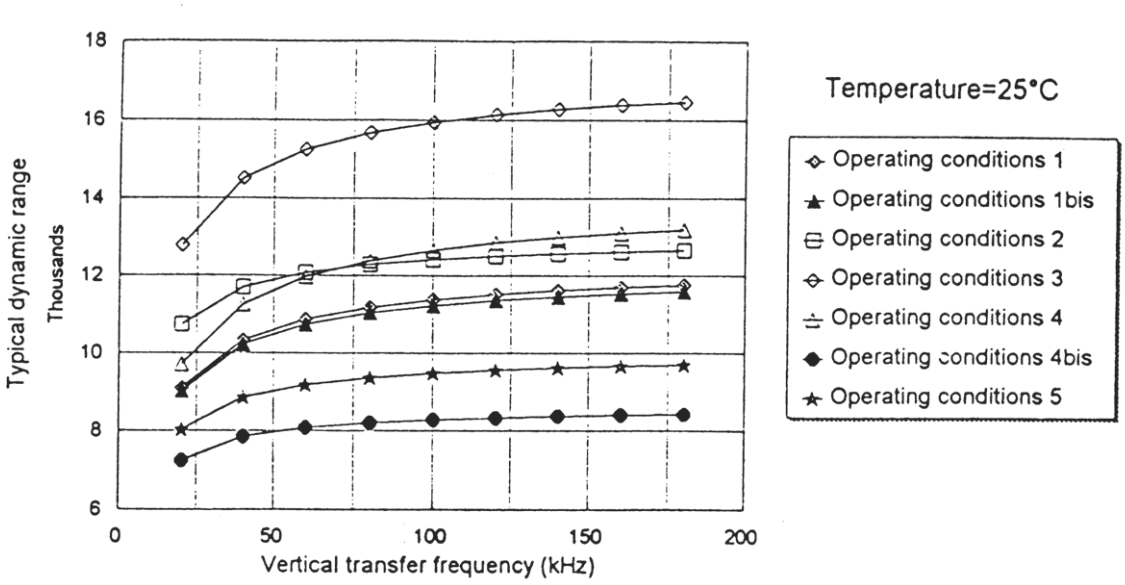


Figure 15. Typical Dynamic Range for Different Operating Conditions



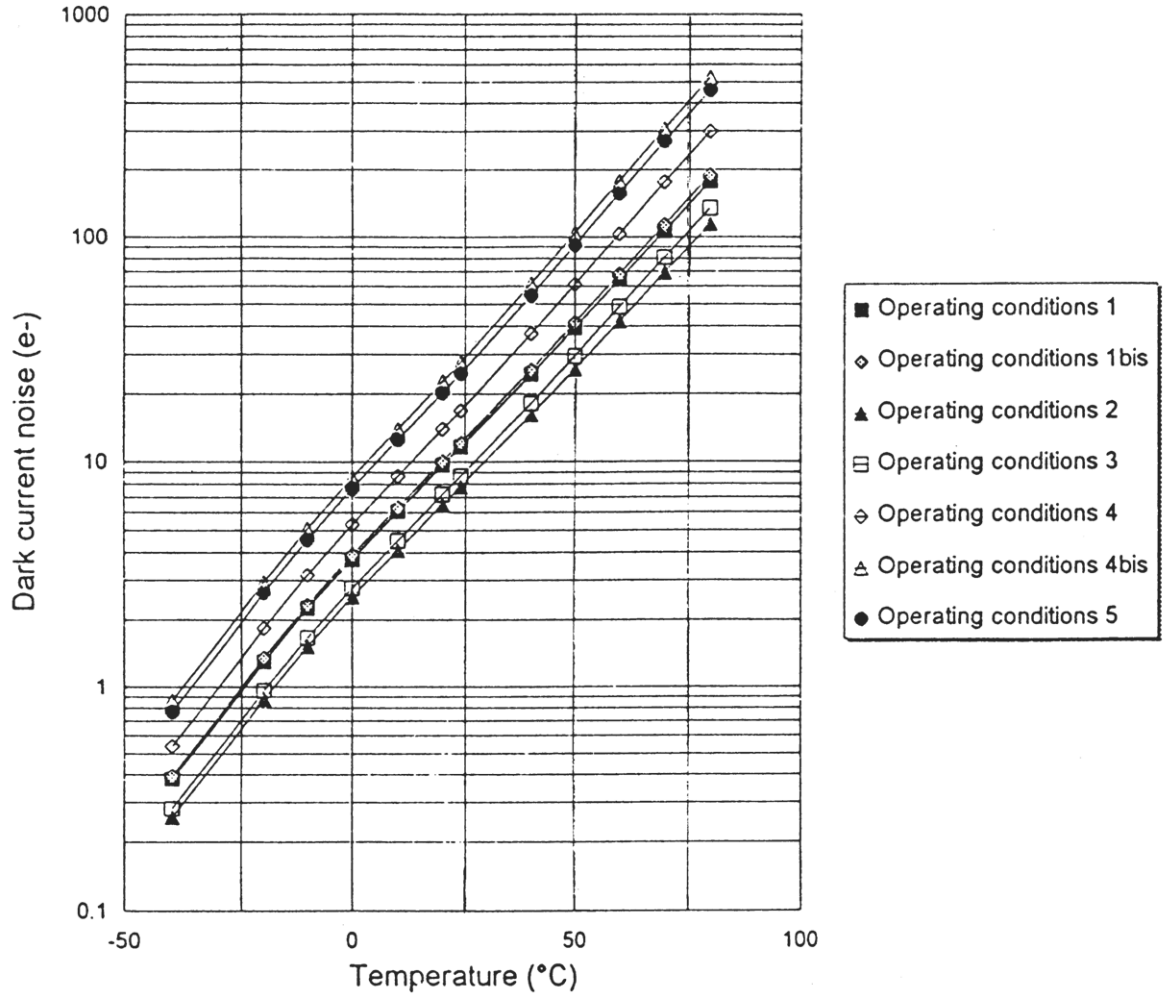
The dynamic range is defined by the ratio of the saturation level to the temporal rms noise in darkness.

The increase of dynamic range with the vertical frequency is due to the reduction of dark current when the vertical frequency increases (in particular reduction of transfer time where the device is no longer in the MPP mode).

Operating Mode	Number of Used Outputs	Output Frequency (MHz) per Output	Exposure Time (ms)
Conditions 1	1	20	50
Conditions 1bis	1	20	100
Conditions 2	4	20	50
Conditions 3	4	10	50
Conditions 4	1	5	10
Conditions 4bis	1	5	2000
Conditions 5	1	2	10

For output frequencies lower than 20 MHz/output, it is recommended to cut-off the output amplifier bandwidth by means of an off chip capacitance so as to minimize amplifier noise. To do so the output amplifier bandwidth has to be adjusted at 5 times the output frequency. The results given above take into account this optimization of amplifier noise.

Figure 16. Typical Dark Current Noise with Respect to the Temperature for Different Operating Conditions



All results have been calculated with a vertical frequency of 100 kHz.

Operating Mode	Number of Used Outputs	Output Frequency (MHz) per Output	Exposure Time (ms)
Conditions 1	1	20	50
Conditions 1bis	1	20	100
Conditions 2	4	20	50
Conditions 3	4	10	50
Conditions 4	1	5	10
Conditions 4bis	1	5	2000
Conditions 5	1	2	10

Preliminary Image Grade Specifications

Image quality grades are available:

- Grade H, ordering code TH7899MCRH
- Grade T, ordering code TH7899MCRT
- Grade E, ordering code TH7899MCRE

These image quality grades are guaranteed at 25°C and provide a good image for applications at ambient temperature.

Operating temperature range: 0°C to = 70°C.

Blemish Definition

- Column:

  It is one pixel in width and ≥ 7 pixel high defect whose height is constant with light level.

- Blemish:

  There are usually three types of blemishes:

  – White defect, dependent on temperature, as dark signal: its amplitude doubles for every 8 to 10°C temperature rise.

  – Black defect, not dependent on temperature, but whose amplitude is proportional to the mean output voltage.

  White defects are specified in darkness, at +25°C

  Black defects are specified under illumination, as a percentage of mean illumination up to VSAT/2 min independently of temperature.

  Traps are specified as defects (white + black) in darkness, at +25°C.

Image Grade Specifications

α is the amplitude of video signal of blemishes.

Eg: 20% < α

For amplitude < 20%, pixel is not a blemish.

Z1 is a square area, whose side is half of the height of the image zone, centered in the image zone.

Z2 is the rest of the image zone.

Image grade is measured on VOS output signal, with 4 outputs operating mode (1s integration time in darkness, 100 kHz vertical frequency and 5 MHz horizontal frequency).

Illumination conditions: 3200K Halogen lamp + BG38 filter + F/3.5.

H Grade

	Z1		**Z1 + Z2**	
Type (White to Black)	White defects in darkness at 25°C	Defects at VSAT/2	White defects in darkness at 25°C	Defects at VSAT/2
Pixels affected by blemishes Area maximum (pixels)	30 2x2		150 2x2	
Amplitude α	α > 40 mV	20%< | α|	α > 40 mV	20%< | α|
Column number maximum Amplitude α	0 α > 2 mV	0 10% < |α|	0 α > 2 mV	0 10% < |α|

T Grade

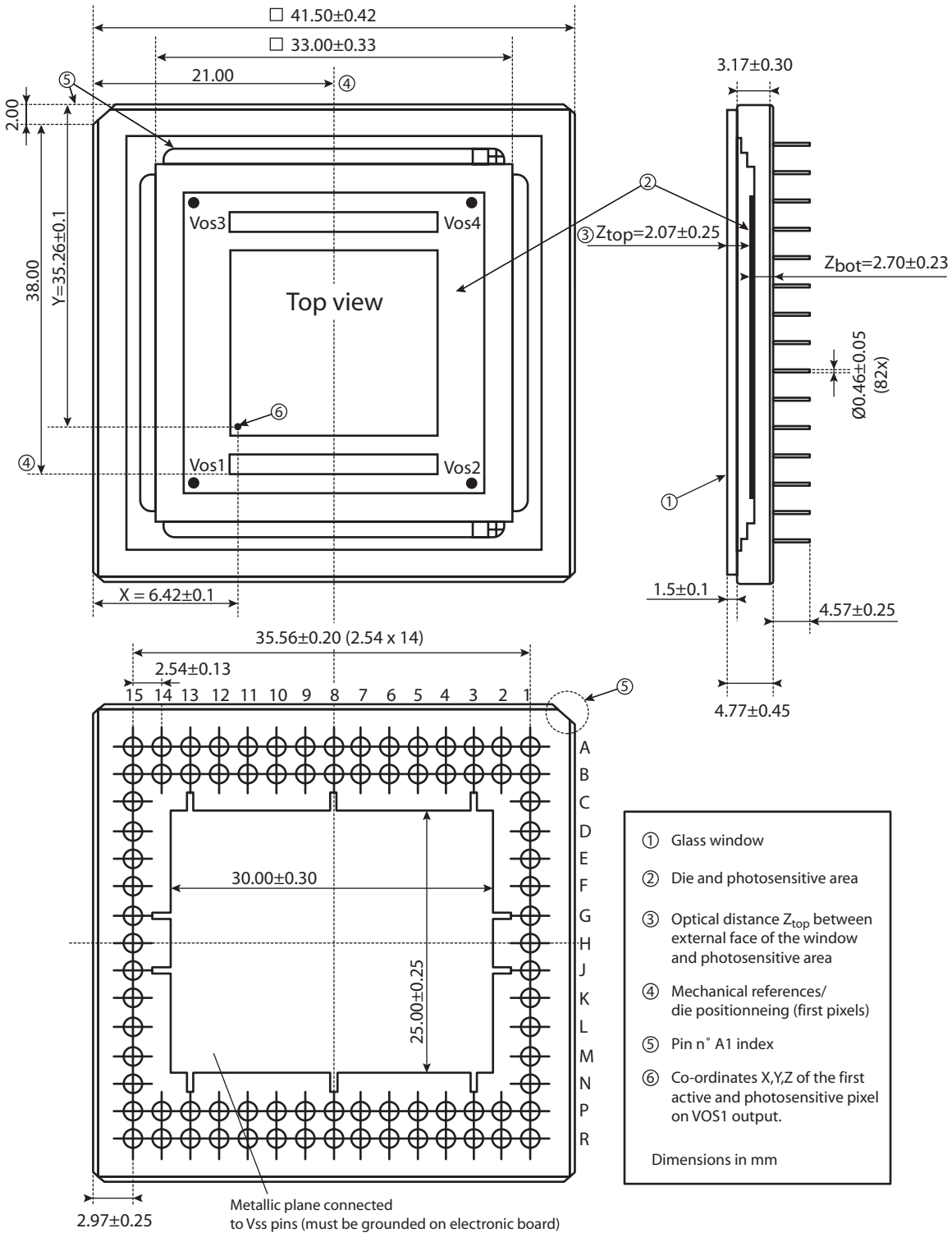
	Z1		Z1 + Z2	
Type (White or Black)	White defects in darkness at 25°C	Defects at VSAT/2	White defects in darkness at 25°C	Defects at VSAT/2
Pixels affected by blemishes Area maximum (pixels)	150 2x2		600 2x2	
Amplitude α	α > 40 mV	20% < |α|	α > 40 mV	20%< |α|
Column number maximum Amplitude α	0 α > 2 mV	5 10% < |α|	0 α > 2 mV	20 10% < |α|

E Grade

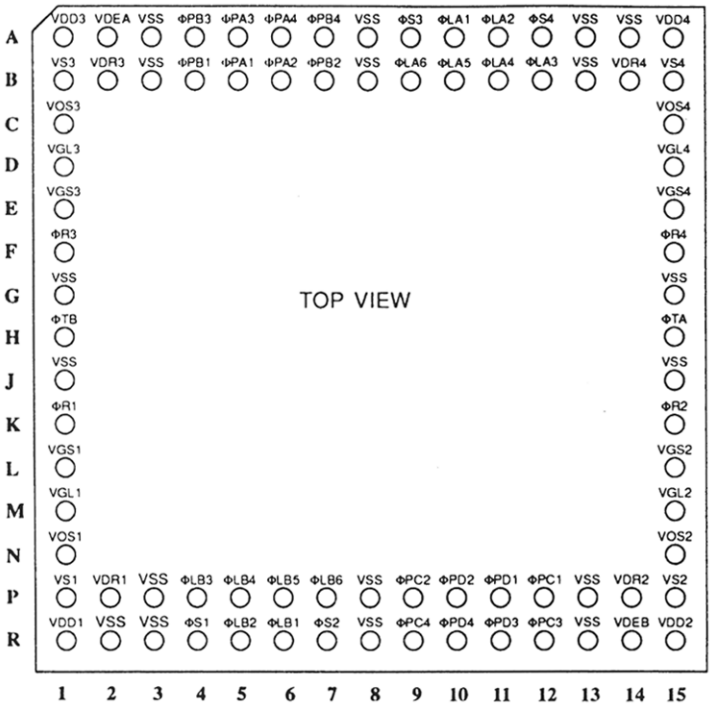
	Z1		Z1 + Z2	
Type (White or Black)	White defects in darkness at 25°C	Defects at VSAT/2	White defects in darkness at 25°C	Defects at VSAT/2
Pixels affected by blemishes Area maximum (pixels)	600 5x5		2000 5x5	
Amplitude α	α > 40 mV	20%< |α|	α > 40 mV	20%< |α|
Column number maximum Amplitude α	3 α > 2 mV	10 10% < |α|	10 α > 2 mV	40 10% < |α|

Outline Drawing

The chip center is located at package center.



Pin-out/Pin Designation



Pin n°	Symbol	Designation
R6, R5, P4, P5, P6, P7	ΦLB1, ΦLB2, ΦLB3, ΦLB4, ΦLB5, ΦLB6	B readout register clocks
A10, A11, B12, B11, B10, B9	ΦLA1, ΦLA2, ΦLA3, ΦLA4, ΦLA5, ΦLA6	A readout register clocks
R4, R7, A9, A12	ΦS1, ΦS@, ΦS3, ΦS4	Summing clocks of the output 1, 2, 3 and 4
M1, M15, D1, D15	VGL1, VGL2, VGL3, VGL4	Readout gate bias of the output 1, 2, 3 and 4
L1, L15, E1, E15	VGS1, VGS2, VGS3, VGS4	Output gate bias of the output 1, 2, 3 and 4
N1, N15, C1, C15	VOS1, VOS2, VOS3, VOS4	Output signal video 1, 2, 3 and 4
R1, R15, A1, A15	VDD1, VDD2, VDD3, VDD4	Output amplifier drain supply of the output 1, 2, 3 and 4
P1, P15, B1, B15	VS1, VS2, VS3, VS4	Output amplifier source bias of the output 1, 2, 3 and 4
K1, K15, F1, F15	ΦR1, ΦR2, ΦR3, ΦR4	Reset clocks of the output 1, 2, 3 and 4
P2, P14, B2, B14	VDR1, VDR2, VDR3, VDR4	Reset bias of the output 1, 2, 3 and 4
B5, B6, A5, A6	ΦPA1, ΦPA2, ΦPA3, ΦPA4	A image zone clocks
B4, B7, A4, A7	ΦPB1, ΦPB2, ΦPB3, ΦPB4	B image zone clocks
P12, P9, R12, R9,	ΦPC1, ΦPC2, ΦPC3, ΦPC4	C image zone clocks
P11, P10, R11, R10	ΦPD1, ΦPD2, ΦPD3, ΦPD4	D image zone clocks
H15, H1	ΦTA, ΦTB	Transfer gate from the image zone to the readout registers A and B respectively
A2, R14	VDEA, VDEB	Shield drain
A3, A8, A13, A14, B3, B8, B13, G1, G15, J1, J15, P3, P8, P13, R2, R3, R8, R13	VSS	Substrate bias

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