Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

IDT29FCT520AT/BT/CT/DT
IDT29FCT521AT/BT/CT/DT

FEATURES:

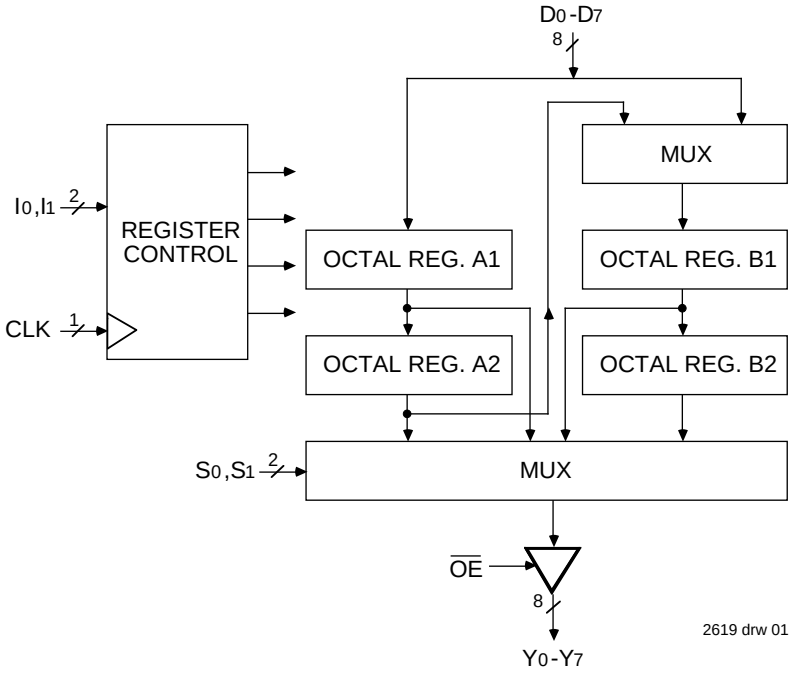
- A, B, C and D speed grades
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

DESCRIPTION:

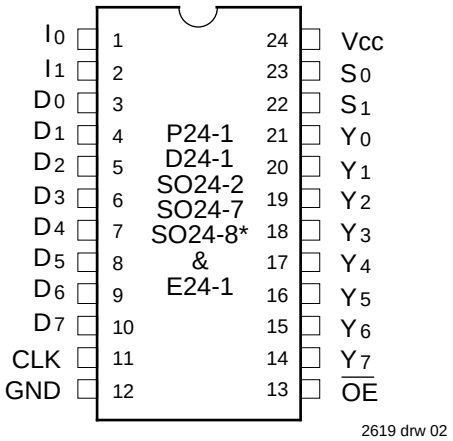
The IDT29FCT520AT/BT/CT/DT and IDT29FCT521AT/BT/CT/DT each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520AT/BT/CT/DT when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521AT/BT/CT/DT, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change. In either part I=3 is for hold.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



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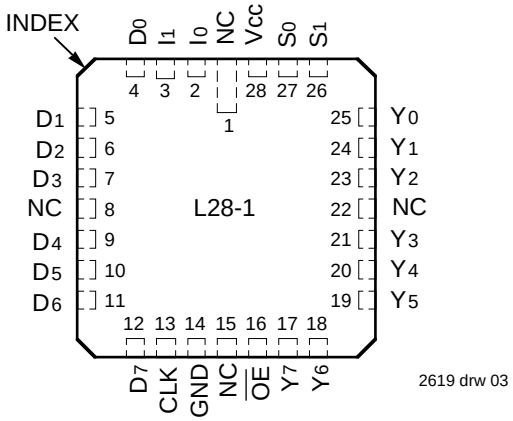
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

*FCT520 only



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LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

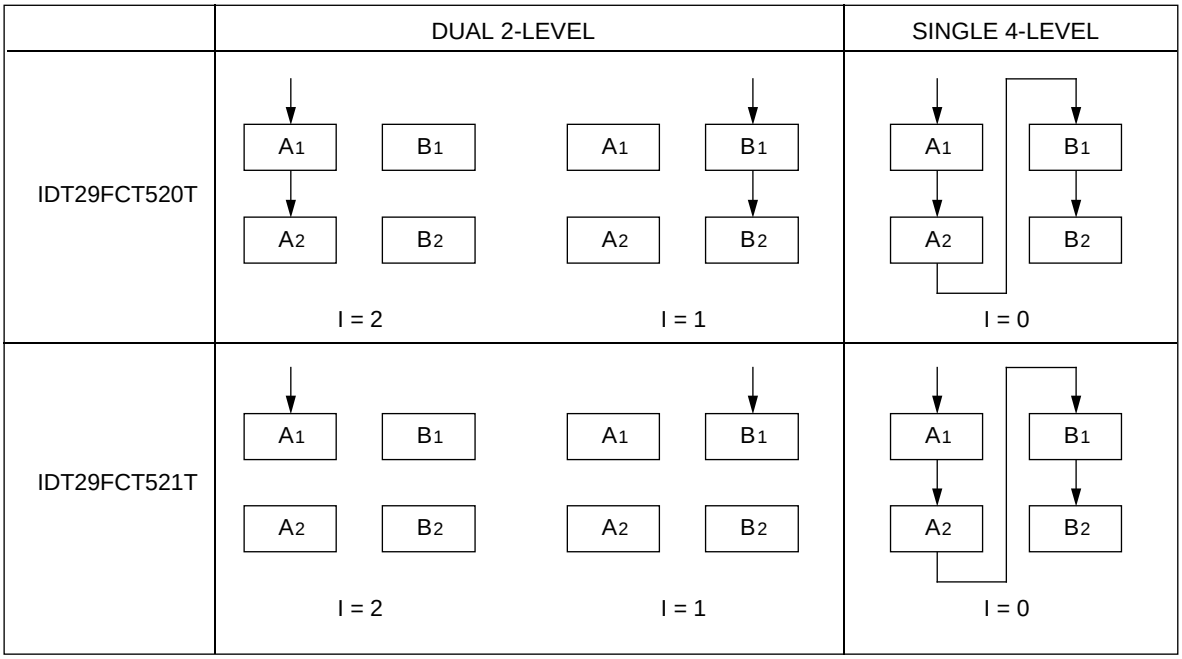
Pin Names	Description
D_n	Register input Port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
$\overline{OE}$	Output enable for 3-state output port.
Y_n	Register output port.

2619 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

2619 tbl 02



NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

2619 drw 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2619 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2619 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance(4)	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

NOTES: 2619 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current, TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

2619 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT520AT/521AT				FCT520BT/521BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Yn	C_L = 50pF R_L = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Yn		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW Dn to CLK		5.0	—	6.0	—	2.5	—	2.8	—	ns
t_H	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{SU}	Set-up Time, HIGH or LOW I_0 or I_1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	ns
t_H	Hold Time, HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	ns
t_W	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	ns

2619 tbl 07

Symbol	Parameter	Condition[1]	FCT520CT/521CT				FCT520DT/521DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Yn	C_L = 50pF R_L = 500Ω	2.0	6.0	2.0	7.0	2.0	5.2	—	—	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Yn		2.0	6.0	2.0	7.0	2.0	4.8	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW Dn to CLK		2.5	—	2.8	—	1.5	—	—	—	ns
t_H	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW I_0 or I_1 to CLK		4.0	—	4.5	—	2.0	—	—	—	ns
t_H	Hold Time, HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	6.0	1.5	6.0	1.5	4.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	6.0	1.5	7.0	1.5	4.0	—	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		5.5	—	6.0	—	3.0	—	—	—	ns

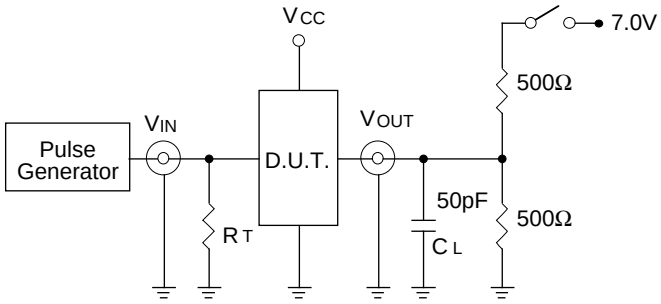
NOTES:

2619 tbl 08

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2619 drw 05

SWITCH POSITION

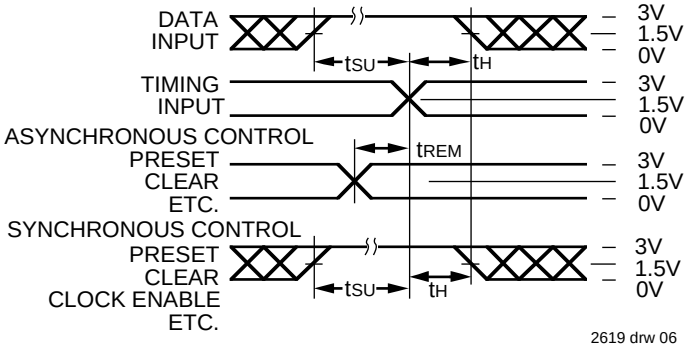
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2619 lnk 09

DEFINITIONS:

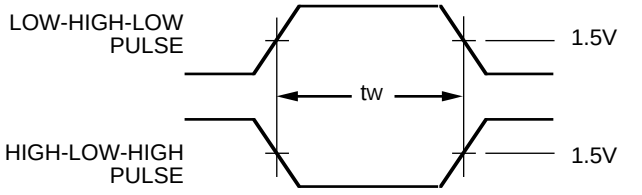
C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



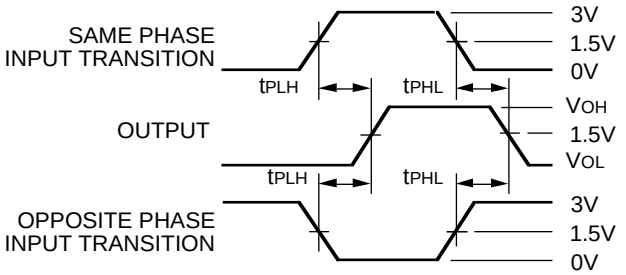
2619 drw 06

PULSE WIDTH



2619 drw 07

PROPAGATION DELAY



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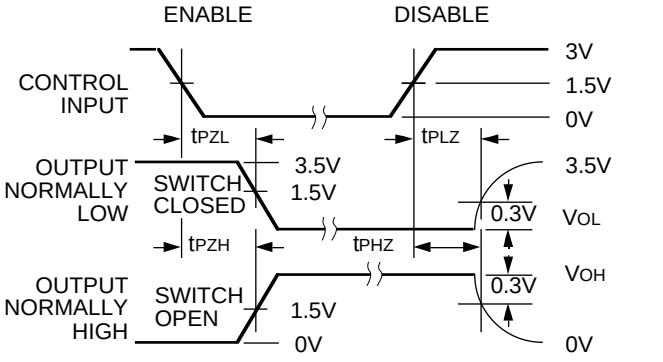
ENABLE AND DISABLE TIMES

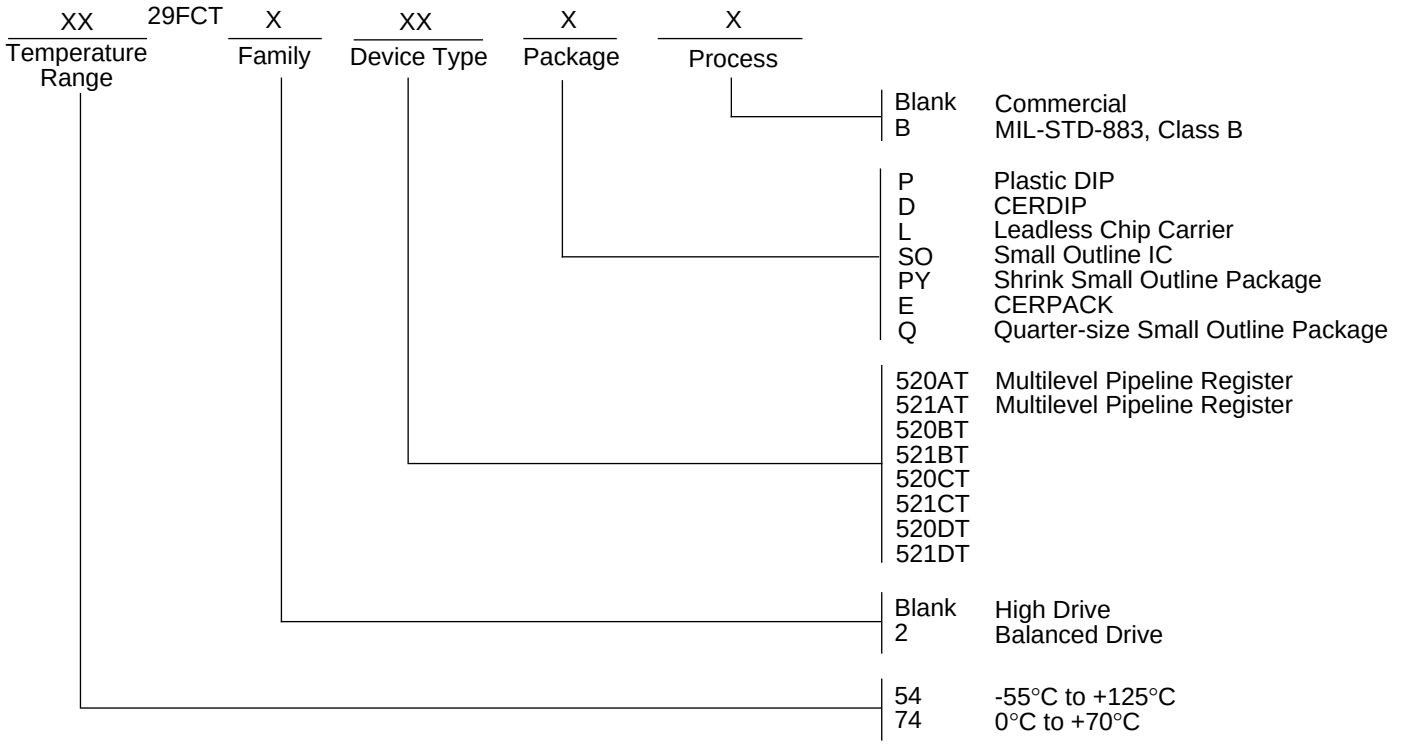


2619 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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