Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (128K x 8-BIT)

IDT71024S70

FEATURES:

- 128K x 8 CMOS static RAM
- Equal access and cycle times
  - — Commercial: 70ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 300 and 400 mil Plastic SOJ packages

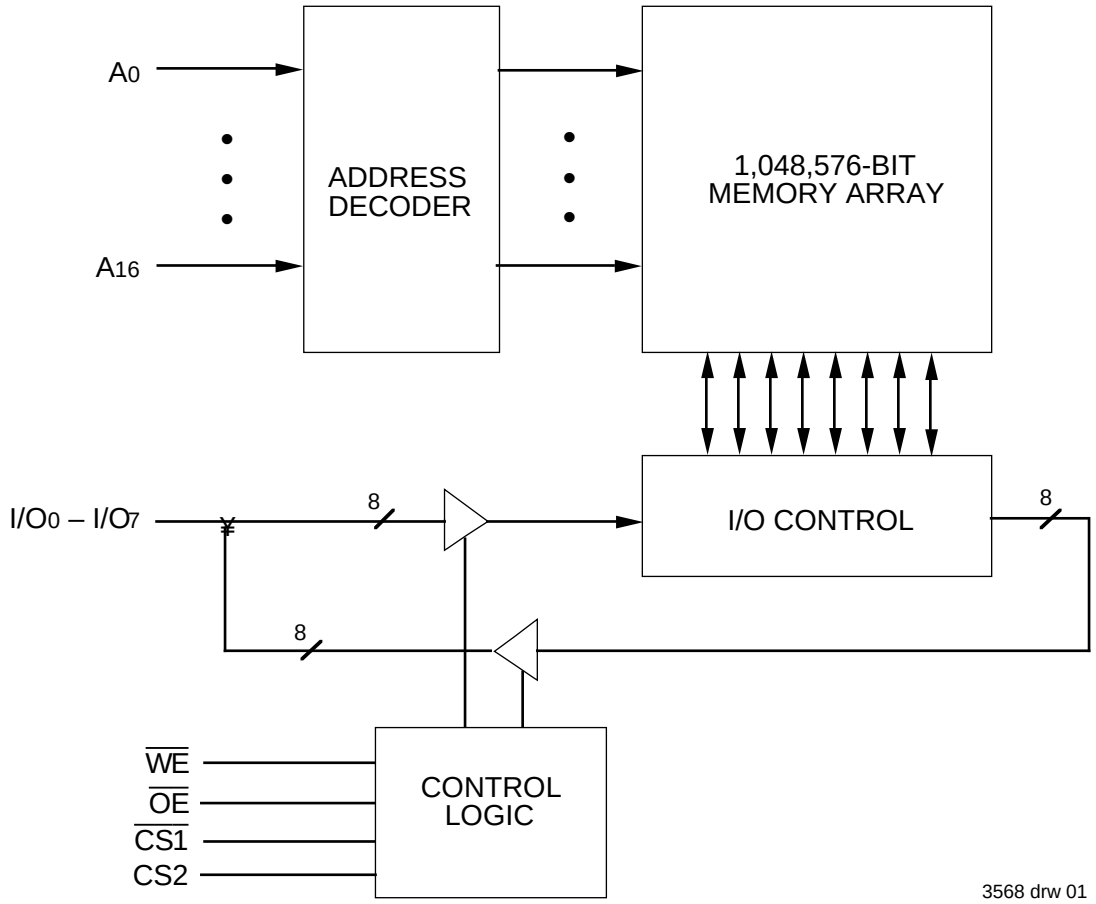
DESCRIPTION:

The IDT71024 is a 1,048,576-bit medium-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for your memory needs.

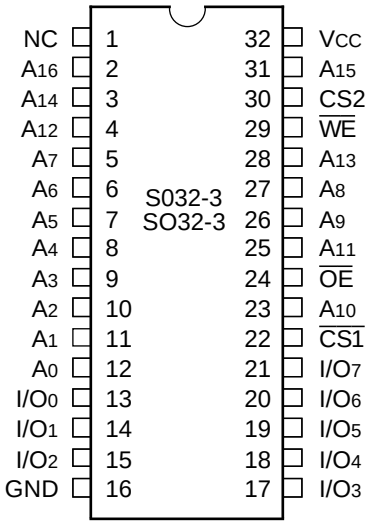
The IDT71024 has an output enable pin which operates as fast as 30ns, with address access times as fast as 70ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71024 is packaged in 32-pin 300 mil Plastic SOJ and 32-pin 400 mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



3568 drw 02

SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'L.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	StorageTemperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3568 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

INPUTS					
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	FUNCTION
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}(3)	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}(3)	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	$DATA_{OUT}$	Read Data
L	L	H	X	$DATA_{IN}$	Write Data

NOTES: 3568 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 3568 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3568 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71024		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3568 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71024S70 Com'l.	71024S70 Mil.	Unit
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	140	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	35	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC}, or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0(2), V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	10	—	mA

NOTES:
1.All values are maximum guaranteed values.
2.f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

3568 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3568 tbl 07

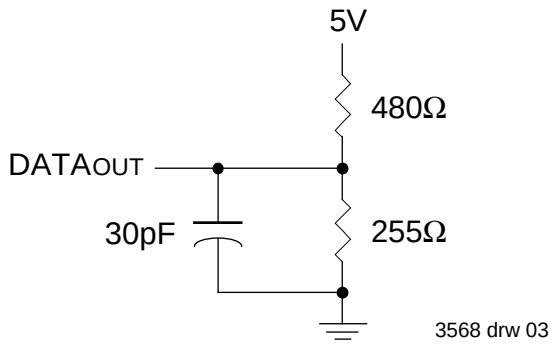
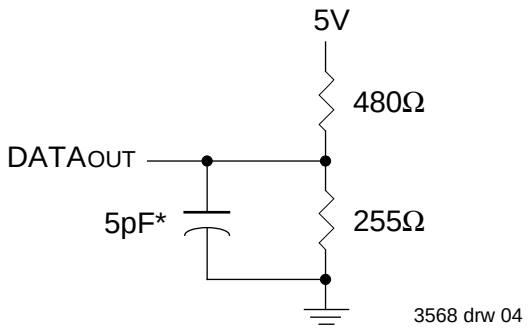


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

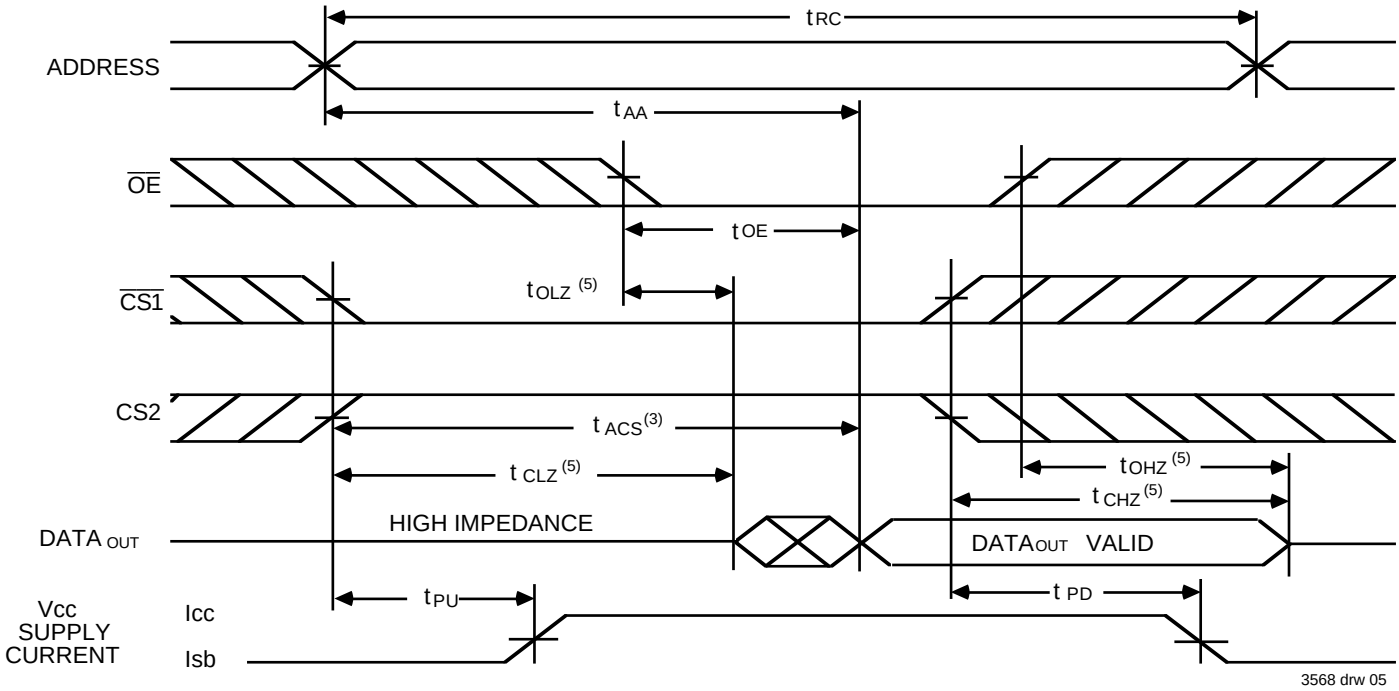
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, Commercial Temperature Range)

Symbol	Parameter	71024S70 Min.	71024S70 Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	70	—	ns
t_{AA}	Address Access Time	—	70	ns
t_{ACS}	Chip Select Access Time	—	70	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	3	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High-Z	0	30	ns
t_{OE}	Output Enable to Output Valid	—	30	ns
t_{OLZ}(2)	Output Enable to Output in Low-Z	0	—	ns
t_{OHZ}(2)	Output Disable to Output in High-Z	0	30	ns
t_{OH}	Output Hold from Address Change	4	—	ns
t_{PU}(2)	Chip Select to Power-Up Time	0	—	ns
t_{PD}(2)	Chip Deselect to Power-Down Time	—	70	ns
Write Cycle				
t_{WC}	Write Cycle Time	70	—	ns
t_{AW}	Address Valid to End-of-Write	60	—	ns
t_{CW}	Chip Select to End-of-Write	60	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WP}	Write Pulse Width	45	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DW}	Data Valid to End-of-Write	30	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{OW}(2)	Output Active from End-of-Write	5	—	ns
t_{WHZ}(2)	Write Enable to Output in High-Z	0	30	ns

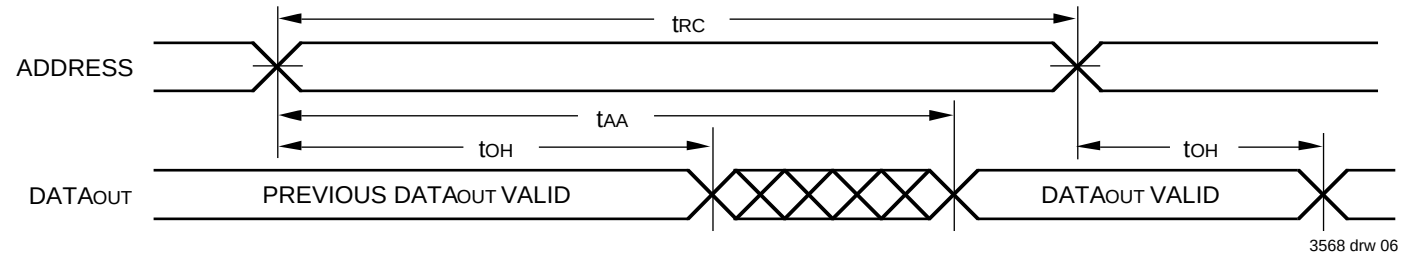
NOTES:
3568 tbl 08

1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

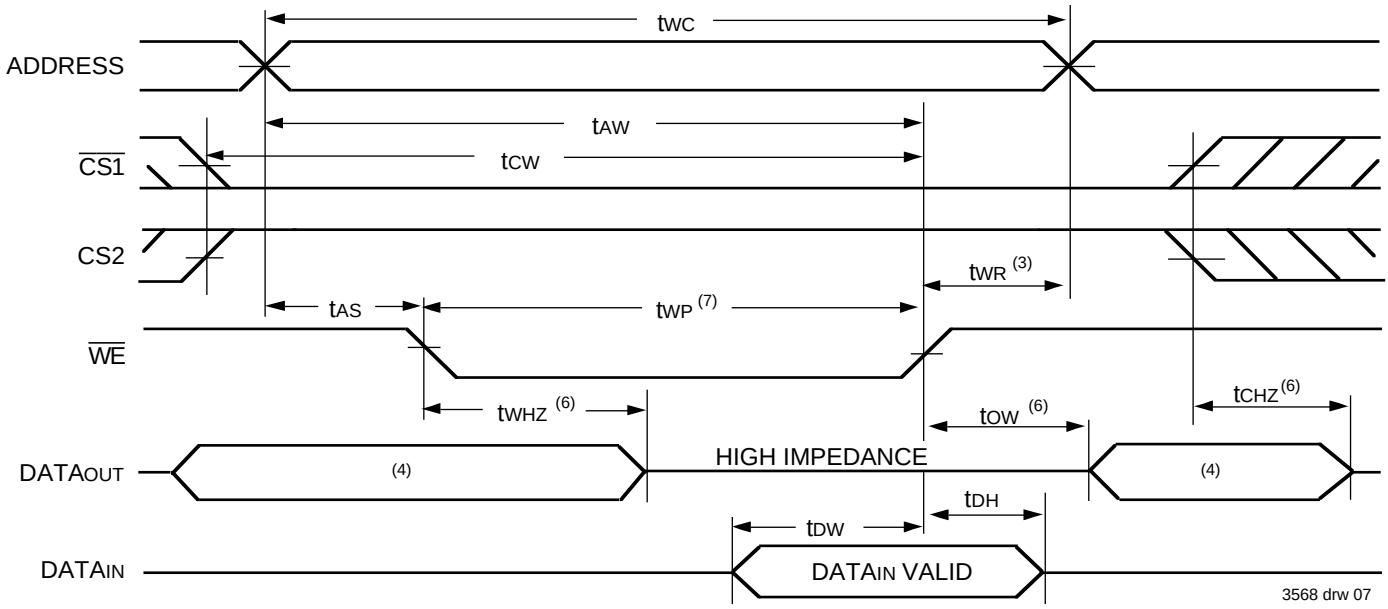


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

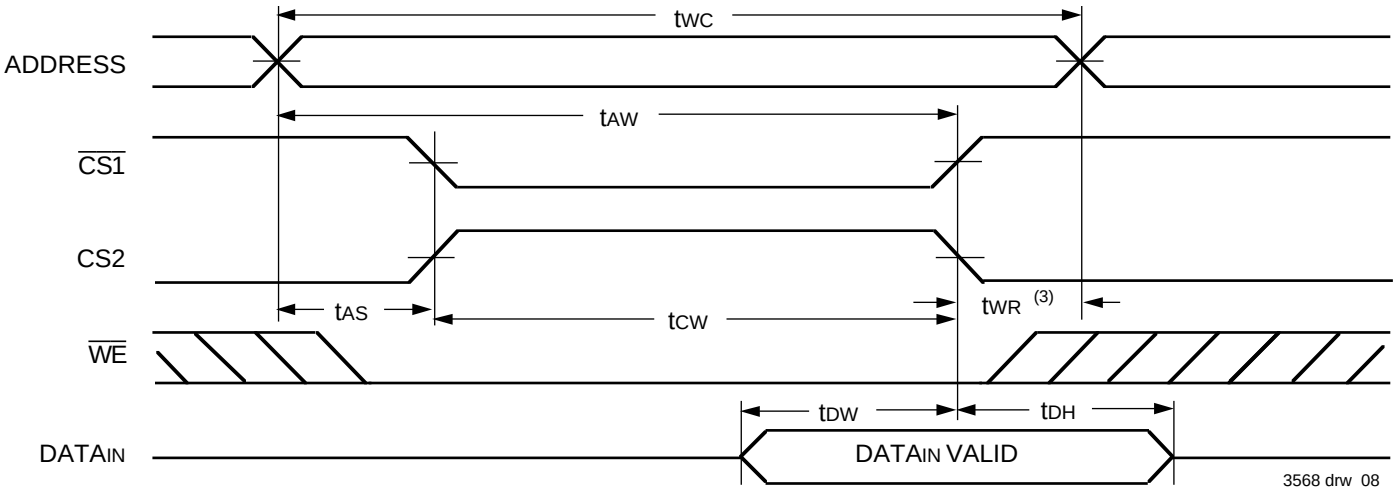


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS1}$ and CS2 must both be active during the t_{CW} write period.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.

ORDERING INFORMATION