



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256SA70

FEATURES:

- 32K x 8 CMOS static RAM
- Equal access and cycle times
 - Commercial: 70ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin 30 mil Plastic SOJ, 28-pin 300 mil Plastic Dip, 28-pin 300 mil TSOP Type I, and 28-pin 600 mil Plastic Dip.

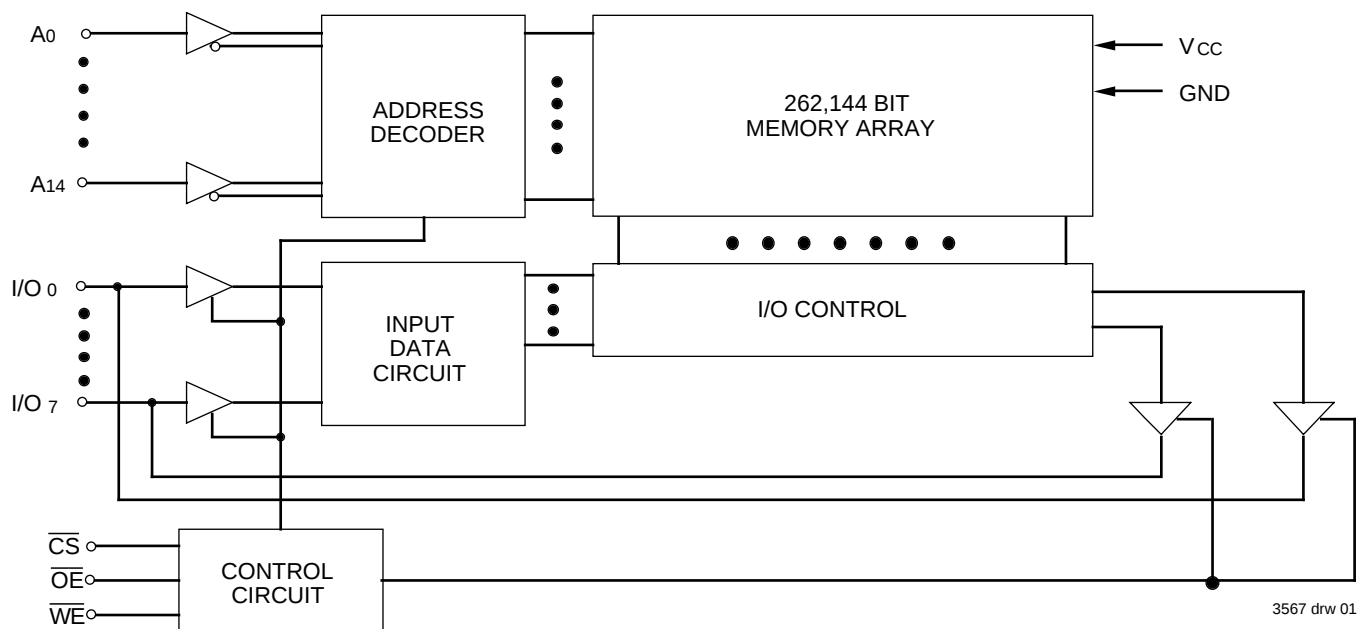
DESCRIPTION:

The IDT71256SA is a 262,144-bit medium-speed Static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for your memory needs.

All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in a 28-pin 300 mil Plastic SOJ, 28-pin 300 mil Plastic Dip, 28-pin 300 mil TSOP Type I and 28-pin 600 mil Plastic Dip.

FUNCTIONAL BLOCK DIAGRAM

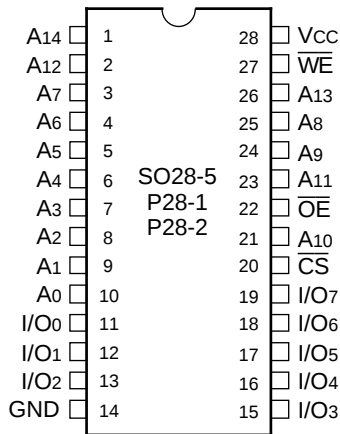


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COMMERCIAL TEMPERATURE RANGE

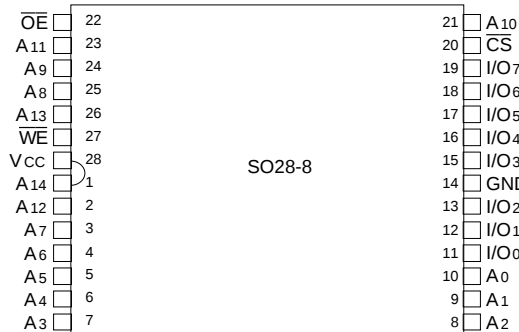
JULY 1996

PIN CONFIGURATION



3567 drw 02

SOJ/DIP
TOP VIEW



3567 drw 03

TSOP
TOP VIEW

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

3567 tbl 01

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA		Unit
			Min.	Max.	
ILI	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	5	μA
ILO	Output Leakage Current	VCC = Max., CS = VIH, VOUT = GND to VCC	—	5	μA
VOL	Output Low Voltage	IOL = 8mA, VCC = Min.	—	0.4	V
VOH	Output High Voltage	IOH = -4mA, VCC = Min.	2.4	—	V

3567 tbl 05

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	11	pF
CIO	I/O Capacitance	VOUT = 3dV	11	pF

NOTE:

3567 tbl 03

- This parameter is guaranteed by device characterization, but not production tested.

TRUTH TABLE^(1,2)

CS	OE	WE	I/O	Function
L	L	H	DATAOUT	Read Data
L	X	L	DATAIN	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected — Standby (ISB)
VHC ⁽³⁾	X	X	High-Z	Deselected — Standby (ISB1)

NOTES:

3567 tbl 04

- H = VIH, L = VIL, X = Don't care.
- VLC = 0.2V, VHC = VCC - 0.2V.
- Other inputs ≥ VHC or ≤ VLC.

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC–0.2V)

Symbol	Parameter	71256SA70	Unit
		Com'l.	
ICC	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, VCC = Max., f = fMAX ⁽²⁾	130	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, VCC = Max., f = fMAX ⁽²⁾	20	mA
ISB1	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, VCC = Max., f = 0 ⁽²⁾ VIN ≤ VLC or VIN ≥ VHC	15	mA

NOTES:

1. All values are maximum guaranteed values.
2. fMAX = 1/trc (all address inputs are cycling at fMAX); f = 0 means no address input lines are changing .

3567 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3567 tbl 07

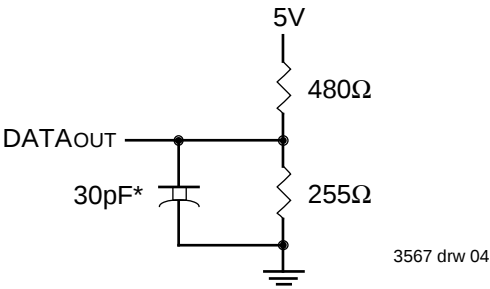


Figure 1. AC Test Load

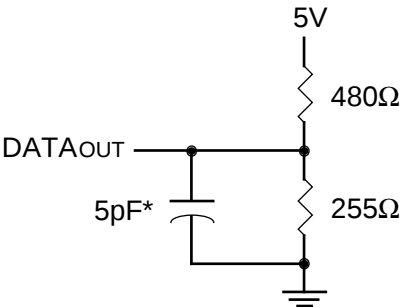


Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

*Including jig and scope capacitance.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, Commercial Temperature Range Only)

Symbol	Parameter	71256SA70		Unit	
		Min.	Max.		
Read Cycle					
tRC	Read Cycle Time	70	—	ns	
tAA	Address Access Time	—	70	ns	
tACS	Chip Select Access Time	—	70	ns	
tCLZ ⁽²⁾	Chip Select to Output in Low-Z	4	—	ns	
tCHZ ⁽²⁾	Chip Deselect to Output in High-Z	0	11	ns	
tOE	Output Enable to Output Valid	—	11	ns	
tOLZ ⁽²⁾	Output Enable to Output in Low-Z	0	—	ns	
tOHZ ⁽²⁾	Output Disable to Output in High-Z	0	10	ns	
tOH	Output Hold from Address Change	3	—	ns	
tPU ⁽²⁾	Chip Select to Power Up Time	0	—	ns	
tPD ⁽²⁾	Chip Deselect to Power Down Time	—	25	ns	
Write Cycle					
tWC	Write Cycle Time	70	—	ns	
tAW	Address Valid to End of Write	20	—	ns	
tCW	Chip Select to End of Write	20	—	ns	
tAS	Address Set-up Time	0	—	ns	
tWP	Write Pulse Width	20	—	ns	
tWR	Write Recovery Time	0	—	ns	
tDW	Data Valid to End of Write	13	—	ns	
tDH	Data Hold Time	0	—	ns	
tOW ⁽²⁾	Output Active from End of Write	4	—	ns	
tWHZ ⁽²⁾	Write Enable to Output in High-Z	0	11	ns	

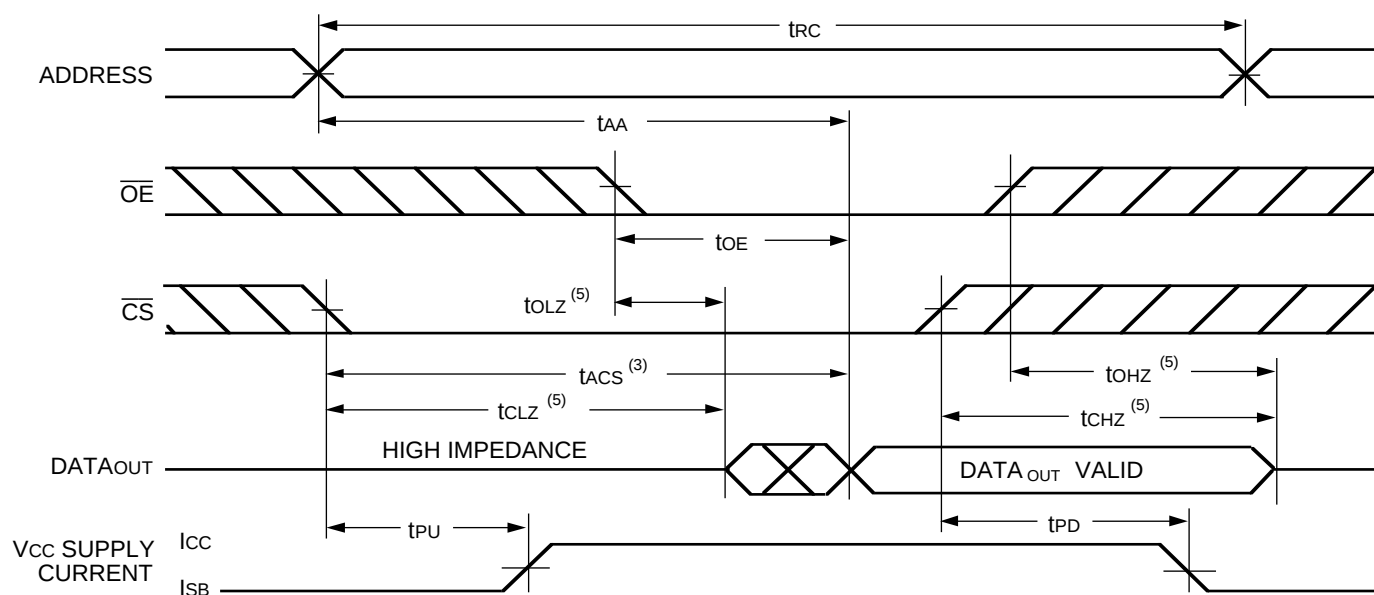
NOTES:

3567 tbl 08

1. 0° to +70°C temperature range only.

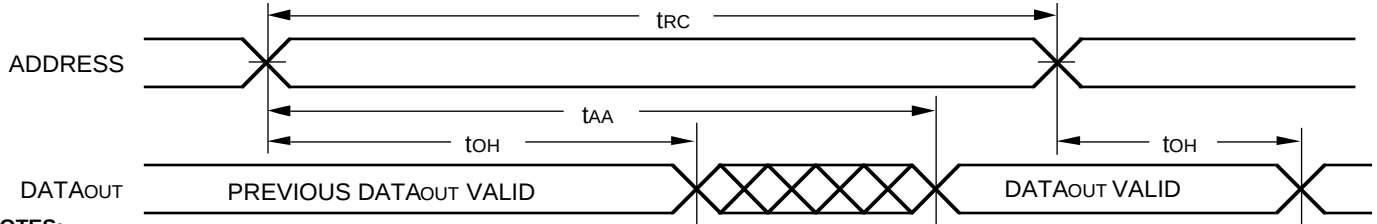
2. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



3567 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)

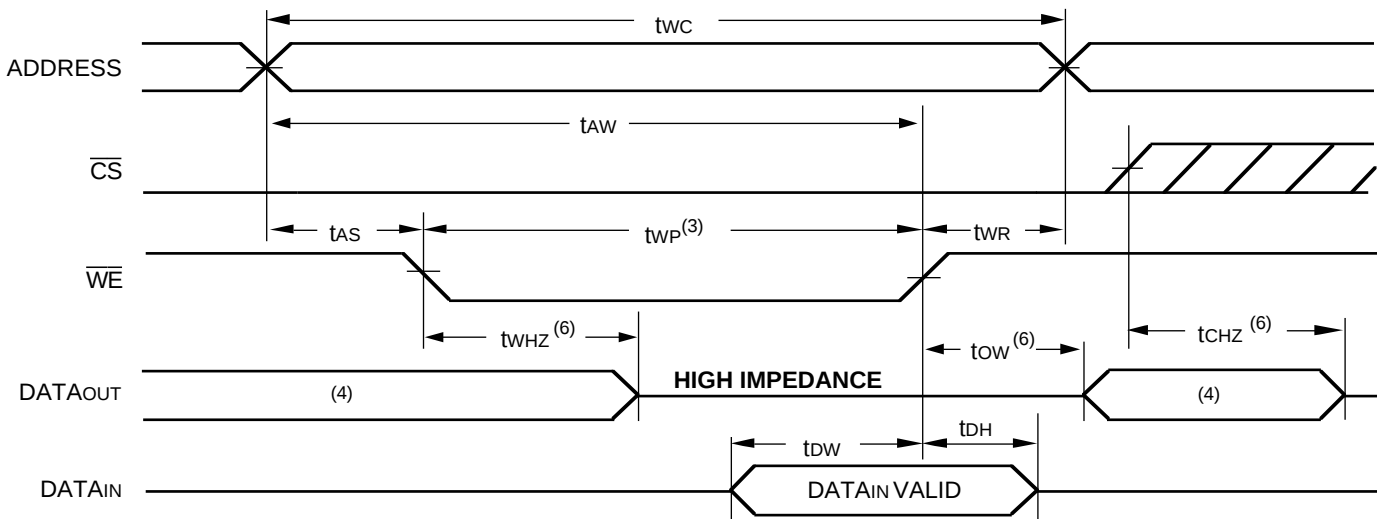


NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

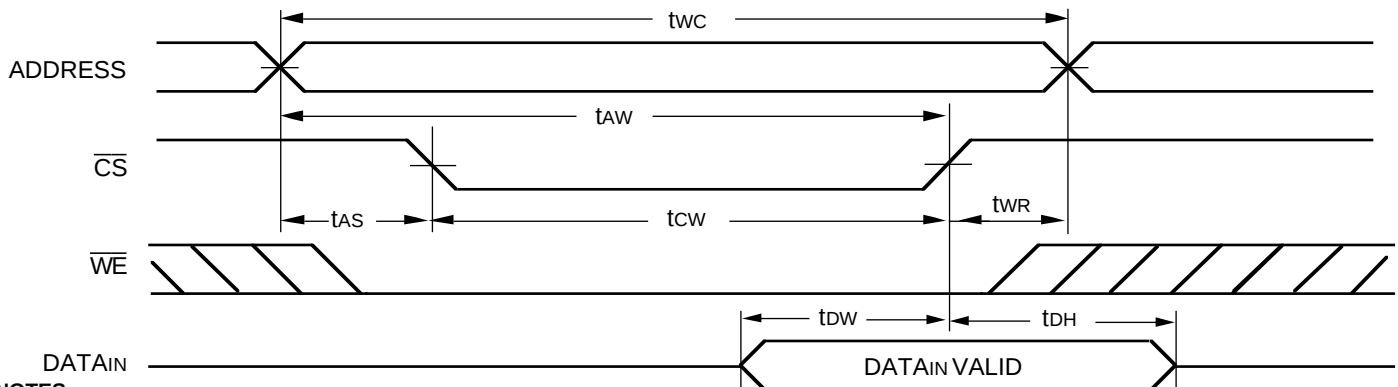
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TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)^(1,2,3,5)



3567 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)^(1,2,5)

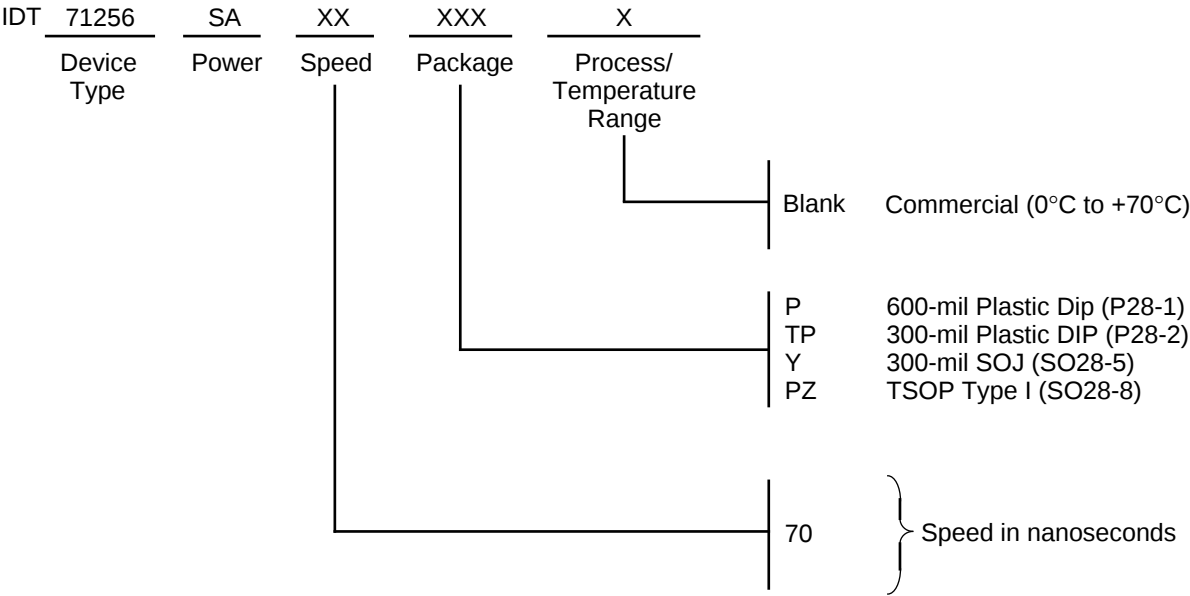


NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

3567 drw 09

ORDERING INFORMATION



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