



Integrated Device Technology, Inc.

# CMOS ASYNCHRONOUS FIFO WITH RETRANSMIT

## 1K x 9, 2K x 9, 4K x 9

IDT72021  
IDT72031  
IDT72041

### FEATURES:

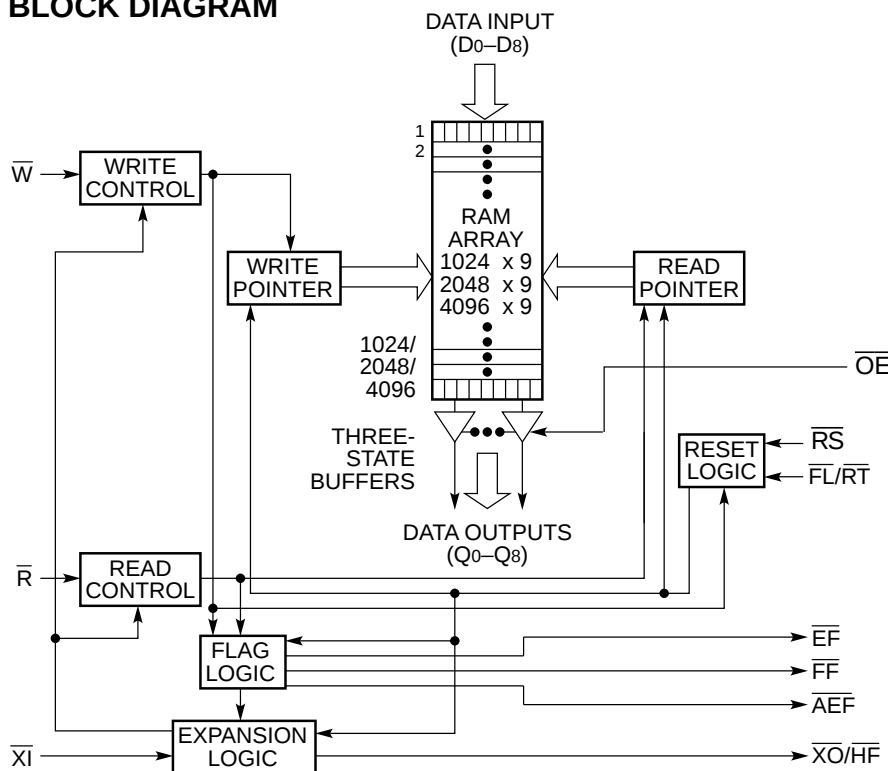
- First-In/First-Out Dual-Port memory
- Bit organization
  - IDT72021—1K x 9
  - IDT72031—2K x 9
  - IDT72041—4K x 9
- Ultra high speed
  - IDT72021—25ns access time
  - IDT72031—35ns access time
  - IDT72041—35ns access time
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ( $\overline{OE}$ ) and Almost Empty/Almost Full Flag ( $\overline{AEF}$ )
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost Empty/Almost Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and PLCC
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

### DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a Static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags, ( $\overline{HF}$ ,  $\overline{FF}$ ,  $\overline{EF}$ ,  $\overline{AEF}$ ) to monitor data overflow and underflow. Output Enable ( $\overline{OE}$ ) is provided to control the flow of data through the output port. Additional key features are Write ( $\overline{W}$ ), Read ( $\overline{R}$ ), Retransmit ( $\overline{RT}$ ), First Load ( $\overline{FL}$ ), Expansion In ( $\overline{XI}$ ) and Expansion Out ( $\overline{XO}$ ). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ( $\overline{OE}$ ) in multiprocessing and rate buffer applications.

The IDT72021/031/041s are fabricated using IDT's CMOS technology. Military grade product is manufactured in compliance with the latest version of MIL-STD-883, Class B, for high reliability systems.

### FUNCTIONAL BLOCK DIAGRAM



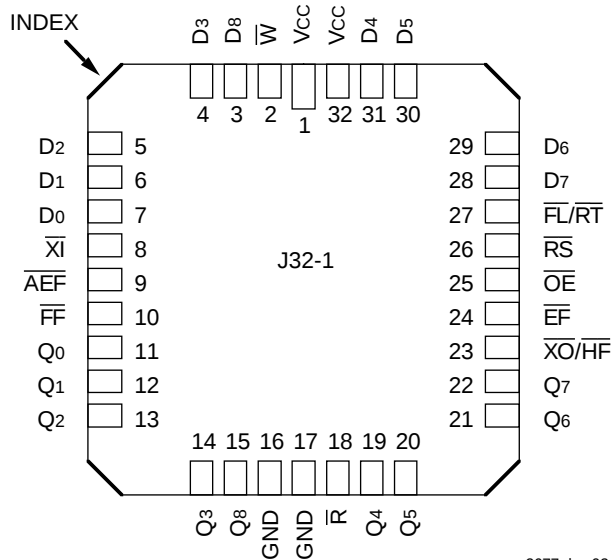
2677 drw 01

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### MILITARY AND COMMERCIAL TEMPERATURE RANGES

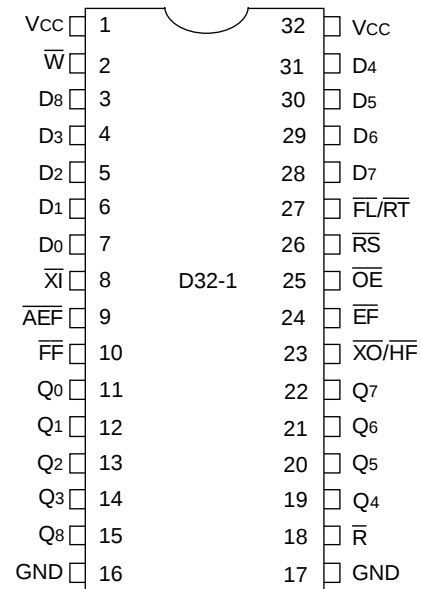
DECEMBER 1996

## PIN CONFIGURATIONS



2677 drw 03

PLCC TOP VIEW



2677 drw 02

DIP TOP VIEW

## PIN DESCRIPTIONS

| Symbol             | Name                              | I/O | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------|-----------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D0–D8              | Inputs                            | I   | Data inputs for 9-bit wide data.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| $\overline{RS}$    | Reset                             | I   | When $\overline{RS}$ is set LOW, internal READ and WRITE pointers are set to the first location of the RAM array. HF and FF go HIGH, and AEF and EF go LOW. A reset is required before an initial WRITE after power-up. R and W must be HIGH during $\overline{RS}$ cycle.                                                                                                                                                                                           |
| $\overline{W}$     | Write                             | I   | When WRITE is LOW, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, FF must be HIGH. When the FIFO is full (FF-LOW), the internal WRITE operation is blocked.                                                                                                                                                                                                                                              |
| $\overline{R}$     | Read                              | I   | When READ is LOW, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, EF must be HIGH. When the FIFO is empty (EF-LOW), the internal READ operation is blocked. The three-state output buffer is controlled by the read signal and the external output control ( $\overline{OE}$ ).                                                                                                                              |
| $\overline{FL/RT}$ | First Load/<br>Retransmit         | I   | This is a dual-purpose input. In the single device configuration ( $\overline{XI}$ grounded), activating retransmit ( $\overline{FL/RT}$ -LOW) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. R and W must be HIGH before setting $\overline{FL/RT}$ LOW. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL/RT}$ -LOW indicates the first activated device. |
| $\overline{XI}$    | Expansion In                      | I   | In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to XO (expansion out) of the previous device.                                                                                                                                                                                                                                                                             |
| $\overline{OE}$    | Output Enable                     | I   | When $\overline{OE}$ is set HIGH, the data flow through the three-state output buffer is inhibited regardless of an active READ operation. A read operation does increment the read pointer in this situation. When $\overline{OE}$ is set LOW, Q0-Q8 are still in a HIGH impedance condition if no READ occurs. For a complete READ operation with data appearing on Q0-Q8, both $\overline{R}$ and $\overline{OE}$ should be asserted LOW.                         |
| FF                 | Full Flag                         | O   | When FF goes LOW, the device is full and further WRITE operations are inhibited. When FF is HIGH, the device is not full.                                                                                                                                                                                                                                                                                                                                            |
| EF                 | Empty Flag                        | O   | When EF goes LOW, the device is empty and further READ operations are inhibited. When EF is HIGH, the device is not empty.                                                                                                                                                                                                                                                                                                                                           |
| AEF                | Almost-Empty/<br>Almost-Full Flag | O   | When AEF is LOW, the device is empty to 1/8 full or 7/8 to completely full. When AEF is HIGH, the device is greater than 1/8 full, but less than 7/8 full.                                                                                                                                                                                                                                                                                                           |
| $\overline{XO/HF}$ | Expansion Out/<br>Half-Full Flag  | O   | This is a dual purpose output. In the single device configuration ( $\overline{XI}$ grounded), the device is more than half full when HF is LOW. In the depth expansion configuration ( $\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.                                                                                                 |
| Q0–Q8              | Outputs                           | O   | Data outputs for 9-bit wide data.                                                                                                                                                                                                                                                                                                                                                                                                                                    |

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**STATUS FLAG**

| Number of Words in FIFO |           |           | $\overline{FF}$ | $\overline{AEF}$ | $\overline{HF}$ | $\overline{EF}$ |
|-------------------------|-----------|-----------|-----------------|------------------|-----------------|-----------------|
| 1K                      | 2K        | 4K        |                 |                  |                 |                 |
| 0                       | 0         | 0         | H               | L                | H               | L               |
| 1-127                   | 1-255     | 1-511     | H               | L                | H               | H               |
| 128-512                 | 256-1024  | 512-2048  | H               | H                | H               | H               |
| 513-896                 | 1025-1792 | 2049-3584 | H               | H                | L               | H               |
| 897-1023                | 1793-2047 | 3585-4095 | H               | L                | L               | H               |
| 1024                    | 2048      | 4096      | L               | L                | L               | H               |

2677 tbl 02

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

| Symbol            | Rating                               | Com'l.       | Mil.         | Unit |
|-------------------|--------------------------------------|--------------|--------------|------|
| V <sub>TERM</sub> | Terminal Voltage with Respect to GND | −0.5 to +7.0 | −0.5 to +7.0 | V    |
| T <sub>A</sub>    | Operating Temperature                | 0 to +70     | −55 to +125  | °C   |
| T <sub>BIAS</sub> | Temperature Under Bias               | −55 to +125  | −65 to +135  | °C   |
| T <sub>STG</sub>  | Storage Temperature                  | −55 to +125  | −65 to +155  | °C   |
| I <sub>OUT</sub>  | DC Output Current                    | 50           | 50           | mA   |

**NOTE:**

2677 tbl 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0 MHz)

| Symbol           | Parameter <sup>(1)</sup> | Condition             | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 10   | pF   |

**NOTE:**

2677 tbl 03

- These parameters are sampled and not 100% tested.

**RECOMMENDED DC OPERATING CONDITIONS**

| Symbol                         | Parameter                                 | Min. | Typ. | Max. | Unit |
|--------------------------------|-------------------------------------------|------|------|------|------|
| V <sub>CCM</sub>               | Military Supply Voltage                   | 4.5  | 5.0  | 5.5  | V    |
| V <sub>CC</sub>                | Commercial Supply Voltage                 | 4.5  | 5.0  | 5.5  | V    |
| GND                            | Supply Voltage                            | 0    | 0    | 0    | V    |
| V <sub>IH</sub>                | Input High Voltage Commercial             | 2.0  | —    | —    | V    |
| V <sub>IH</sub>                | Input High Voltage Military               | 2.2  | —    | —    | V    |
| V <sub>IL</sub> <sup>(1)</sup> | Input Low Voltage Commercial and Military | —    | —    | 0.8  | V    |

**NOTE:**

2677 tbl 05

- 1.5V undershoots are allowed for 10ns once per cycle.

**DC ELECTRICAL CHARACTERISTICS — IDT72021**(Commercial:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ; Military:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ )

| Symbol            | Parameter                                                                          | IDT72021<br>Commercial<br>$t_A = 25, 35\text{ns}$ |      |      | IDT72021<br>Military<br>$t_A = 30, 40\text{ns}$ |      |      | IDT72021<br>Commercial<br>$t_A = 50\text{ns}$ |      |      | IDT72021<br>Military<br>$t_A = 50\text{ns}$ |      |      | Unit          |
|-------------------|------------------------------------------------------------------------------------|---------------------------------------------------|------|------|-------------------------------------------------|------|------|-----------------------------------------------|------|------|---------------------------------------------|------|------|---------------|
|                   |                                                                                    | Min.                                              | Typ. | Max. | Min.                                            | Typ. | Max. | Min.                                          | Typ. | Max. | Min.                                        | Typ. | Max. |               |
| $I_{LI}^{(1)}$    | Input Leakage Current (Any Input)                                                  | -1                                                | —    | 1    | -10                                             | —    | 10   | -1                                            | —    | 1    | -10                                         | —    | 10   | $\mu\text{A}$ |
| $I_{LO}^{(2)}$    | Output Leakage Current                                                             | -10                                               | —    | 10   | -10                                             | —    | 10   | -10                                           | —    | 10   | -10                                         | —    | 10   | $\mu\text{A}$ |
| $V_{OH}$          | Output Logic "1" Voltage<br>$I_{OH} = -2\text{mA}$                                 | 2.4                                               | —    | —    | 2.4                                             | —    | —    | 2.4                                           | —    | —    | 2.4                                         | —    | —    | V             |
| $V_{OL}$          | Output Logic "0" Voltage<br>$I_{OL} = 8\text{mA}$                                  | —                                                 | —    | 0.4  | —                                               | —    | 0.4  | —                                             | —    | 0.4  | —                                           | —    | 0.4  | V             |
| $I_{CC1}^{(3,4)}$ | Active Power Supply Current                                                        | —                                                 | —    | 120  | —                                               | —    | 140  | —                                             | 50   | 80   | —                                           | 70   | 100  | mA            |
| $I_{CC2}^{(3)}$   | Standby Current<br>( $\bar{R} = \bar{W} = \bar{RS} = \bar{FL}/\bar{RT} = V_{IH}$ ) | —                                                 | —    | 12   | —                                               | —    | 20   | —                                             | 5    | 8    | —                                           | 8    | 15   | mA            |
| $I_{CC3}^{(3)}$   | Power Down Current<br>(All Input = $V_{CC} - 0.2V$ )                               | —                                                 | —    | 500  | —                                               | —    | 900  | —                                             | —    | 500  | —                                           | —    | 900  | $\mu\text{A}$ |

2677 tbl 06

**DC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041**(Commercial:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ; Military:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ )

| Symbol            | Parameter                                                                       | IDT72031<br>IDT72041<br>Commercial<br>$t_A = 35, 50\text{ns}$ |      |      | IDT72031<br>IDT72041<br>Military<br>$t_A = 40, 50\text{ns}$ |      |      | Unit          |
|-------------------|---------------------------------------------------------------------------------|---------------------------------------------------------------|------|------|-------------------------------------------------------------|------|------|---------------|
|                   |                                                                                 | Min.                                                          | Typ. | Max. | Min.                                                        | Typ. | Max. |               |
| $I_{LI}^{(1)}$    | Input Leakage Current (Any Input)                                               | -1                                                            | —    | 1    | -10                                                         | —    | 10   | $\mu\text{A}$ |
| $I_{LO}^{(2)}$    | Output Leakage Current                                                          | -10                                                           | —    | 10   | -10                                                         | —    | 10   | $\mu\text{A}$ |
| $V_{OH}$          | Output Logic "1" Voltage $I_{OUT} = -2\text{mA}$                                | 2.4                                                           | —    | —    | 2.4                                                         | —    | —    | V             |
| $V_{OL}$          | Output Logic "0" Voltage $I_{OUT} = 8\text{mA}$                                 | —                                                             | —    | 0.4  | —                                                           | —    | 0.4  | V             |
| $I_{CC1}^{(3,5)}$ | Active Power Supply Current                                                     | —                                                             | 75   | 120  | —                                                           | 100  | 150  | mA            |
| $I_{CC2}^{(3)}$   | Standby Current ( $\bar{R} = \bar{W} = \bar{RS} = \bar{FL}/\bar{RT} = V_{IH}$ ) | —                                                             | 8    | 12   | —                                                           | 12   | 25   | mA            |
| $I_{CC3}^{(3)}$   | Power Down Current (All Input = $V_{CC} - 0.2V$ )                               | —                                                             | —    | 2    | —                                                           | —    | 4    | mA            |

**NOTES:**

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- Measurements with  $0.4 \leq V_{IN} \leq V_{CC}$ .
- $\bar{R} \geq V_{IH}$ ,  $0.4 \leq V_{OUT} \leq V_{CC}$ .
- $I_{CC}$  measurements are made with  $\bar{OE} = \text{HIGH}$ .
- Tested at  $f = 20\text{MHz}$ .
- Tested at  $f = 15.3\text{MHz}$ .

**AC ELECTRICAL CHARACTERISTICS — IDT72021<sup>(1)</sup>**(Commercial: V<sub>CC</sub> = 5.0V±10%, T<sub>A</sub> = 0°C to +70°C; Military: V<sub>CC</sub> = 5V±10%, T<sub>A</sub> = -55°C to +125°C)

| Symbol | Parameter                                                   | Com'l    |      | Mil.     |      | Com'l    |      | Mil.     |      | Com'l & Mil. |      | Unit |
|--------|-------------------------------------------------------------|----------|------|----------|------|----------|------|----------|------|--------------|------|------|
|        |                                                             | 72021L25 |      | 72021L30 |      | 72021L35 |      | 72021L40 |      | 72021L50     |      |      |
|        |                                                             | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.         | Max. |      |
| fs     | Shift Frequency                                             | —        | 28.5 | —        | 25   | —        | 22.2 | —        | 20   | —            | 15   | MHz  |
| trc    | $\bar{R}$ Cycle Time                                        | 35       | —    | 40       | —    | 45       | —    | 50       | —    | 65           | —    | ns   |
| ta     | Access Time                                                 | —        | 25   | —        | 30   | —        | 35   | —        | 40   | —            | 50   | ns   |
| trr    | $\bar{R}$ Recovery Time                                     | 10       | —    | 10       | —    | 10       | —    | 10       | —    | 15           | —    | ns   |
| trpw   | $\bar{R}$ Pulse Width <sup>(2)</sup>                        | 25       | —    | 30       | —    | 35       | —    | 40       | —    | 50           | —    | ns   |
| trlz   | $\bar{R}$ Pulse LOW to Data Bus at Low-Z <sup>(3)</sup>     | 5        | —    | 5        | —    | 5        | —    | 5        | —    | 10           | —    | ns   |
| twlz   | $\bar{W}$ Pulse HIGH to Data Bus at Low-Z <sup>(3,4)</sup>  | 5        | —    | 5        | —    | 5        | —    | 5        | —    | 5            | —    | ns   |
| tdv    | Data Valid from $\bar{R}$ Pulse HIGH                        | 5        | —    | 5        | —    | 5        | —    | 5        | —    | 5            | —    | ns   |
| trhz   | $\bar{R}$ Pulse HIGH to Data Bus at High-Z <sup>(3)</sup>   | —        | 18   | —        | 20   | —        | 20   | —        | 25   | —            | 30   | ns   |
| twc    | $\bar{W}$ Cycle Time                                        | 35       | —    | 40       | —    | 45       | —    | 50       | —    | 65           | —    | ns   |
| twpw   | $\bar{W}$ Pulse Width <sup>(2)</sup>                        | 25       | —    | 30       | —    | 35       | —    | 40       | —    | 50           | —    | ns   |
| twr    | $\bar{W}$ Recovery Time                                     | 10       | —    | 10       | —    | 10       | —    | 10       | —    | 15           | —    | ns   |
| tds    | Data Set-up Time                                            | 15       | —    | 18       | —    | 18       | —    | 20       | —    | 30           | —    | ns   |
| tdh    | Data Hold Time                                              | 0        | —    | 0        | —    | 0        | —    | 0        | —    | 5            | —    | ns   |
| trsc   | $\overline{RS}$ Cycle Time                                  | 35       | —    | 40       | —    | 45       | —    | 50       | —    | 65           | —    | ns   |
| trs    | $\overline{RS}$ Pulse Width <sup>(2)</sup>                  | 25       | —    | 30       | —    | 35       | —    | 40       | —    | 50           | —    | ns   |
| trss   | $\overline{RS}$ Set-up Time                                 | 25       | —    | 30       | —    | 35       | —    | 40       | —    | 50           | —    | ns   |
| trsr   | $\overline{RS}$ Recovery Time                               | 10       | —    | 10       | —    | 10       | —    | 10       | —    | 15           | —    | ns   |
| trtc   | $\overline{RT}$ Cycle Time                                  | 35       | —    | 40       | —    | 45       | —    | 50       | —    | 65           | —    | ns   |
| trt    | $\overline{RT}$ Pulse Width <sup>(2)</sup>                  | 25       | —    | 30       | —    | 35       | —    | 40       | —    | 50           | —    | ns   |
| trtr   | $\overline{RT}$ Recovery Time                               | 10       | —    | 10       | —    | 10       | —    | 10       | —    | 15           | —    | ns   |
| trsf1  | $\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ LOW | —        | 35   | —        | 40   | —        | 45   | —        | 50   | —            | 65   | ns   |
| trsf2  | $\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ HIGH | —        | 35   | —        | 40   | —        | 45   | —        | 50   | —            | 65   | ns   |
| tref   | $\bar{R}$ LOW to $\overline{EF}$ LOW                        | —        | 25   | —        | 30   | —        | 30   | —        | 35   | —            | 45   | ns   |
| trff   | $\bar{R}$ HIGH to $\overline{FF}$ HIGH                      | —        | 25   | —        | 30   | —        | 30   | —        | 35   | —            | 45   | ns   |
| trpe   | $\bar{R}$ Pulse Width After $\overline{EF}$ HIGH            | 25       | —    | 30       | —    | 35       | —    | 40       | —    | 50           | —    | ns   |
| tweF   | $\bar{W}$ HIGH to $\overline{EF}$ HIGH                      | —        | 25   | —        | 30   | —        | 30   | —        | 35   | —            | 45   | ns   |
| twFF   | $\bar{W}$ LOW to $\overline{EF}$ LOW                        | —        | 25   | —        | 30   | —        | 30   | —        | 35   | —            | 45   | ns   |
| twhF   | $\bar{W}$ LOW to $\overline{HF}$ LOW                        | —        | 35   | —        | 40   | —        | 45   | —        | 50   | —            | 65   | ns   |
| trhF   | $\bar{R}$ HIGH to $\overline{HF}$ HIGH                      | —        | 35   | —        | 40   | —        | 45   | —        | 50   | —            | 65   | ns   |
| twPF   | $\bar{W}$ Pulse Width after $\overline{FF}$ HIGH            | 25       | —    | 30       | —    | 35       | —    | 40       | —    | 50           | —    | ns   |
| trF    | $\bar{R}$ HIGH to Transitioning $\overline{AEF}$            | —        | 35   | —        | 40   | —        | 45   | —        | 50   | —            | 65   | ns   |
| twF    | $\bar{W}$ LOW to Transitioning $\overline{AEF}$             | —        | 35   | —        | 40   | —        | 45   | —        | 50   | —            | 65   | ns   |
| toehz  | $\overline{OE}$ HIGH to High-Z (Disable) <sup>(3)</sup>     | 0        | 12   | 0        | 15   | 0        | 17   | 0        | 20   | 0            | 25   | ns   |
| toelz  | $\overline{OE}$ LOW to Low-Z (Enable) <sup>(3)</sup>        | 0        | 12   | 0        | 15   | 0        | 17   | 0        | 20   | 0            | 25   | ns   |
| taoe   | $\overline{OE}$ LOW Data Valid (Q0–Q8)                      | —        | 15   | —        | 18   | —        | 20   | —        | 25   | —            | 30   | ns   |

**NOTES:**

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 08

**AC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041<sup>(1)</sup>**(Commercial: V<sub>CC</sub> = 5.0V±10%, T<sub>A</sub> = 0°C to +70°C; Military: V<sub>CC</sub> = 5V±10%, T<sub>A</sub> = -55°C to +125°C)

| Symbol | Parameter                                                       | Com'I                |      | Mil.                 |      | Com'I and Mil.       |      | Unit |
|--------|-----------------------------------------------------------------|----------------------|------|----------------------|------|----------------------|------|------|
|        |                                                                 | 72031L35<br>72041L35 |      | 72031L40<br>72041L40 |      | 72031L50<br>72041L50 |      |      |
|        |                                                                 | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |      |
| fS     | Shift Frequency                                                 | —                    | 22.2 | —                    | 20   | —                    | 15   | MHz  |
| tRC    | $\overline{R}$ Cycle Time                                       | 45                   | —    | 50                   | —    | 65                   | —    | ns   |
| tA     | Access Time                                                     | —                    | 35   | —                    | 40   | —                    | 50   | ns   |
| tRR    | $\overline{R}$ Recovery Time                                    | 10                   | —    | 10                   | —    | 15                   | —    | ns   |
| trPW   | $\overline{R}$ Pulse Width <sup>(2)</sup>                       | 35                   | —    | 40                   | —    | 50                   | —    | ns   |
| trLZ   | $\overline{R}$ Pulse LOW to Data Bus at Low-Z <sup>(3)</sup>    | 5                    | —    | 5                    | —    | 10                   | —    | ns   |
| twLZ   | $\overline{W}$ Pulse HIGH to Data Bus at Low-Z <sup>(3,4)</sup> | 5                    | —    | 5                    | —    | 5                    | —    | ns   |
| tdV    | Data Valid from $\overline{R}$ Pulse HIGH                       | 5                    | —    | 5                    | —    | 5                    | —    | ns   |
| trHZ   | $\overline{R}$ Pulse HIGH to Data Bus at High-Z <sup>(3)</sup>  | —                    | 20   | —                    | 25   | —                    | 30   | ns   |
| tWC    | $\overline{W}$ Cycle Time                                       | 45                   | —    | 50                   | —    | 65                   | —    | ns   |
| tWPW   | $\overline{W}$ Pulse Width <sup>(2)</sup>                       | 35                   | —    | 40                   | —    | 50                   | —    | ns   |
| tWR    | $\overline{W}$ Recovery Time                                    | 10                   | —    | 10                   | —    | 15                   | —    | ns   |
| tDS    | Data Set-up Time                                                | 18                   | —    | 20                   | —    | 30                   | —    | ns   |
| tDH    | Data Hold Time                                                  | 0                    | —    | 0                    | —    | 5                    | —    | ns   |
| trSC   | $\overline{RS}$ Cycle Time                                      | 45                   | —    | 50                   | —    | 65                   | —    | ns   |
| trS    | $\overline{RS}$ Pulse Width <sup>(2)</sup>                      | 35                   | —    | 40                   | —    | 50                   | —    | ns   |
| trSS   | $\overline{RS}$ Set-up Time                                     | 35                   | —    | 40                   | —    | 50                   | —    | ns   |
| trSR   | $\overline{RS}$ Recovery Time                                   | 10                   | —    | 10                   | —    | 15                   | —    | ns   |
| trTC   | $\overline{RT}$ Cycle Time                                      | 45                   | —    | 50                   | —    | 65                   | —    | ns   |
| trT    | $\overline{RT}$ Pulse Width <sup>(2)</sup>                      | 35                   | —    | 40                   | —    | 50                   | —    | ns   |
| trTR   | $\overline{RT}$ Recovery Time                                   | 10                   | —    | 10                   | —    | 15                   | —    | ns   |
| trSF1  | $\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ LOW     | —                    | 45   | —                    | 50   | —                    | 65   | ns   |
| trSF2  | $\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ HIGH     | —                    | 45   | —                    | 50   | —                    | 65   | ns   |
| trEF   | $\overline{R}$ LOW to $\overline{EF}$ LOW                       | —                    | 30   | —                    | 35   | —                    | 45   | ns   |
| trFF   | $\overline{R}$ HIGH to $\overline{FF}$ HIGH                     | —                    | 30   | —                    | 35   | —                    | 45   | ns   |
| trPE   | $\overline{R}$ Pulse Width After $\overline{EF}$ HIGH           | 35                   | —    | 40                   | —    | 50                   | —    | ns   |
| twEF   | $\overline{W}$ HIGH to $\overline{EF}$ HIGH                     | —                    | 30   | —                    | 35   | —                    | 45   | ns   |
| twFF   | $\overline{W}$ LOW to $\overline{EF}$ LOW                       | —                    | 30   | —                    | 35   | —                    | 45   | ns   |
| twHF   | $\overline{W}$ LOW to $\overline{HF}$ LOW                       | —                    | 45   | —                    | 50   | —                    | 65   | ns   |
| trHF   | $\overline{R}$ HIGH to $\overline{HF}$ HIGH                     | —                    | 45   | —                    | 50   | —                    | 65   | ns   |
| twPF   | $\overline{W}$ Pulse Width after $\overline{FF}$ HIGH           | 35                   | —    | 40                   | —    | 50                   | —    | ns   |
| trF    | $\overline{R}$ HIGH to Transitioning $\overline{AEF}$           | —                    | 45   | —                    | 50   | —                    | 65   | ns   |
| twF    | $\overline{W}$ LOW to Transitioning $\overline{AEF}$            | —                    | 45   | —                    | 50   | —                    | 65   | ns   |
| toEHZ  | $\overline{OE}$ HIGH to High-Z (Disable) <sup>(3)</sup>         | 0                    | 17   | 0                    | 20   | 0                    | 25   | ns   |
| toELZ  | $\overline{OE}$ LOW to Low-Z (Enable) <sup>(3)</sup>            | 0                    | 17   | 0                    | 20   | 0                    | 25   | ns   |
| taOE   | $\overline{OE}$ LOW Data Valid (Q0–Q8)                          | —                    | 20   | —                    | 25   | —                    | 30   | ns   |

**NOTES:**

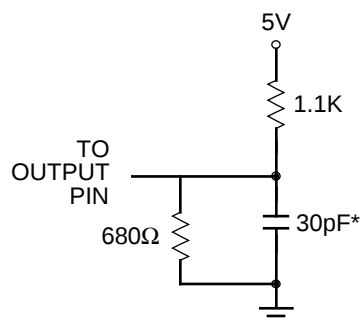
2677 tbl 09

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

## AC TEST CONDITIONS

|                               |              |
|-------------------------------|--------------|
| Input Pulse Levels            | GND to 3.0V  |
| Input Rise/Fall Times         | 5ns          |
| Input Timing Reference Levels | 1.5V         |
| Output Reference Levels       | 1.5V         |
| Output Load                   | See Figure 1 |

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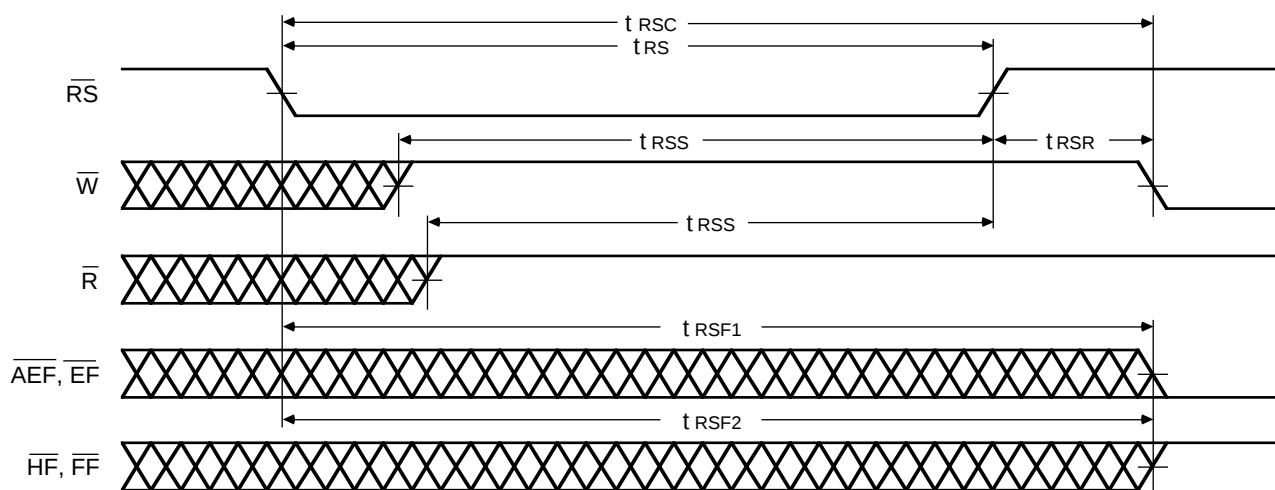


2677 drw 04

or equivalent circuit

**Figure 1. Output Load**

\* Includes scope and jig capacitances.

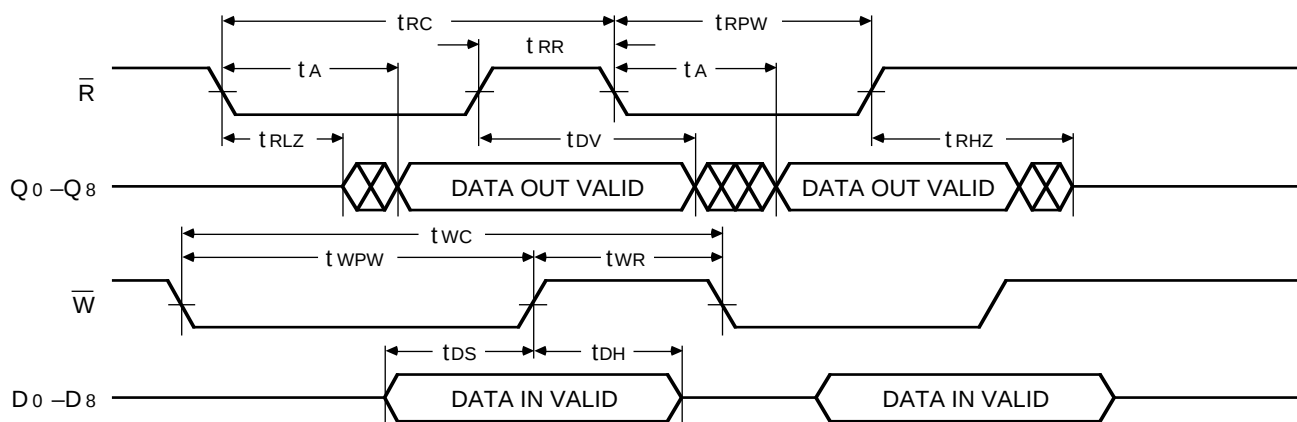


2677 drw 05

**Figure 2. Reset**

### NOTES:

1.  $\overline{EF}$ ,  $\overline{FF}$ ,  $\overline{HF}$ , and  $\overline{AEF}$  may change status during Reset, but flags will be valid at  $t_{RSC}$ .
2.  $\overline{W}$  and  $\overline{R}$  =  $V_{IH}$  around the rising edge of  $\overline{RS}$ .



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**Figure 3. Asynchronous Write and Read Operation**

### NOTE:

1. Assume  $\overline{OE}$  is asserted LOW.

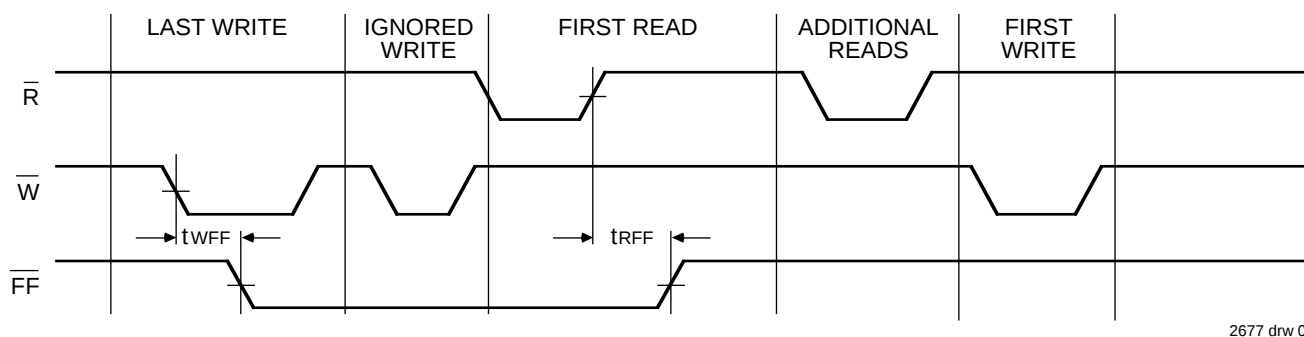


Figure 4. Full Flag From Last Write to First Read

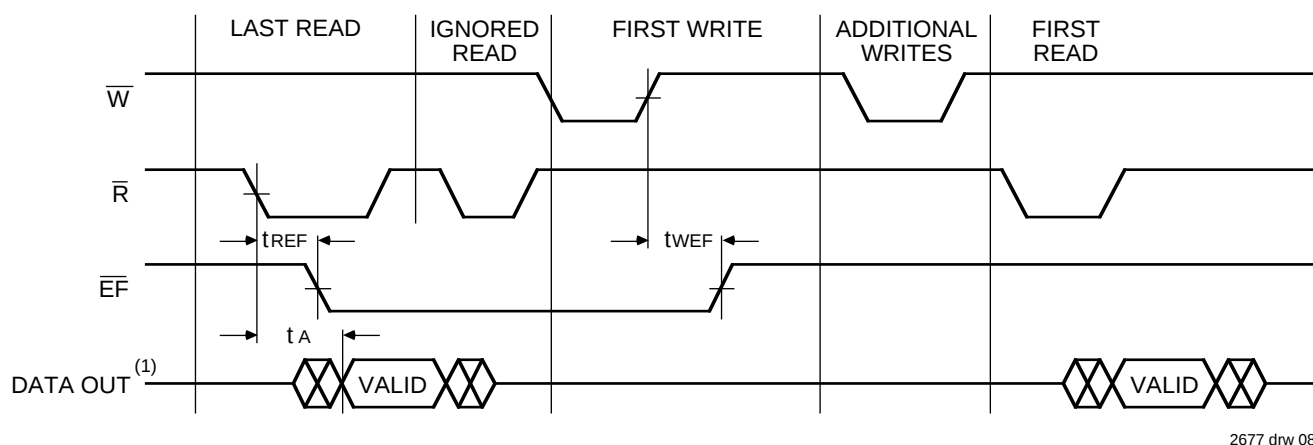


Figure 5. Empty Flag From Last Read to First Write

**NOTE:**

1. Assume  $\overline{OE}$  is asserted LOW.

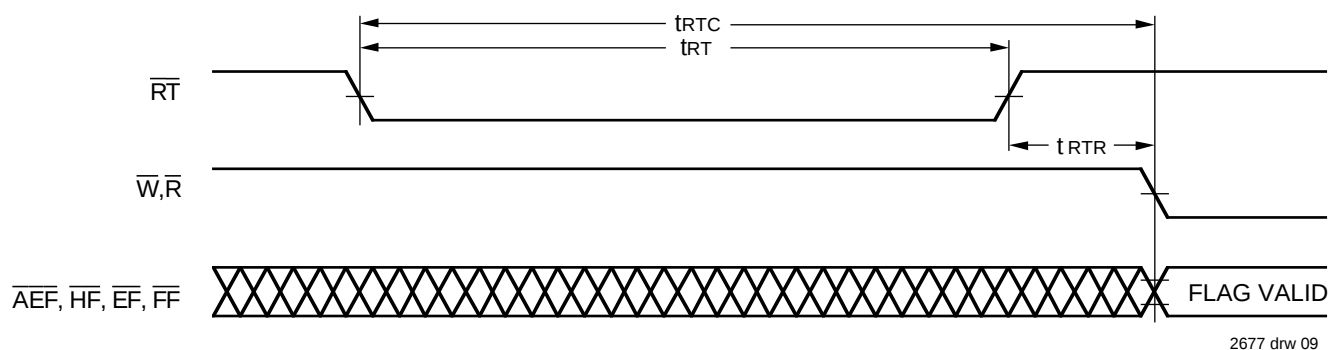


Figure 6. Retransmit

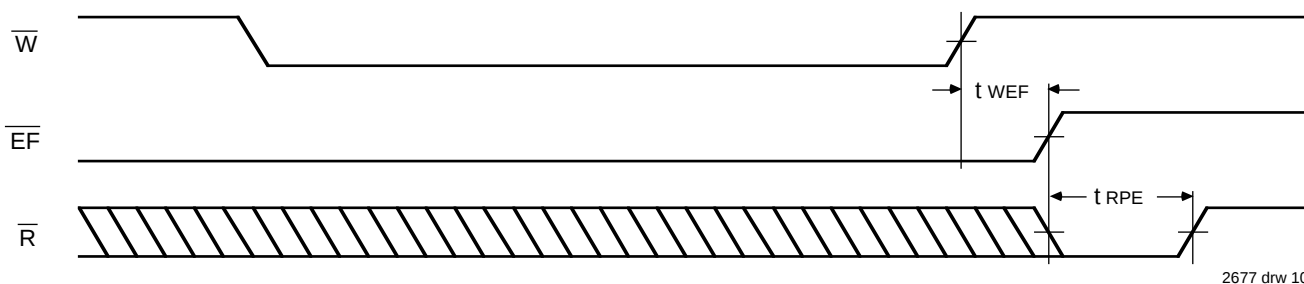


Figure 7. Empty Flag Timing  
Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

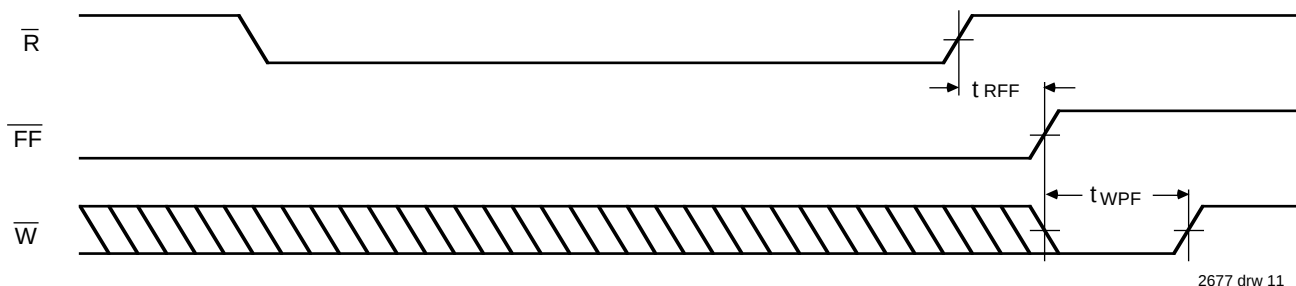


Figure 8. Full Flag Timing

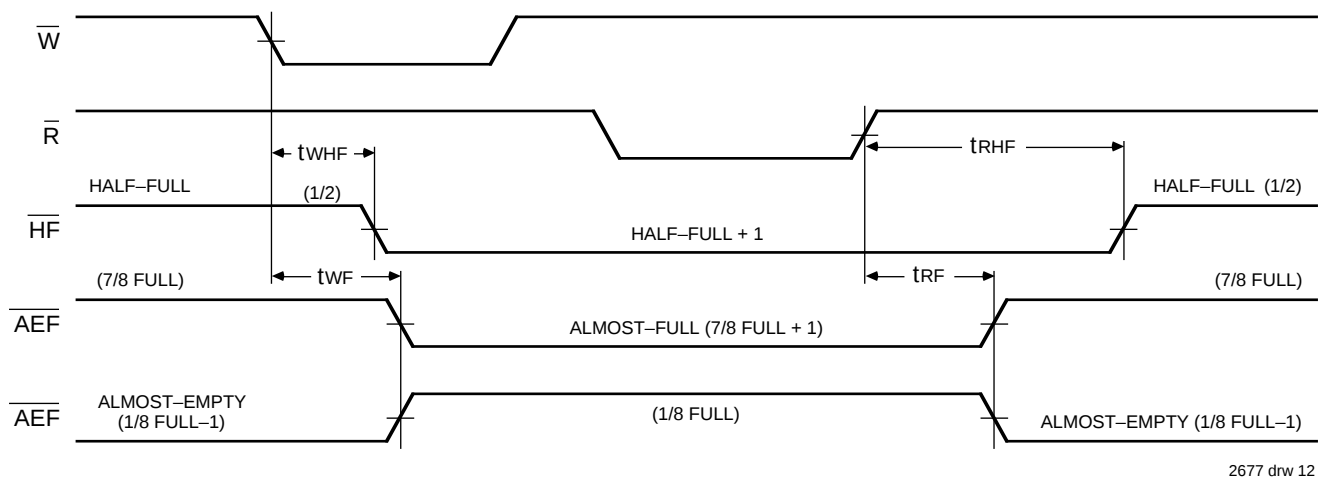


Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

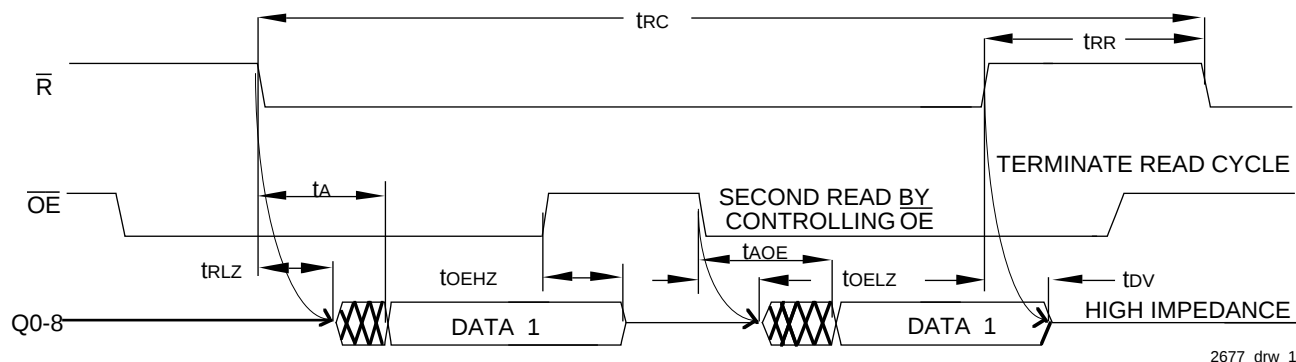


Figure 10. Output Enable and Read Operation Timings

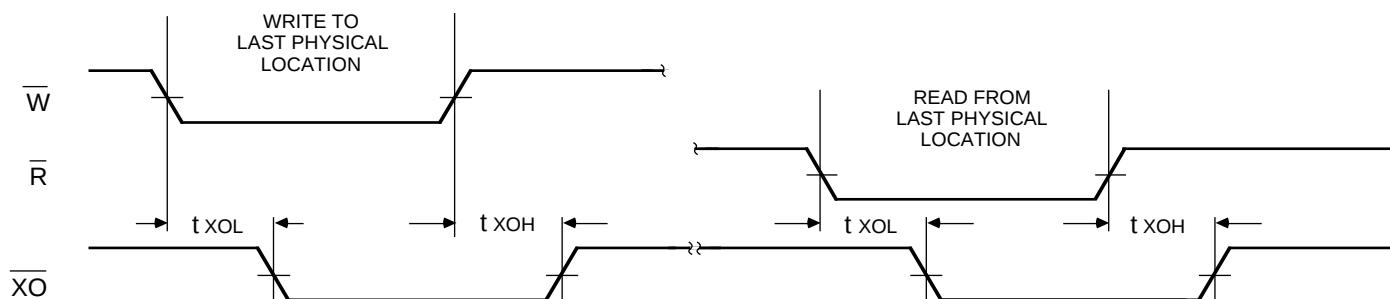


Figure 11. Expansion Out

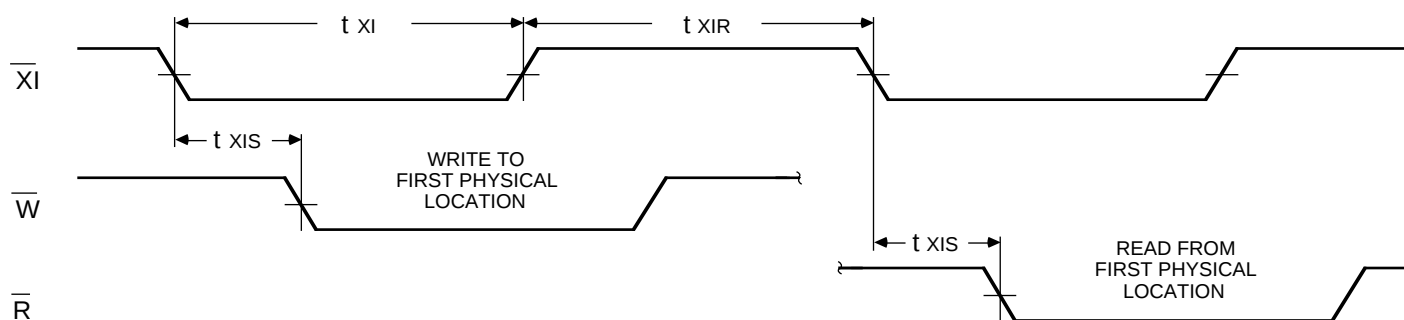


Figure 12. Expansion In

## OPERATING CONFIGURATIONS

### SINGLE DEVICE CONFIGURATION

The IDT72021/031/041 is in the Single Device Configuration when the Expansion In ( $\overline{XI}$ ) control input is grounded (see Figure 13).

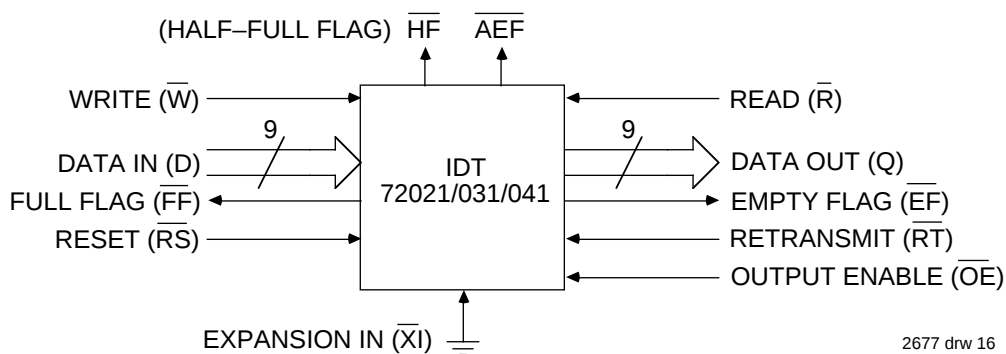


Figure 13. Block Diagram of Single 1K/2K/4K x 9 FIFO

## WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ( $\overline{EF}$ ,  $\overline{FF}$ ,  $\overline{HF}$ , and  $\overline{AEF}$ ) can be detected from any one

device. Figure 14 demonstrates an 18-bit word width by using two IDT72021/031/041 devices. Any word width can be attained by adding additional IDT72021/031/041s.

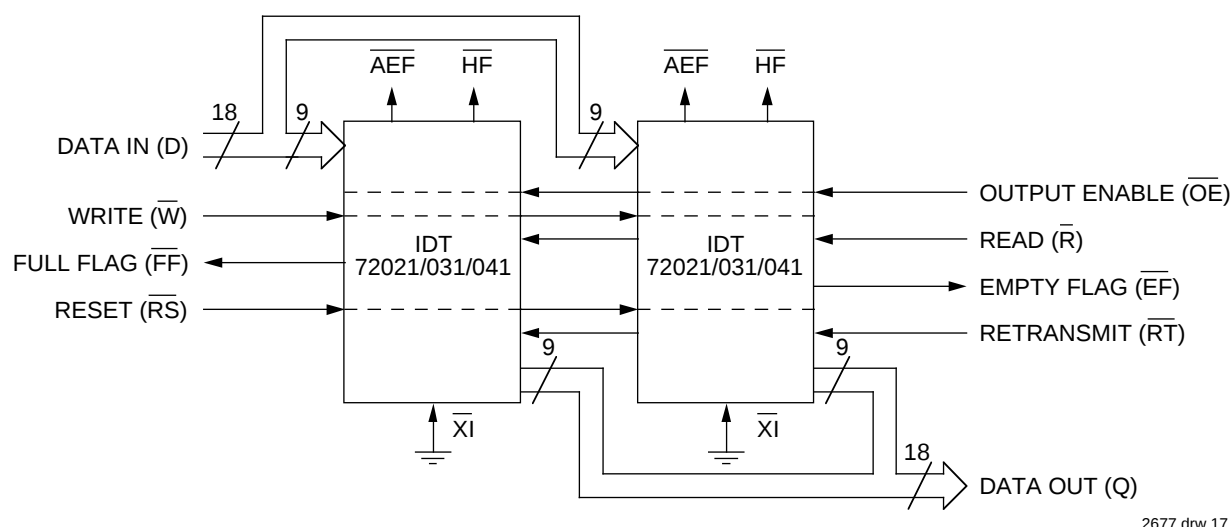


Figure 14. Block Diagram of 1K/2K/4K x 18 FIFO Memory Used in Width Expansion Configuration

### NOTE:

1. Flag detection is accomplished by monitoring the  $\overline{FF}$ ,  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{AEF}$  signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

## DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72021/031/041 can easily be adapted to applications when the requirements are for greater than 1K/2K/4K words. Figure 15 demonstrates Depth Expansion using three IDT72021/031/041s. Any depth can be attained by adding additional devices. The IDT72021/031/041 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ( $\overline{FL}$ ) control input.
2. All other devices must have  $\overline{FL}$  in the HIGH state.
3. The Expansion Out ( $\overline{XO}$ ) pin of each device must be tied to the Expansion In ( $\overline{XI}$ ) pin of the next device. See Figure 15.
4. External logic is needed to generate a composite Full Flag ( $\overline{FF}$ ) and Empty Flag ( $\overline{EF}$ ). This requires the ORing of all  $\overline{EF}$ s and ORing of all  $\overline{FF}$ s (i.e. all must be set to generate the correct composite  $\overline{FF}$  or  $\overline{EF}$ ). See Figure 15.
5. The Retransmit ( $\overline{RT}$ ) function and Half-Full Flag ( $\overline{HF}$ ) are not available in the Depth Expansion Mode. For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

## COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 16).

## BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72021/031/041s as shown in Figure 17. Care must be taken to assure that the appropriate flag is monitored by each system (i.e.,  $\overline{FF}$  is monitored on the device where  $\overline{W}$  is used;  $\overline{EF}$  is monitored on the device where  $\overline{R}$  is used). Both Depth Expansion and Width Expansion may be used in this mode.

## DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 18), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ( $t_{WEF} + t_A$ ) ns after the rising edge of  $\overline{W}$ , called the first write edge. It remains on the bus until the  $\overline{R}$  line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after  $t_{RHZ}$  ns. The  $\overline{EF}$  line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that  $\overline{R}$  was LOW, more words can be written to the FIFO (the subsequent writes after the first write edge will be deassert the Empty Flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when  $\overline{R}$  was LOW. On toggling  $\overline{R}$ , the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The  $\overline{R}$  line causes the  $\overline{FF}$  to be deasserted but the  $\overline{W}$  line, being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of  $\overline{W}$ , the new word is loaded in the FIFO. The  $\overline{W}$  line must be toggled when  $\overline{FF}$  is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TRUTH TABLES  
TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

| Mode       | Inputs          |                 |                 | Internal Status          |                          | Outputs         |                 |                 |                  |
|------------|-----------------|-----------------|-----------------|--------------------------|--------------------------|-----------------|-----------------|-----------------|------------------|
|            | $\overline{RS}$ | $\overline{RT}$ | $\overline{XI}$ | Read Pointer             | Write Pointer            | $\overline{EF}$ | $\overline{FF}$ | $\overline{HF}$ | $\overline{AEF}$ |
| Reset      | 0               | X               | 0               | Location Zero            | Location Zero            | 0               | 1               | 1               | 0                |
| Retransmit | 1               | 0               | 0               | Location Zero            | Unchanged                | X               | X               | X               | X                |
| Read/Write | 1               | 1               | 0               | Increment <sup>(1)</sup> | Increment <sup>(1)</sup> | X               | X               | X               | X                |

NOTE:  
1. Pointer will increment if flag is HIGH.

2677 tbl 11

TABLE II—RESET AND FIRST LOAD TRUTH TABLE  
Depth Expansion/Compound Expansion Mode

| Mode                    | Inputs          |                 |                 | Internal Status |               | Outputs         |                 |
|-------------------------|-----------------|-----------------|-----------------|-----------------|---------------|-----------------|-----------------|
|                         | $\overline{RS}$ | $\overline{FL}$ | $\overline{XI}$ | Read Pointer    | Write Pointer | $\overline{EF}$ | $\overline{FF}$ |
| Reset First Device      | 0               | 0               | (1)             | Location Zero   | Location Zero | 0               | 1               |
| Reset All Other Devices | 0               | 1               | (1)             | Location Zero   | Location Zero | 0               | 1               |
| Read/Write              | 1               | X               | (1)             | X               | X             | X               | X               |

NOTE:  
1.  $\overline{XI}$  is connected to  $\overline{XO}$  of previous device. See Figure 15.  $\overline{RS}$  = Reset Input  $\overline{FL}/\overline{RT}$  = First Load/Retransmit,  $\overline{EF}$  = Empty Flag Output,  $\overline{FF}$  = Flag Full Output,  $\overline{XI}$  = Expansion Input,  $\overline{HF}$  = Half-Full Flag Output,  $\overline{AEF}$  = Almost Empty/Almost Full Flag.

2677 tbl 12

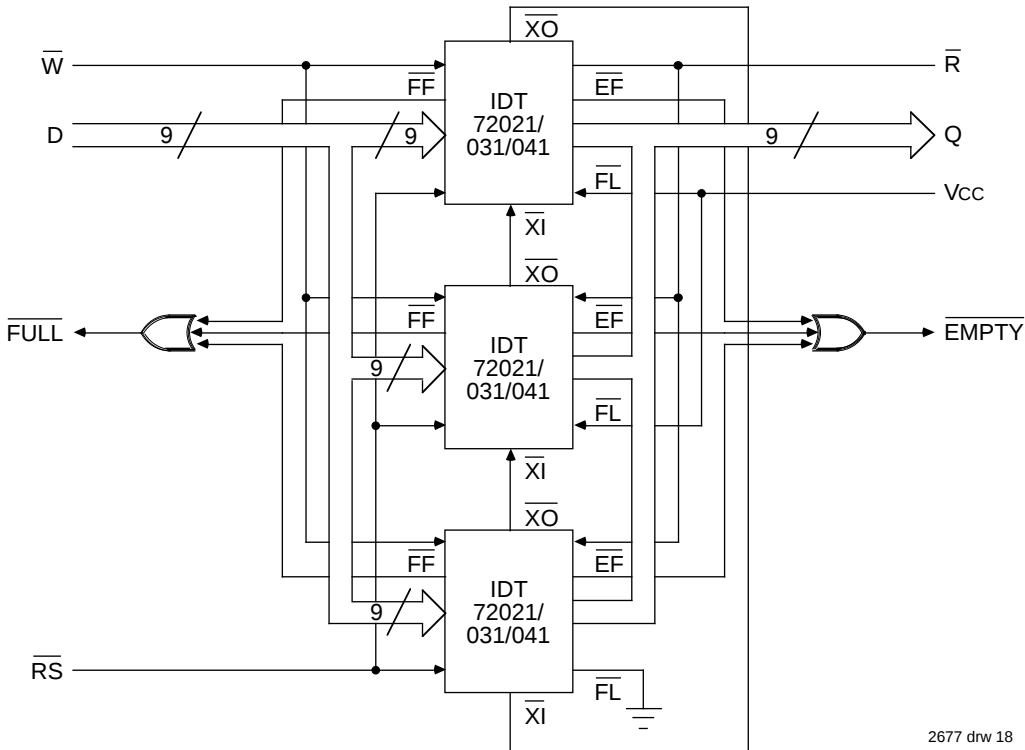
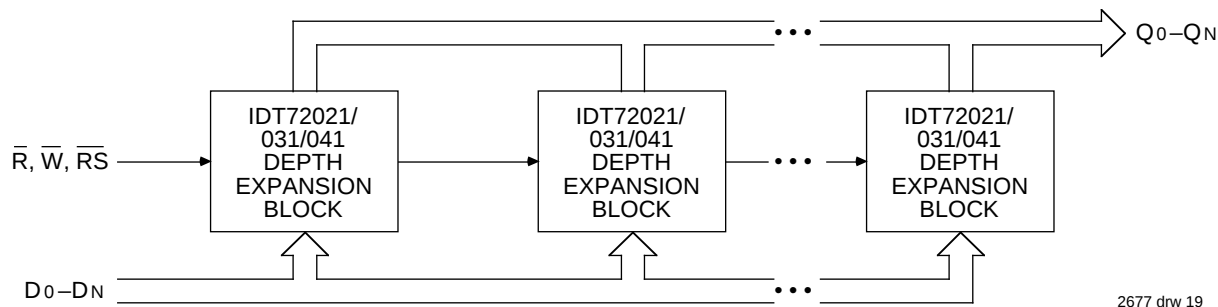


Figure 15. Block Diagram of 3K/6K/12K x 9 FIFO Memory (Depth Expansion)

NOTE:  
1. IDT only guarantees depth expansion with identical IDT part numbers and speed.

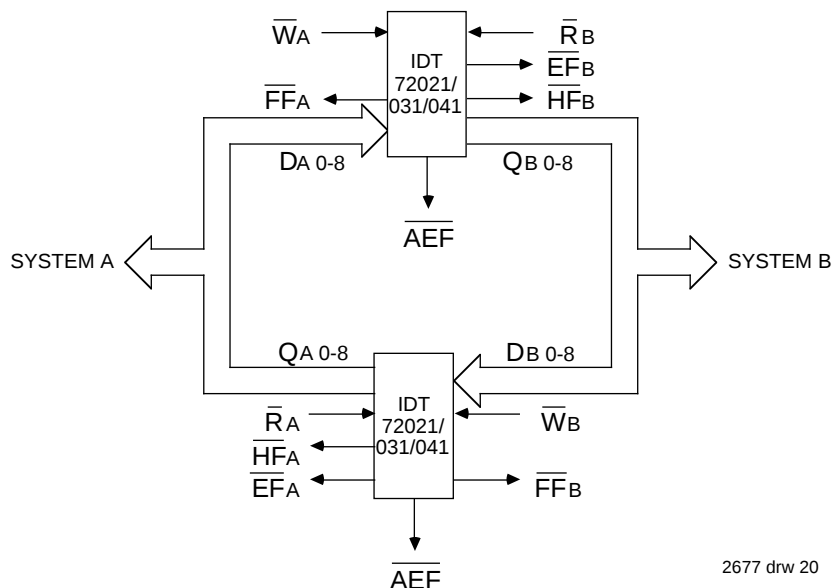


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Figure 16. Compound FIFO Expansion

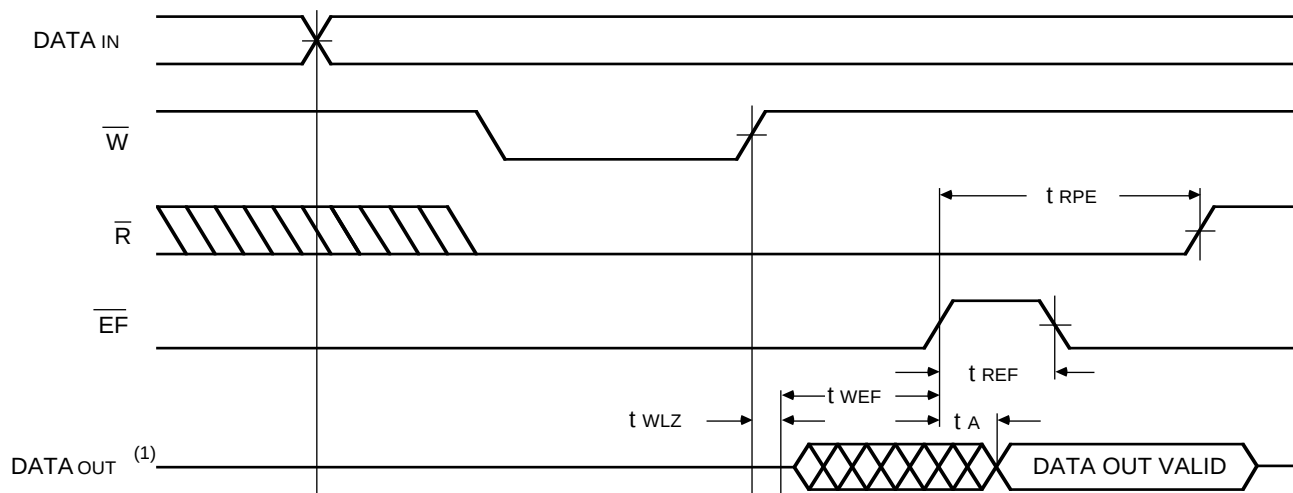
**NOTES:**

1. For depth expansion block see section od Depth Expansion and Figure 15.
2. For Flag detection see section on Width Expansion and Figure 14.



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Figure 17. Bidirectional FIFO Mode



2677 drw 21

Figure 18. Read Data Flow-Through Mode

**NOTE:**

1. Assume OE is asserted LOW.

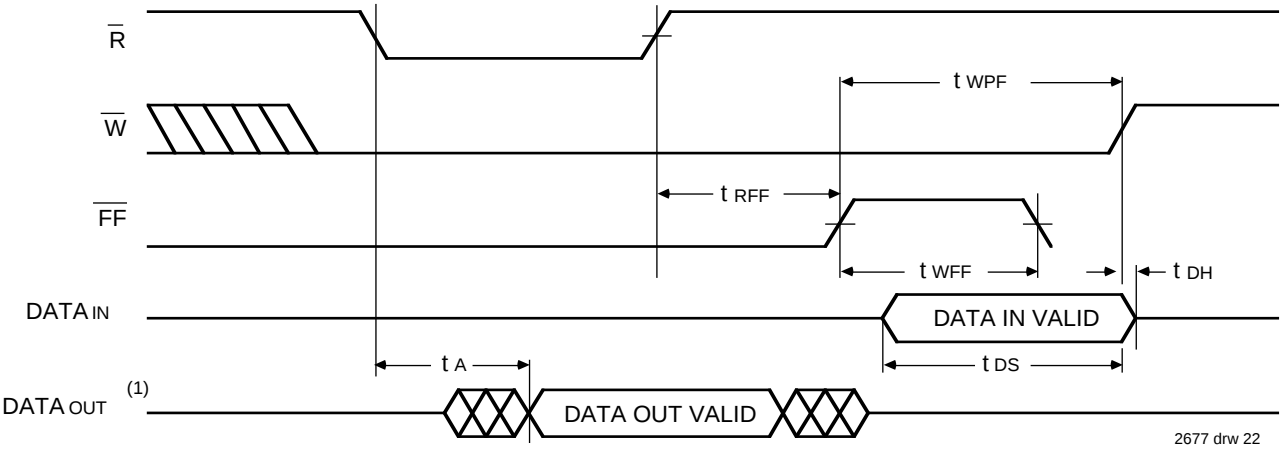


Figure 19. Write Data Flow-Through Mode

NOTE:  
1. Assume  $\overline{OE}$  is asserted LOW.

ORDERING INFORMATION

| IDT         | XXXXX | X     | X       | X                                | X                                                                                                                          |                                          |
|-------------|-------|-------|---------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| Device Type | Power | Speed | Package | Process/<br>Temperature<br>Range |                                                                                                                            |                                          |
|             |       |       |         | Blank                            | Commercial (0°C to +70°C)                                                                                                  |                                          |
|             |       |       |         | B                                | Military (−55°C to +125°C)<br>Compliant to MIL-STD-883, Class B                                                            |                                          |
|             |       |       |         | D<br>J                           | CERDIP<br>Plastic Leaded Chip Carrier                                                                                      |                                          |
|             |       |       |         | 25<br>30<br>35<br>40<br>50       | 72021—Com'l. Only<br>72021—Mil. Only<br>72021/031/041—Com'l. Only<br>72021/031/041—Mil. Only<br>72021/031/041—Com'l & Mil. | Access Time (tA)<br>Speed in Nanoseconds |
|             |       |       |         | L                                | Low Power                                                                                                                  |                                          |
|             |       |       |         | 72021<br>72031<br>72041          | 1024 x 9-Bit FIFO<br>2048 x 9-Bit FIFO<br>4096 x 9-Bit FIFO                                                                |                                          |