



3.3V CMOS 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

IDT74ALVC162835

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP and TVSOP packages

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

DESCRIPTION:

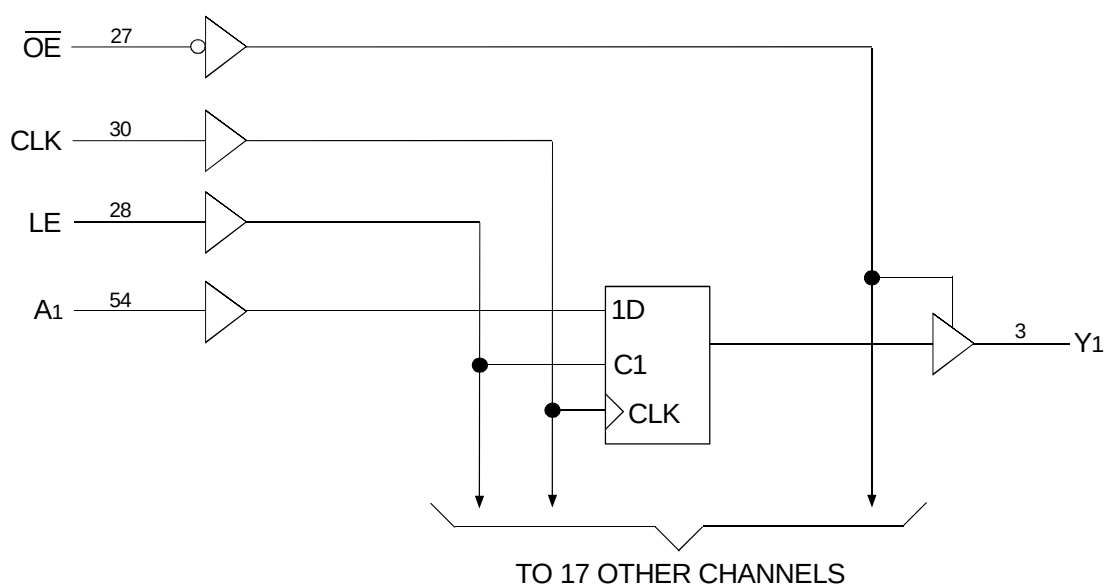
This 18-bit universal bus driver is built using advanced dual metal CMOS technology. Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The ALVC162835 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

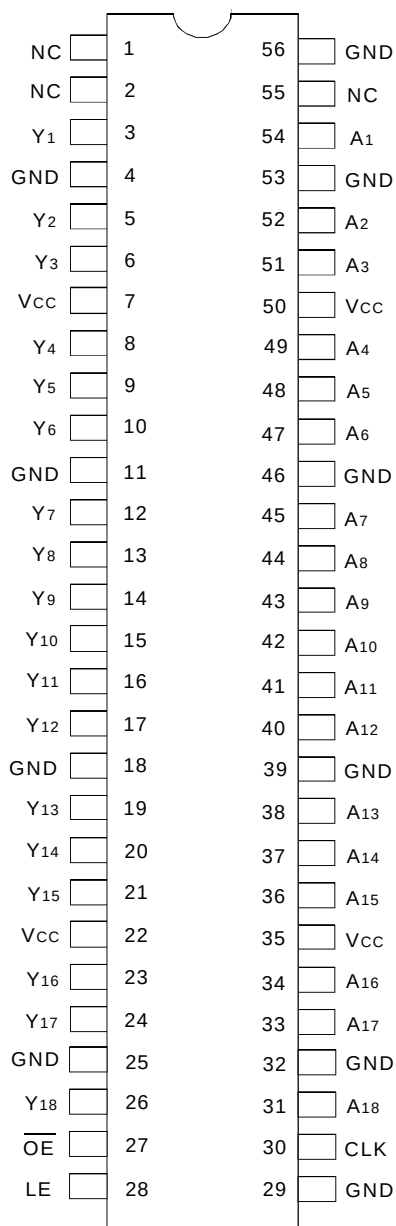
APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
LE	Latch Enable (Transparent HIGH)
Ax	Data Inputs
Yx	3-State Outputs
NC	No Internal Connection

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, $V_i < 0$ or $V_i > V_{CC}$	±50	mA
IOK	Continuous Clamp Current, $V_o < 0$	-50	mA
ICC ISS	Continuous Current through each VCC or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COU	Output Capacitance	VOU = 0V	7	9	pF
COU	I/O Port Capacitance	VIN = 0V	7	9	pF

NOTE:

- As applicable to the device type.

FUNCTION TABLE⁽¹⁾

Inputs				Outputs
$\overline{OE}$	LE	CLK	Ax	Yx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y ₀ ⁽²⁾
L	L	L	X	Y ₀ ⁽³⁾

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established, provided that CLK is HIGH before LE went LOW.
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	μA
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -4\text{mA}$	1.9	—	
			$I_{OH} = -6\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$	$I_{OH} = -4\text{mA}$	2.2	—	
			$I_{OH} = -8\text{mA}$	2	—	
		$V_{CC} = 3\text{V}$	$I_{OH} = -6\text{mA}$	2.4	—	
			$I_{OH} = -12\text{mA}$	2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 4\text{mA}$	—	0.4	
			$I_{OL} = 6\text{mA}$	—	0.55	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 4\text{mA}$	—	0.4	
			$I_{OL} = 8\text{mA}$	—	0.6	
		$V_{CC} = 3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.55	
			$I_{OL} = 12\text{mA}$	—	0.8	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
 $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Vcc = 2.5V $\pm$ 0.2V	Vcc = 3.3V $\pm$ 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	35.5	40	pF
CPD	Power Dissipation Capacitance Outputs disabled		12.5	14	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Vcc = 2.5V $\pm$ 0.2V		Vcc = 2.7V		Vcc = 3.3V $\pm$ 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fMAX		150	—	150	—	150	—	MHz
tPLH tPHL	Propagation Delay Ax to Yx	1	5	—	5	1	4.2	ns
tPLH tPHL	Propagation Delay LE to Yx	1.3	5.9	—	5.8	1.3	5.1	ns
tPLH tPHL	Propagation Delay CLK to Yx	1.4	6.3	—	6.1	1.4	5.4	ns
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to Yx	1.4	6.3	—	6.5	1.1	5.5	ns
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to Yx	1	4.9	—	4.9	1.3	4.5	ns
tW	Pulse Duration, LE LOW	3.3	—	3.3	—	3.3	—	ns
tW	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tSU	Set-up Time, data before CLK $\uparrow$	2.2	—	2.1	—	1.7	—	ns
tSU	Set-up Time, data before LE $\downarrow$, CLK HIGH	1.9	—	1.6	—	1.5	—	ns
tSU	Set-up Time, data before LE $\downarrow$, CLK LOW	1.3	—	1.5	—	1	—	ns
tH	Hold Time, data after CLK $\uparrow$	0.6	—	0.6	—	0.7	—	ns
tH	Hold Time, data after LE $\downarrow$, CLK HIGH or LOW	1.4	—	1.7	—	1.4	—	ns
tSK(O)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction.

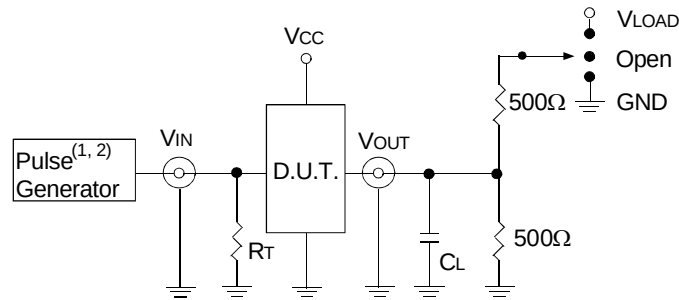
SWITCHING CHARACTERISTICS FROM 0°C TO 65°C , CL = 5pF

Symbol	Parameter	Vcc = 3.3V $\pm$ 0.15V		Unit
		Min.	Max.	
tPLH tPHL	Propagation Delay CLK to xYx	1.9	5	ns

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

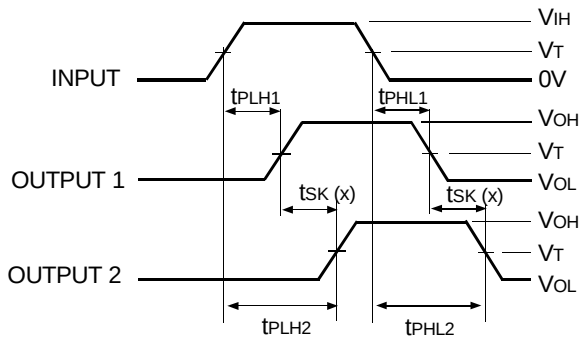
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open

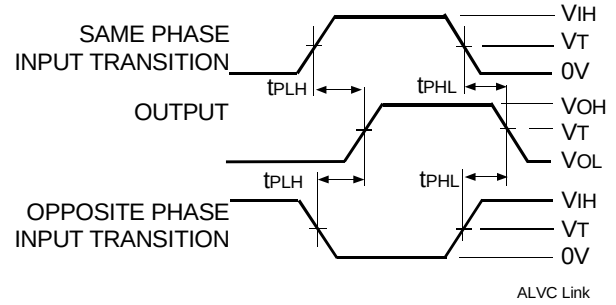


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

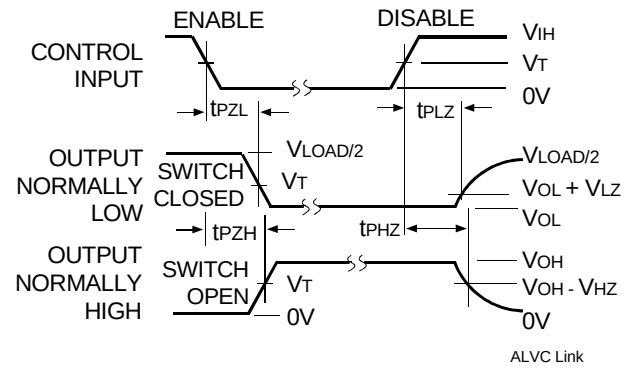
Output Skew - t_{sk}(x)

NOTES:

1. For t_{sk}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{sk}(b) OUTPUT1 and OUTPUT2 are in the same bank.



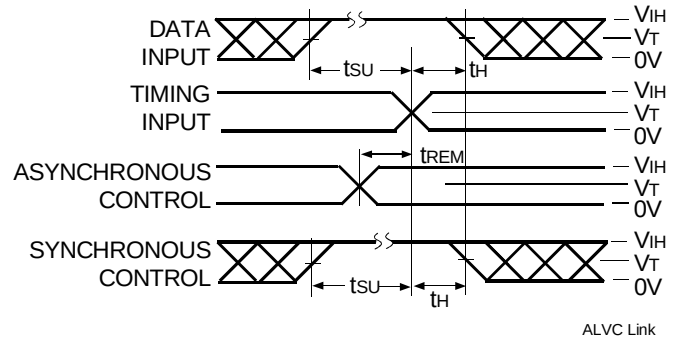
Propagation Delay



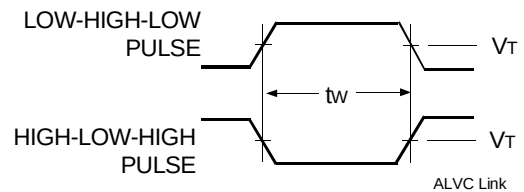
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
Temp. Range			Bus-Hold	Family	Device Type	Package	
						PA	Thin Shrink Small Outline Package
						PF	Thin Very Small Outline Package
					835		18-Bit Universal Bus Driver with 3-State Outputs
				162			Double-Density with Resistors, $\pm 12\text{mA}$
			Blank				No Bus-Hold
				74			-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459