



HIGH-SPEED CMOS 8-BIT TRANSCEIVER

IDTQS74FCT2245T/AT/CT

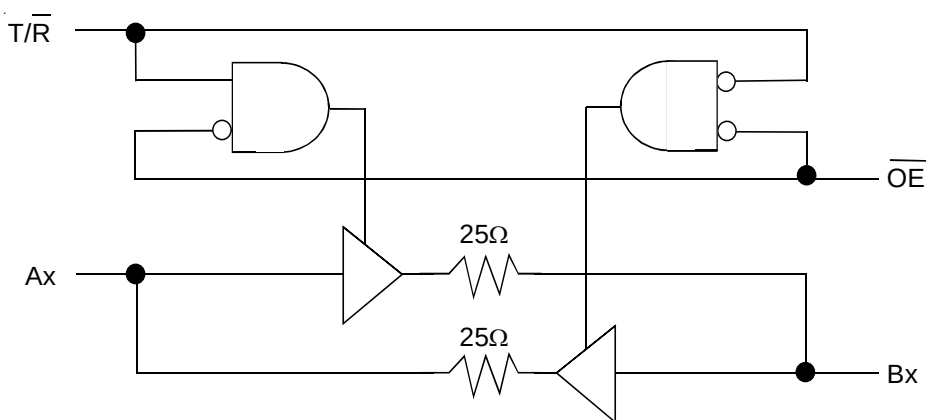
FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades with 4.1ns t_{PD} for C
- I_{OL} = 12mA
- Available in SOIC and QSOP packages

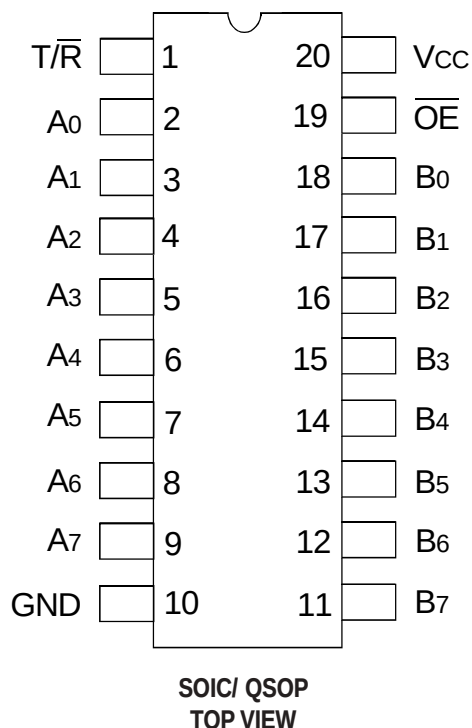
DESCRIPTION:

The IDTQS74FCT2245T is an 8-bit non-inverting transceiver that has three-state outputs, ideal for bus-oriented applications. The Transmit/Receive (T/ $\bar{R}$) input determines the direction of data flow, either from A to B or B to A, and the Output Enable ($\overline{OE}$) input enables the selected port for output. The QS74FCT2245 has a 25Ω resistor output that is useful for driving transmission lines and reducing system noise. The QS74FCT2245 parts can replace the 245 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current Max Current Sink/Pin	+120	mA
I _{IK}	Input Diode Current, V _{IN} < 0	-20	mA
I _{OK}	DC Output Current, V _{OUT} < 0	-50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4	—	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	—	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
A _x	I/O	Data Bus A
B _x	I/O	Data Bus B
T/ $\overline{R}$	I	Direction
$\overline{OE}$	I	Output Enable Input (Active LOW)

FUNCTION TABLE⁽¹⁾

$\overline{OE}$	T/ $\overline{R}$	A	B	Function
H	X	Z	Z	Disable
L	L	Output	Input	Bus B to Bus A
L	H	Input	Output	Bus A to Bus B

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current						
I_{OZ}	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	± 5	μA
I_{OR}	Current Drive	$V_{CC} = \text{Max.}, V_{OUT} = 2V^{(2)}$		50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^{\circ}\text{C}^{(2)}$		—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	—	—	0.5	V
R_{OUT}	Output Resistance	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	20	28	40	Ω

NOTES:

- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ $\text{freq} = 0$	—	2	mA
I_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under DC Electrical Characteristics.
 - Per TTL driven input ($V_{IN} = 3.4\text{V}$).
 - For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
 - $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4\text{V})$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Output Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Output Frequency}$
 $N_i = \text{Number of Outputs at } f_i$
- All currents are in milliamps and all frequencies are in megahertz.

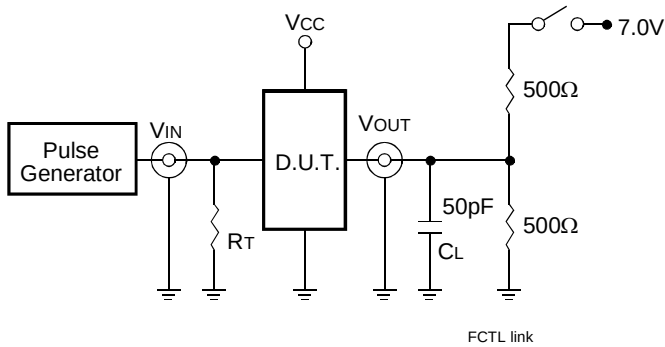
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter ⁽²⁾	74FCT2245T		74FCT2245AT		74FCT2245CT		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	1.5	7	1.5	4.6	1.5	4.1	ns
t _{PHL}	Ax to/from Bx							
t _{PZH}	Output Enable Time	1.5	9.5	1.5	6.2	1.5	5.8	ns
t _{PZL}	$\overline{OE}$, T/ $\overline{R}$ to A/B							
t _{PHZ}	Output Disable Time ⁽³⁾	1.5	7.5	1.5	5	1.5	4.5	ns
t _{PLZ}	$\overline{OE}$, T/ $\overline{R}$ to A/B							

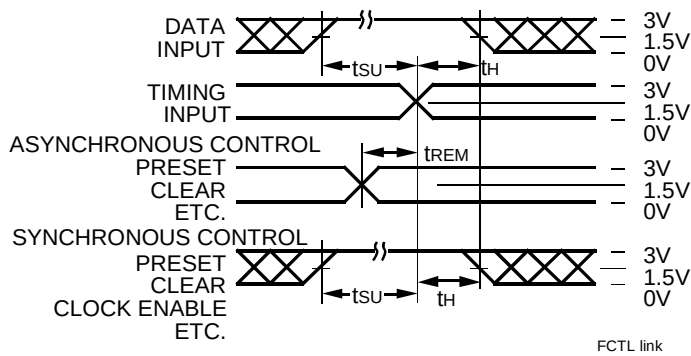
NOTES:

1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

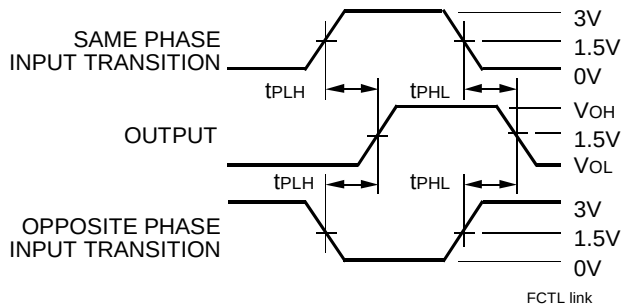
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



Propagation Delay

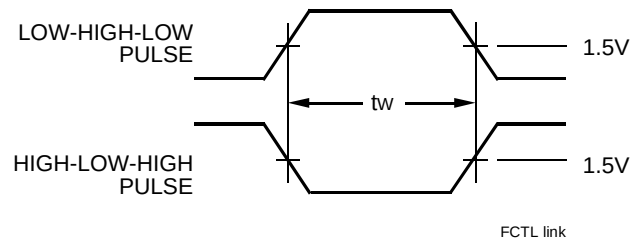
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

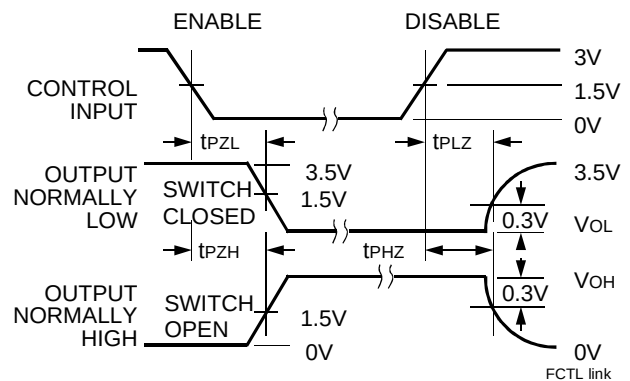
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDTQS	XX	FCT	XXXX	XX	
	Temp. Range		Device Type	Package	
				SO	Small Outline IC (gull wing)
				Q	Quarter Size Small Outline Package
			2245T		High-Speed CMOS 8-Bit Transceiver
			2245AT		
			2245CT		
			74		–40°C to +85°C



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