

## DESCRIPTION

THE Hynix HY57V161610E is a 16,777,216-bits CMOS Synchronous DRAM, ideally suited for the main memory and graphic applications which require large memory density and high bandwidth. HY57V161610E is organized as 2banks of 524,288x16.

HY57V161610E is offering fully synchronous operation referenced to a positive edge clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 1,2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipeline design is not restricted by a '2N' rule.)

## FEATURES

- Single 3.0V to 3.6V power supply
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 50pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM/LDQM
- Internal two banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 and Full Page for Sequence Burst
  - 1, 2, 4 and 8 for Interleave Burst
- Programmable  $\overline{\text{CAS}}$  Latency ; 1, 2, 3 Clocks

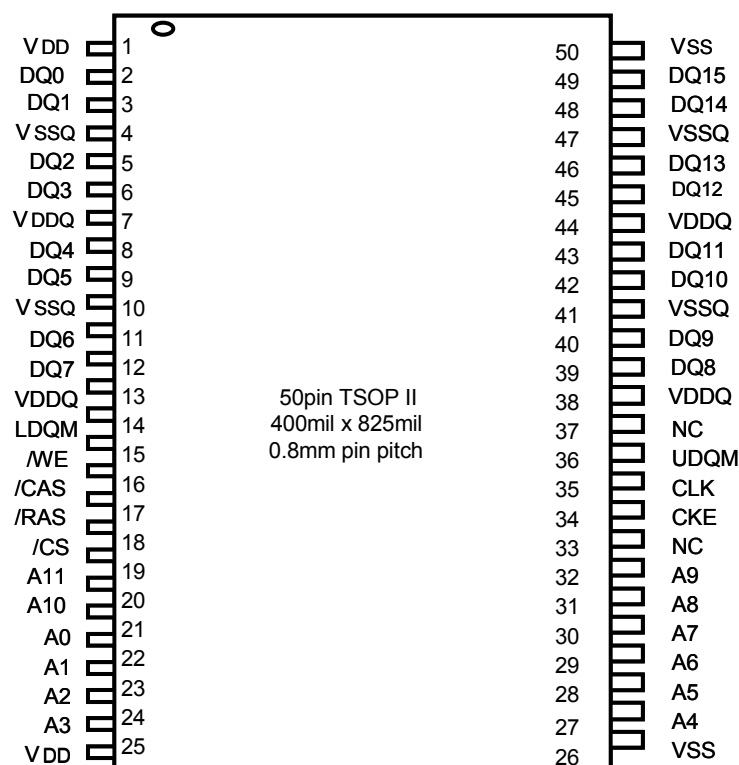
## ORDERING INFORMATION

| Part No.         | Clock Frequency | Organization           | Interface | Package                 |
|------------------|-----------------|------------------------|-----------|-------------------------|
| HY57V161610ET-5  | 200MHz          | 2Banks x 512Kbits x 16 | LVTTL     | 400mil<br>50pin TSOP II |
| HY57V161610ET-55 | 183MHz          |                        |           |                         |
| HY57V161610ET-6  | 166MHz          |                        |           |                         |
| HY57V161610ET-7  | 143MHz          |                        |           |                         |
| HY57V161610ET-8  | 125MHz          |                        |           |                         |
| HY57V161610ET-10 | 100MHz          |                        |           |                         |
| HY57V161610ET-15 | 66MHz           |                        |           |                         |

Note :

1. VDD(min) of HY57V161610ET-5/55 is 3.15V

## PIN CONFIGURATION

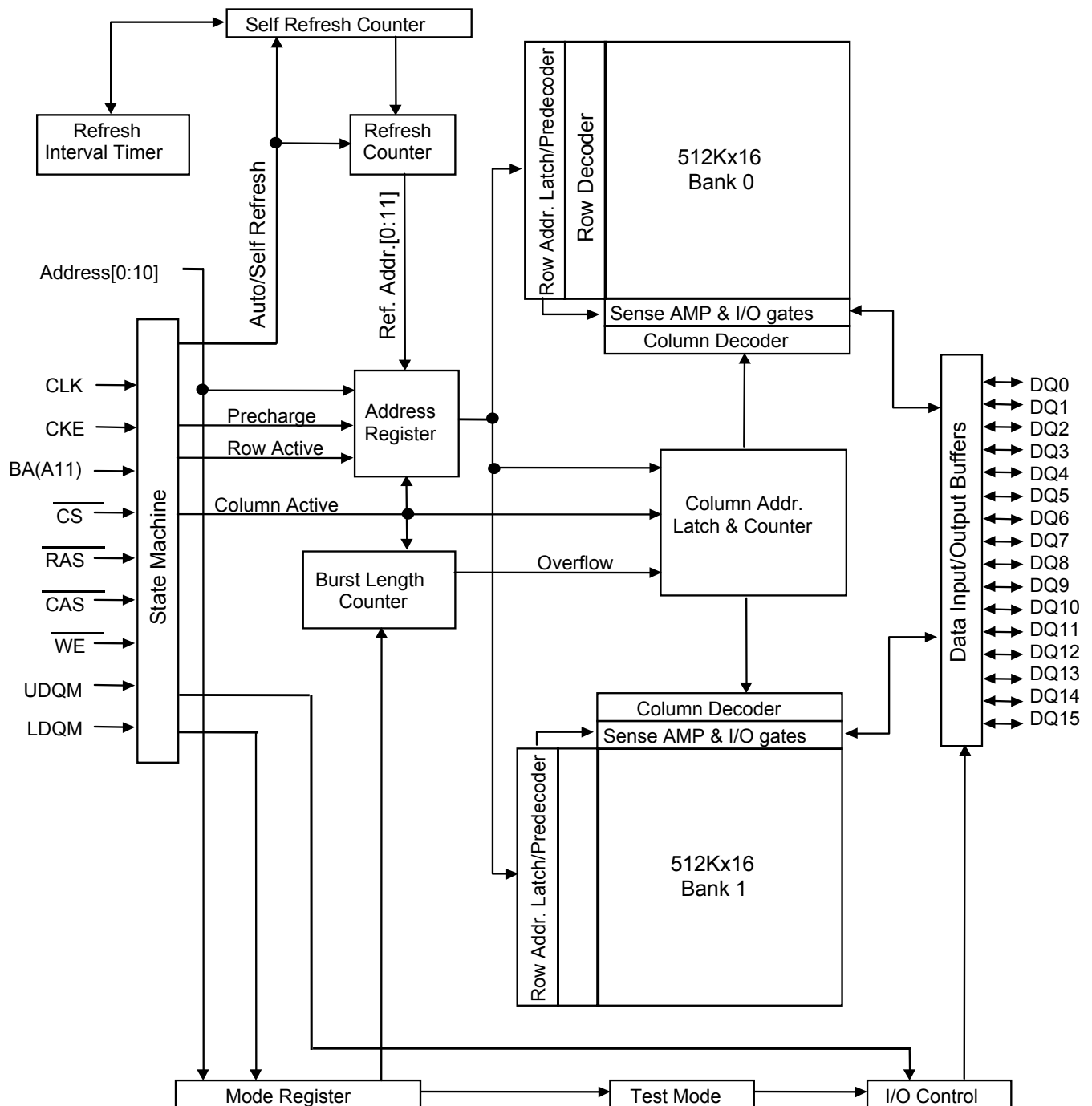


## PIN DESCRIPTION

| PIN                                                                        | PIN NAME                                                | DESCRIPTION                                                                                                                                  |
|----------------------------------------------------------------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| CLK                                                                        | Clock                                                   | The system clock input. All other inputs are referenced to the SDRAM on the rising edge of CLK.                                              |
| CKE                                                                        | Clock Enable                                            | Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.          |
| $\overline{\text{CS}}$                                                     | Chip Select                                             | Command input enable or mask except CLK, CKE and DQM                                                                                         |
| BA                                                                         | Bank Address                                            | Select either one of banks during both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ activity.                                         |
| A0 ~ A10                                                                   | Address                                                 | Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7<br>Auto-precharge flag : A10                                                            |
| $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ | Row Address Strobe, Column Address Strobe, Write Enable | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation.<br>Refer function truth table for details |
| LDQM, UDQM                                                                 | Data Input/Output Mask                                  | DQM control output buffer in read mode and mask input data in write mode                                                                     |
| DQ0 ~ DQ15                                                                 | Data Input/Output                                       | Multiplexed data input / output pin                                                                                                          |
| VDD/VSS                                                                    | Power Supply/Ground                                     | Power supply for internal circuit and input buffer                                                                                           |
| VDDQ/VSSQ                                                                  | Data Output Power/Ground                                | Power supply for DQ                                                                                                                          |
| NC                                                                         | No Connection                                           | No connection                                                                                                                                |

## FUNCTIONAL BLOCK DIAGRAM

1Mx16 Synchronous DRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter                          | Symbol    | Rating     | Unit    |
|------------------------------------|-----------|------------|---------|
| Ambient Temperature                | TA        | 0 ~ 70     | °C      |
| Storage Temperature                | TSTG      | -55 ~ 125  | °C      |
| Voltage on Any Pin relative to VSS | VIN, VOUT | -1.0 ~ 4.6 | V       |
| Voltage on VDD relative to VSS     | VDD       | -1.0 ~ 4.6 | V       |
| Short Circuit Output Current       | IOS       | 50         | mA      |
| Power Dissipation                  | PD        | 1          | W       |
| Soldering Temperature-Time         | TSOLDER   | 260-10     | °C ·Sec |

Note : Operation at above absolute maximum rating can adversely affect device reliability.

## DC OPERATING CONDITION (TA=0°C to 70°C)

| Parameter            | Symbol    | Min  | Typ. | Max       | Unit | Note    |
|----------------------|-----------|------|------|-----------|------|---------|
| Power Supply Voltage | VDD, VDDQ | 3.0  | 3.3  | 3.6       | V    | 1, 2, 3 |
| Input high voltage   | VIH       | 2.0  | 3.0  | VDD + 0.3 | V    | 1, 4    |
| Input low voltage    | VIL       | -0.3 | 0    | 0.8       | V    | 1, 5    |

Note :

1. All voltages are referenced to VSS = 0V.
2. VDD(min) is 3.15V when HY57V161610ET-7 operates at  $\overline{\text{CAS}}$  latency=2
3. VDD(min) of HY57V161610ET-5/55 is 3.15V
4. VIH(Max) : 4.6V AC pulse width with < 3ns of duration.
5. VIL(min) : -1.5V AC pulse width with < 3ns of duration.

## AC OPERATING CONDITION (TA=0°C to 70°C, VDD=3.0V to 3.6V, VSS=0V)

| Parameter                                           | Symbol    | Value   | Unit | Note |
|-----------------------------------------------------|-----------|---------|------|------|
| AC input high / low level voltage                   | VIH / VIL | 2.4/0.4 | V    |      |
| Input timing measurement reference level voltage    | Vtrip     | 1.4     | V    |      |
| Input rise / fall time                              | tR / tF   | 1       | ns   |      |
| Output timing measurement reference level           | Voutref   | 1.4     | V    |      |
| Output load capacitance for access time measurement | CL        | 30      | pF   | 1    |

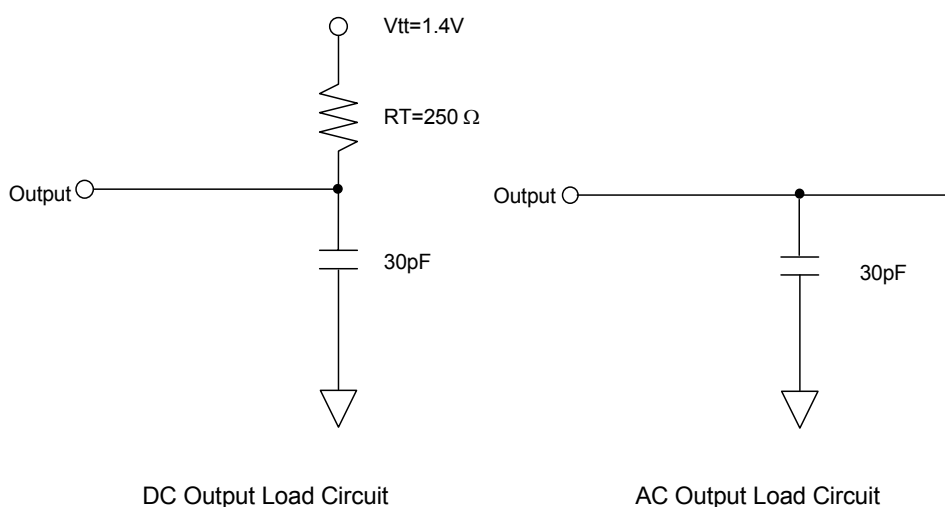
Note :

1. Output load to measure access times is equivalent to two TTL gates and one capacitance(30pF).  
For details, refer to AC/DC output load circuit.
2. VDD(min) is 3.15V when HY57V161610ET-7 operates at  $\overline{\text{CAS}}$  latency=2 and tCK2=8.9ns
3. VDD(min) of HY57V161610ET-5/55 is 3.15V

## CAPACITANCE (TA=25°C, f=1MHz)

| Parameter                       | Pin                                             | Symbol | Min | Max | Unit |
|---------------------------------|-------------------------------------------------|--------|-----|-----|------|
| Input capacitance               | CLK                                             | Cl1    | 2.5 | 4   | pF   |
|                                 | A0 ~ A10, BA, CKE, CS, RAS, CAS, WE, UDQM, LDQM | Cl2    | 2.5 | 5   | pF   |
| Data input / output capacitance | DQ0 ~ DQ15                                      | Cl/O   | 4   | 6.5 | pF   |

## OUTPUT LOAD CIRCUIT



## DC CHARACTERISTICS I (TA=0°C to 70°C)

| Parameter              | Symbol | Min. | Max | Unit | Note       |
|------------------------|--------|------|-----|------|------------|
| Power Supply Voltage   | VDD    | 3.0  | 3.6 | V    | 1, 2       |
| Input leakage current  | IL     | -1   | 1   | uA   | 3          |
| Output leakage current | IO     | -1   | 1   | uA   | 4          |
| Output high voltage    | VOH    | 2.4  | -   | V    | IOH = -4mA |
| Output low voltage     | VOL    | -    | 0.4 | V    | IOL = +4mA |

Note :

- 1.VDD(min) is 3.15V when HY57V161610ET-7 operates at  $\overline{\text{CAS}}$  latency=2 and tCK2=8.9ns.
- 2.VDD(min) of HY57V161610ET-5/55 is 3.15V
- 3.VIN = 0 to 3.6V, All other pins are not under test = 0V
- 4.DOUT is disabled, VOUT=0 to 3.6V

**DC CHARACTERISTICS II** (TA=0°C to 70°C, VDD=3.0V to 3.6V, VSS=0V<sup>Note1,2)</sup>

| Parameter                                           | Symbol | Test Condition                                                                                                                                 |      | Speed |     |     |     |     |     |     | Unit | Note |  |
|-----------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|-----|-----|-----|-----|-----|-----|------|------|--|
|                                                     |        |                                                                                                                                                |      | -5    | -55 | -6  | -7  | -8  | -10 | -15 |      |      |  |
| Operating Current                                   | IDD1   | Burst Length=1, One bank active<br>tRAS ≥ tRAS(min),tRP ≥ tRP(min),<br>IO=0mA                                                                  |      | 130   | 130 | 120 | 110 | 110 | 110 | 100 | mA   | 2    |  |
| Precharge Standby Current<br>in power down mode     | IDD2P  | CKE ≤ VIL(max), tCK = 15ns                                                                                                                     |      | 2     |     |     |     |     |     |     | mA   |      |  |
|                                                     | IDD2PS | CKE ≤ VIL(max), tCK = ∞                                                                                                                        |      | 1     |     |     |     |     |     |     |      |      |  |
| Precharge Standby Current<br>in non power down mode | IDD2N  | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns<br>Input signals are changed one time during 2Clks. All other pins ≥ VDD-0.2V or ≤ 0.2V |      | 25    |     |     |     |     |     |     | mA   |      |  |
|                                                     | IDD2NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable.                                                                                           |      | 15    |     |     |     |     |     |     |      |      |  |
| Active Standby Current<br>in power down mode        | IDD3P  | CKE ≤ VIL(max), tCK = min                                                                                                                      |      | 3.0   |     |     |     |     |     |     | mA   |      |  |
|                                                     | IDD3PS | CKE ≤ VIL(max), tCK = ∞                                                                                                                        |      | 3.0   |     |     |     |     |     |     |      |      |  |
| Active Standby Current<br>in non power down mode    | IDD3N  | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = min<br>Input signals are changed one time during 2CLKs. All other pins ≥ VDD-0.2V or ≤ 0.2V  |      | 50    |     |     |     |     |     |     | mA   |      |  |
|                                                     | IDD3NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable                                                                                            |      | 30    |     |     |     |     |     |     |      |      |  |
| Burst Mode Operating Current                        | IDD4   | tCK ≥ tCK(min),<br>tRAS ≥ tRAS(min),<br>IO=0mA<br>All banks active                                                                             | CL=3 | 130   | 130 | 120 | 110 | 110 | 90  | 80  | mA   | 3    |  |
|                                                     |        |                                                                                                                                                | CL=2 | -     | -   | 110 | 110 | -   | -   | -   |      |      |  |
|                                                     |        |                                                                                                                                                | CL=1 | -     | -   | -   | -   | -   | -   | 70  |      |      |  |
| Auto Refresh Current                                | IDD5   | tRRC ≥ tRRC(min), All banks active                                                                                                             |      | 130   | 130 | 110 | 110 | 110 | 110 | 100 | mA   |      |  |
| Self Refresh Current                                | IDD6   | CKE ≤ 0.2V                                                                                                                                     |      | 2     |     |     |     |     |     |     |      | mA   |  |

Note :

1.VDD(min) is 3.15V when HY57V161610ET-7 operates at  $\overline{CAS}$  latency=2 and tCK2=8.9ns.

2.VDD(min) of HY57V161610ET-5/55 is 3.15V

3.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.

**AC CHARACTERISTICS** (TA=0°C to 70°C, VDD=3.0V to 3.6V, VSS=0V<sup>Note1,2)</sup>

| Parameter                         |      | Symbol | -5  |     | -55 |     | -6  |     | -7   |     | Unit | Note |
|-----------------------------------|------|--------|-----|-----|-----|-----|-----|-----|------|-----|------|------|
|                                   |      |        | Min | Max | Min | Max | Min | Max | Min  | Max |      |      |
| System clock cycle time           | CL=3 | tCK3   | 5   |     | 5.5 |     | 6   | -   | 7    | -   | ns   | 3    |
|                                   | CL=2 | tCK2   | -   |     | -   |     | 10  | -   | 10   | -   |      |      |
|                                   | CL=1 | tCK1   | -   |     | -   |     | -   | -   | -    | -   |      |      |
| Clock high pulse width            |      | tCHW   | 2   |     | 2   |     | 2   | -   | 2.5  | -   | ns   | 4    |
| Clock low pulse width             |      | tCLW   | 2   |     | 2   |     | 2   | -   | 2.5  | -   | ns   | 4    |
| Access time from clock            | CL=3 | tAC3   |     | 4.5 |     | 5   | -   | 5.5 | -    | 6   | ns   | 3    |
|                                   | CL=2 | tAC2   |     |     |     |     | -   | 6   | -    | 6   |      |      |
|                                   | CL=1 | tAC1   |     |     |     |     | -   | -   | -    | -   |      |      |
| Data-out hold time                |      | tOH    | 1.5 |     | 2   |     | 2   | -   | 2.5  | -   | ns   |      |
| Data-Input setup time             |      | tDS    | 1.5 |     | 1.5 |     | 1.5 | -   | 1.75 | -   | ns   | 4    |
| Data-Input hold time              |      | tDH    | 1   |     | 1   |     | 1   | -   | 1    | -   | ns   | 4    |
| Address setup time                |      | tAS    | 1.5 |     | 1.5 |     | 1.5 | -   | 1.75 | -   | ns   | 4    |
| Address hold time                 |      | tAH    | 1   |     | 1   |     | 1   | -   | 1    | -   | ns   | 4    |
| CKE setup time                    |      | tCKS   | 1.5 |     | 1.5 |     | 1.5 | -   | 1.75 | -   | ns   | 4    |
| CKE hold time                     |      | tCKH   | 1   |     | 1   |     | 1   | -   | 1    | -   | ns   | 4    |
| Command setup time                |      | tCS    | 1.5 |     | 1.5 |     | 1.5 | -   | 1.75 | -   | ns   | 4    |
| Command hold time                 |      | tCH    | 1   |     | 1   |     | 1   | -   | 1    | -   | ns   | 4    |
| CLK to data output in low Z-time  |      | tOLZ   | 2   |     | 2   |     | 2   | -   | 2    | -   | ns   |      |
| CLK to data output in high Z-time |      | tOHZ   | 2   | 5   | 2   | 5.5 | 2   | 6   | 2    | 7   | ns   |      |

**AC CHARACTERISTICS** (TA=0°C to 70°C, VDD=3.0V to 3.6V, VSS=0V<sup>Note1,2)</sup>
*- continued -*

| Parameter                         |      | Symbol | -8  |     | -10 |     | -15 |     | Unit | Note |
|-----------------------------------|------|--------|-----|-----|-----|-----|-----|-----|------|------|
|                                   |      |        | Min | Max | Min | Max | Min | Max |      |      |
| System clock cycle time           | CL=3 | tCK3   | 8   | -   | 10  | -   | 15  | -   | ns   | 3    |
|                                   | CL=2 | tCK2   | 12  | -   | 12  | -   | 15  | -   |      |      |
|                                   | CL=1 | tCK1   | -   | -   | -   | -   | 15  | -   |      |      |
| Clock high pulse width            |      | tCHW   | 3   | -   | 3   | -   | 3   | -   | ns   | 4    |
| Clock low pulse width             |      | tCLW   | 3   | -   | 3   | -   | 3   | -   | ns   | 4    |
| Access time from clock            | CL=3 | tAC3   | -   | 6   | -   | 7   | -   | 7   | ns   | 3    |
|                                   | CL=2 | tAC2   | -   | 6   | -   | 7   | -   | 7   |      |      |
|                                   | CL=1 | tAC1   | -   | -   | -   | -   | -   | 14  |      |      |
| Data-out hold time                |      | tOH    | 2.5 | -   | 2.5 | -   | 2.5 | -   | ns   |      |
| Data-Input setup time             |      | tDS    | 2   | -   | 2.5 | -   | 2.5 | -   | ns   | 4    |
| Data-Input hold time              |      | tDH    | 1   | -   | 1   | -   | 1   | -   | ns   | 4    |
| Address setup time                |      | tAS    | 2   | -   | 2.5 | -   | 2.5 | -   | ns   | 4    |
| Address hold time                 |      | tAH    | 1   | -   | 1   | -   | 1   | -   | ns   | 4    |
| CKE setup time                    |      | tCKS   | 2   | -   | 2.5 | -   | 2.5 | -   | ns   | 4    |
| CKE hold time                     |      | tCKH   | 1   | -   | 1   | -   | 1   | -   | ns   | 4    |
| Command setup time                |      | tCS    | 2   | -   | 2.5 | -   | 2.5 | -   | ns   | 4    |
| Command hold time                 |      | tCH    | 1   | -   | 1   | -   | 1   | -   | ns   | 4    |
| CLK to data output in low Z-time  |      | tOLZ   | 2   | -   | 2   | -   | 2   | -   | ns   |      |
| CLK to data output in high Z-time |      | tOHZ   | 2   | 8   | 3   | 10  | 3   | 15  | ns   |      |

**Note :**

- 1.VDD(min) is 3.15V when HY57V161610ET-7 operates at  $\overline{\text{CAS}}$  latency=2 and tCK2=8.9ns.
- 2.VDD(min) of HY57V161610ET-5/55 is 3.15V
- 3.tCK2 is 8.9ns only when tAC2 is 7.9ns in HY57V161610ET-6 and HY57V161610ET-7.
- 4.Assume tR / tF (input rise and fall time ) is 1ns.

**AC CHARACTERISTICS** (TA=0°C to 70°C, VDD=3.0V to 3.6V, VSS=0V<sup>Note1,2)</sup>)

| Paramter                                                             |              | Symbol | -5  |      | -55  |      | -6  |      | -7  |      | Unit | Note |
|----------------------------------------------------------------------|--------------|--------|-----|------|------|------|-----|------|-----|------|------|------|
|                                                                      |              |        | Min | Max  | Min  | Max  | Min | Max  | Min | Max  |      |      |
| $\overline{\text{RAS}}$ cycle time                                   | Operation    | tRC    | 55  |      | 55   |      | 60  | -    | 70  | -    | ns   |      |
|                                                                      | Auto Refresh | tRRC   | 55  |      | 55   |      | 60  | -    | 70  | -    | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay             |              | tRCD   | 15  |      | 16.5 |      | 18  | -    | 20  | -    | ns   |      |
| $\overline{\text{RAS}}$ active time                                  |              | tRAS   | 40  | 100K | 38.5 | 100K | 40  | 100K | 45  | 100K | ns   |      |
| $\overline{\text{RAS}}$ precharge time                               |              | tRP    | 3   |      | 3    |      | 3   | -    | 3   | -    | CLK  |      |
| $\overline{\text{RAS}}$ to $\overline{\text{RAS}}$ bank active delay |              | tRRD   | 2   |      | 2    |      | 2   | -    | 2   | -    | CLK  |      |
| $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ bank active delay |              | tCCD   | 1   |      | 1    |      | 1   | -    | 1   | -    | CLK  |      |
| Write command to data-in delay                                       |              | tWTL   | 0   |      | 0    |      | 0   | -    | 0   | -    | CLK  |      |
| Data-in to precharge command                                         |              | tDPL   | 1   |      | 1    |      | 1   | -    | 1   | -    | CLK  |      |
| Data-in to active command                                            |              | tDAL   | 5   |      | 4    |      | 4   | -    | 4   | -    | CLK  |      |
| DQM to data-in Hi-Z                                                  |              | tDQZ   | 2   |      | 2    |      | 2   | -    | 2   | -    | CLK  |      |
| DQM to data mask                                                     |              | tDQM   | 0   |      | 0    |      | 0   | -    | 0   | -    | CLK  |      |
| MRS to new command                                                   |              | tMRD   | 2   |      | 2    |      | 2   | -    | 2   | -    | CLK  |      |
| Precharge to data output Hi-Z                                        |              | tPROZ  | 3   |      | 3    |      | 3   | -    | 3   | -    | CLK  |      |
| Power down exit time                                                 |              | tPDE   | 1   |      | 1    |      | 1   | -    | 1   | -    | CLK  |      |
| Self refresh exit time                                               |              | tSRE   | 1   |      | 1    |      | 1   | -    | 1   | -    | CLK  | 3    |
| Refresh Time                                                         |              | tREF   |     | 64   |      | 64   | -   | 64   | -   | 64   | ms   |      |

**AC CHARACTERISTICS** (TA=0°C to 70°C, VDD=3.0V to 3.6V, VSS=0V<sup>Note1,2)</sup>
**- continued**

| Paramter                                                             |              | Symbol | -8  |      | -10 |      | -15 |      | Unit | Note |
|----------------------------------------------------------------------|--------------|--------|-----|------|-----|------|-----|------|------|------|
|                                                                      |              |        | Min | Max  | Min | Max  | Min | Max  |      |      |
| $\overline{\text{RAS}}$ cycle time                                   | Operation    | tRC    | 70  | -    | 70  | -    | 70  | -    | ns   |      |
|                                                                      | Auto Refresh | tRRC   | 70  | -    | 80  | -    | 80  | -    | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay             |              | tRCD   | 20  | -    | 20  | -    | 20  | -    | ns   |      |
| $\overline{\text{RAS}}$ active time                                  |              | tRAS   | 45  | 100K | 45  | 100K | 45  | 100K | ns   |      |
| $\overline{\text{RAS}}$ precharge time                               |              | tRP    | 3   | -    | 2   | -    | 2   | -    | CLK  |      |
| $\overline{\text{RAS}}$ to $\overline{\text{RAS}}$ bank active delay |              | tRRD   | 2   | -    | 2   | -    | 2   | -    | CLK  |      |
| $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ bank active delay |              | tCCD   | 1   | -    | 1   | -    | 1   | -    | CLK  |      |
| Write command to data-in delay                                       |              | tWTL   | 0   | -    | 0   | -    | 0   | -    | CLK  |      |
| Data-in to precharge command                                         |              | tDPL   | 1   | -    | 1   | -    | 1   | -    | CLK  |      |
| Data-in to active command                                            |              | tDAL   | 4   | -    | 3   | -    | 3   | -    | CLK  |      |
| DQM to data-in Hi-Z                                                  |              | tDQZ   | 2   | -    | 2   | -    | 2   | -    | CLK  |      |
| DQM to data mask                                                     |              | tDQM   | 0   | -    | 0   | -    | 0   | -    | CLK  |      |
| MRS to new command                                                   |              | tMRD   | 2   | -    | 2   | -    | 2   | -    | CLK  |      |
| Precharge to data output Hi-Z                                        |              | tPROZ  | 3   | -    | 3   | -    | 3   | -    | CLK  |      |
| Power down exit time                                                 |              | tPDE   | 1   | -    | 1   | -    | 1   | -    | CLK  |      |
| Self refresh exit time                                               |              | tSRE   | 1   | -    | 1   | -    | 1   | -    | CLK  | 3    |
| Refresh Time                                                         |              | tREF   | -   | 64   | -   | 64   | -   | 64   | ms   |      |

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Note :

1. VDD(min) is 3.15V when HY57V161610ET-7 operates at  $\overline{\text{CAS}}$  latency=2 and tCK2=8.9ns.

2. VDD(min) of HY57V161610ET-5/55 is 3.15V

3. A new command can be given tRRC after self refresh exit.

**DEVICE OPERATING OPTION TABLE**
**HY57V161610ET-5**

|               | $\overline{\text{CAS}}$ Latency | tRCD  | tRAS  | tRC    | tRP   | tAC   | tOH   |
|---------------|---------------------------------|-------|-------|--------|-------|-------|-------|
| <b>200MHz</b> | 3CLKs                           | 3CLKs | 8CLKs | 11CLKs | 3CLKs | 4.5ns | 1.5ns |
| <b>183MHz</b> | 3CLKs                           | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5ns   | 2ns   |
| <b>166MHz</b> | 3CLKs                           | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5.5ns | 2ns   |

**HY57V161610ET-55**

|               | CAS Latency | tRCD  | tRAS  | tRC    | tRP   | tAC   | tOH   |
|---------------|-------------|-------|-------|--------|-------|-------|-------|
| <b>183MHz</b> | 3CLKs       | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5ns   | 2ns   |
| <b>166MHz</b> | 3CLKs       | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5.5ns | 2ns   |
| <b>143MHz</b> | 3CLKs       | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5.5ns | 2.5ns |

**HY57V161610ET-6**

|               | CAS Latency | tRCD  | tRAS  | tRC    | tRP   | tAC   | tOH   |
|---------------|-------------|-------|-------|--------|-------|-------|-------|
| <b>166MHz</b> | 3CLKs       | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5.5ns | 2ns   |
| <b>143MHz</b> | 3CLKs       | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5.5ns | 2.5ns |
| <b>125MHz</b> | 3CLKs       | 2CLKs | 6CLKs | 9CLKs  | 3CLKs | 6ns   | 2.5ns |

**HY57V161610ET-7**

|               | CAS Latency | tRCD  | tRAS  | tRC    | tRP   | tAC   | tOH   |
|---------------|-------------|-------|-------|--------|-------|-------|-------|
| <b>143MHz</b> | 3CLKs       | 3CLKs | 7CLKs | 10CLKs | 3CLKs | 5.5ns | 2.5ns |
| <b>125MHz</b> | 3CLKs       | 3CLKs | 6CLKs | 9CLKs  | 3CLKs | 6ns   | 2.5ns |
| <b>100MHz</b> | 2CLKs       | 2CLKs | 5CLKs | 7CLKs  | 2CLKs | 7ns   | 2.5ns |

**HY57V161610ET-8**

|               | CAS Latency | tRCD  | tRAS  | tRC   | tRP   | tAC | tOH   |
|---------------|-------------|-------|-------|-------|-------|-----|-------|
| <b>125MHz</b> | 3CLKs       | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 2.5ns |
| <b>100MHz</b> | 3CLKs       | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 7ns | 2.5ns |
| <b>83MHz</b>  | 2CLKs       | 2CLKs | 4CLKs | 6CLKs | 2CLKs | 7ns | 2.5ns |

**HY57V161610ET-10**

|               | CAS Latency | tRCD  | tRAS  | tRC   | tRP   | tAC | tOH   |
|---------------|-------------|-------|-------|-------|-------|-----|-------|
| <b>100MHz</b> | 3CLKs       | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 7ns | 2.5ns |
| <b>83MHz</b>  | 2CLKs       | 2CLKs | 4CLKs | 6CLKs | 2CLKs | 7ns | 2.5ns |

**HY57V161610ET-15**

|              | CAS Latency | tRCD  | tRAS  | tRC   | tRP   | tAC  | tOH   |
|--------------|-------------|-------|-------|-------|-------|------|-------|
| <b>66MHz</b> | 1CLKs       | 2CLKs | 4CLKs | 6CLKs | 2CLKs | 14ns | 2.5ns |

**COMMAND TRUTH TABLE**

| Command                   |       | CKEn-1 | CKEn | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | DQM | A0~A9                               | A10/<br>AP | BA | Note |
|---------------------------|-------|--------|------|------------------------|-------------------------|-------------------------|------------------------|-----|-------------------------------------|------------|----|------|
| Mode Register Set         |       | H      | X    | L                      | L                       | L                       | L                      | X   | OP code                             |            |    |      |
| No Operation              |       | H      | X    | H                      | X                       | X                       | X                      | X   | X                                   |            |    |      |
|                           |       |        |      | L                      | H                       | H                       | H                      |     |                                     |            |    |      |
| Bank Active               |       | H      | X    | L                      | L                       | H                       | H                      | X   | Row Address                         |            | V  |      |
| Read                      |       | H      | X    | L                      | H                       | L                       | H                      | X   | Column<br>Address                   | L          | V  |      |
| Read with Auto precharge  |       |        |      |                        |                         |                         |                        |     |                                     | H          |    |      |
| Write                     |       | H      | X    | L                      | H                       | L                       | L                      | X   | Column<br>Address                   | L          | V  |      |
| Write with Auto precharge |       |        |      |                        |                         |                         |                        |     |                                     | H          |    |      |
| Precharge All Bank        |       | H      | X    | L                      | L                       | H                       | L                      | X   | X                                   | H          | X  |      |
| Precharge selected Bank   |       |        |      |                        |                         |                         |                        |     |                                     | L          | V  |      |
| Burst Stop                |       | H      | X    | L                      | H                       | H                       | L                      | X   | X                                   |            |    |      |
| U/LDQM                    |       | H      | X    |                        |                         |                         |                        | V   | X                                   |            |    |      |
| Auto Refresh              |       | H      | H    | L                      | L                       | L                       | H                      | X   | X                                   |            |    |      |
| Burst-READ-Single-WRITE   |       | H      | X    | L                      | L                       | L                       | L                      | X   | A9 Pin High<br>(Other Pins OP code) |            |    |      |
| Self Refresh <sup>1</sup> | Entry | H      | L    | L                      | L                       | L                       | H                      | X   | X                                   |            |    |      |
|                           | Exit  | L      | H    | H                      | X                       | X                       | X                      | X   |                                     |            |    |      |
| Precharge power<br>down   | Entry | H      | L    | H                      | X                       | X                       | X                      |     | X                                   | X          |    |      |
|                           |       |        |      | L                      | H                       | H                       | H                      |     |                                     |            |    |      |
|                           | Exit  | L      | H    | H                      | X                       | X                       | X                      | X   |                                     |            |    |      |
|                           |       |        |      | L                      | H                       | H                       | H                      |     |                                     |            |    |      |
| Clock Suspend             | Entry | H      | L    | H                      | X                       | X                       | X                      | X   | X                                   |            |    |      |
|                           |       |        |      | L                      | V                       | V                       | V                      |     |                                     |            |    |      |
|                           | Exit  | L      | H    | X                      |                         |                         |                        | X   |                                     |            |    |      |

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.

2. X=Do not care, L=Low, H=High, BA=Bank Address, RA= Row Address, CA=Column Address, Opcode=Operand Code, NOP=No Operation.

**PACKAGE INFORMATION**

400mil 50pin Thin Small Outline Package (TC)  
1Mx16 Synchronous DRAM

UNIT : mm(inch)

