

Document Title

512K x16 bit 3.0V Super Low Power Full CMOS slow SRAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
04	Initial Revision History Insert Revised - Reliability Spec Deleted	Jul.02.2000	Preliminary
05	Change AC Characteristics - tBLZ : 5/5/5 ---> 10/10/10	Oct.23.2000	Preliminary
06	Part Number is changed - HY62UF16803A --> HY62UF16804A	Nov.13.2000	Preliminary
07	Marking Instruction is inserted	Dec.5.2000	Preliminary
08	Test Condition Changed - I _{LO} / I _{SB} / I _{SB1} / V _{DR} / I _{CCDR} Marking Instruction Inserted	Dec.16.2000	Preliminary
09	Change Logo - Hyundai → Hynix	Apr.28.2001	
10	Change DC Parameter - I _{sb1} (LL) : 40uA → 25uA - I _{sb1} (Typ) : 8uA → 1uA - I _{cc} : 5mA → 4mA - I _{cc1} (1us) : 8mA → 4mA - I _{cc1} (Min) : 50mA → 40mA Change Data Retention - I _{ccDR} (LL) : 25uA → 15uA Change AC Parameter - tOE : 35ns → 25ns@55ns : 40ns → 35ns@70ns - tCW : 50ns → 45ns@55ns - tAW : 50ns → 45ns@55ns - tBW : 50ns → 45ns@55ns - tWP : 45ns → 40ns@55ns - tCHZ : 30ns → 20ns@55ns , 30ns → 25ns@70ns - tOHZ : 30ns → 20ns@55ns , 30ns → 25ns@70ns - tBHZ : 30ns → 20ns@55ns , 30ns → 25ns@70ns	Jan.28.2002	

DESCRIPTION

The HY62UF16804A is a high speed, super low power and 8Mbit full CMOS SRAM organized as 524,288 words by 16bits. The HY62UF16804A uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

FEATURES

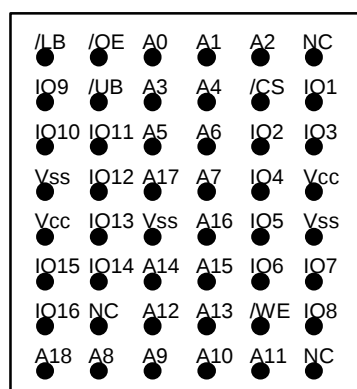
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL/SL-part)
 - 1.2V(min) data retention
- Standard pin configuration
 - 48-uBGA

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)		Temperature (°C)
				LL	SL	
HY62UF16804A-C	2.7~3.3	55/70/85	4	25	8	0~70
HY62UF16804A-I	2.7~3.3	55/70/85	4	25	8	-40~85

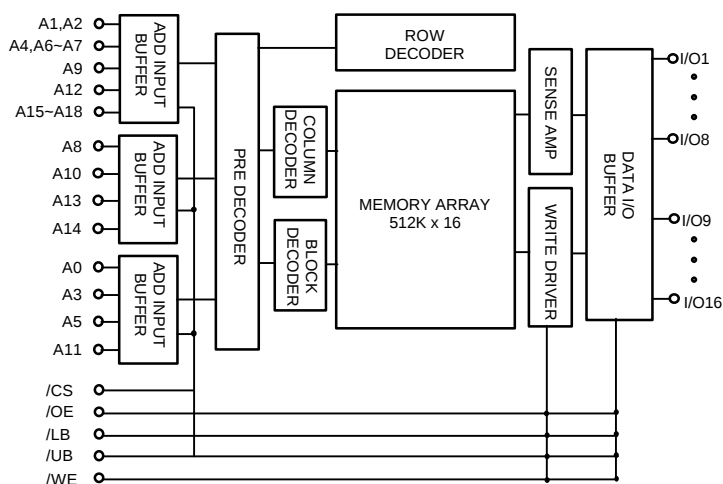
Note 1. C : Commercial, I : Industrial

2. Current value is max.

PIN CONNECTION (Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	I/O1~I/O16	Data Inputs / Outputs
/WE	Write Enable	A0~A18	Address Inputs
/OE	Output Enable	Vcc	Power(2.7V~3.3V)
/LB	Lower Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Package	Temp.
HY62UF16804A-DMC	55/70/85	LL-part	uBGA	C
HY62UF16804A-SMC	55/70/85	SL-part	uBGA	C
HY62UF16804A-DMI	55/70/85	LL-part	uBGA	I
HY62UF16804A-SMI	55/70/85	SL-part	uBGA	I

Note 1. C : Commercial, I : Industrial

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit	Remark
V _{IN} , V _{OUT}	Input/Output Voltage	-0.3 to V _{CC} +0.3V	V	
V _{CC}	Power Supply	-0.3 to 3.6	V	
T _A	Operating Temperature	0 to 70	°C	HY62UF16804A-C
		-40 to 85	°C	HY62UF16804A-I
T _{STG}	Storage Temperature	-55 to 150	°C	
P _D	Power Dissipation	1.0	W	
T _{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C • sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	Mode	I/O		Power
						I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	Deselected	High-Z	High-Z	Standby
X	X	X	H	H	Deselected	High-Z	High-Z	Standby
L	H	H	L	X	Output Disabled	High-Z	High-Z	Active
L	H	H	X	L	Output Disabled	High-Z	High-Z	Active
L	H	L	L	H	Read	DOUT	High-Z	Active
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Active
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

Note:

- H=V_{IH}, L=V_{IL}, X=don't care(V_{IH} or V_{IL})

- /UB, /LB(Upper, Lower Byte enable)

These active LOW inputs allow individual bytes to be written or read.

When /LB is LOW, data is written or read to the lower byte, I/O1 -I/O8.

When /UB is LOW, data is written or read to the upper byte, I/O9 -I/O16.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	2.7	3.0	3.3	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3(1)	-	0.6	V

Note : 1. V_{IL} = -1.5V for pulse width less than 30ns

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V~3.3V, T_A = 0°C to 70°C/ -40°C to 85°C

VCC = 2.7V 3.3V, 1A = 0 C to 70 C, 40 C to 85 C

Sym	Parameter	Test Condition		Min.	Typ.	Max.	Unit
ILI	Input Leakage Current	VSS ≤ VIN ≤ VCC		-1	-	1	uA
ILO	Output Leakage Current	VSS ≤ VOUT ≤ VCC, /CS = VIH or /OE = VIH or /WE = VIL, /UB = /LB = VIH		-1	-	1	uA
Icc	Operating Power Supply Current	/CS = VIL, VIN = VIH or VIL, Ii/O = 0mA		-	-	4	mA
Icc1	Average Operating Current	Cycle Time=Min,100% duty, Ii/O = 0mA, /CS = VIL,VIN = VIH or VIL		-	-	40	mA
		Cycle time = 1us, 100% duty, Ii/O = 0mA, /CS ≤ 0.2V, VIN<0.2V		-	-	4	mA
ISB	TTL Standby Current (TTL Input)	/CS = VIH or /UB=/LB= VIH, VIN = VIH or VIL		-	-	0.5	mA
ISB1	Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V or /UB=/LB ≥ Vcc-0.2V, VIN ≥ Vcc-0.2V or VIN ≤ Vss+0.2V	SL	-	-	8	uA
			LL	-	1	25	uA
VOL	Output Low Voltage	IoL = 2.1mA		-	-	0.4	V
VOH	Output High Voltage	IoH = -1.0mA		2.4	-	-	V

Note : Typical values are at V_{CC} = 3.0V, T_A = 25°C

CAPACITANCE

(Temp = 25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C _{IN}	Input Capacitance(Add, /CS, /LB, /UB /WE, /OE)	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance(I/O)	V _{I/O} = 0V	10	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

V_{CC} = 2.7V~3.3V, T_A = 0°C to 70°C/ -40°C to 85°C unless otherwise specified

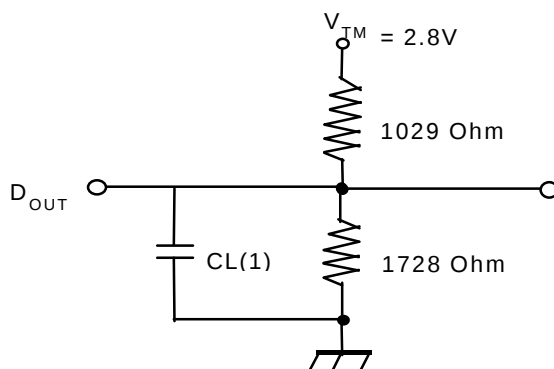
#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	tRC	Read Cycle Time	55	-	70	-	85	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	25	-	35	-	45	ns
5	tBA	/LB, /UB Access Time	-	55	-	70	-	85	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	10	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	20	0	25	0	30	ns
10	tOHZ	Out Disable to Output in High Z	0	20	0	25	0	30	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	20	0	25	0	30	ns
12	tOH	Output Hold from Address Change	10	-	10	-	10	-	ns
WRITE CYCLE									
13	tWC	Write Cycle Time	55	-	70	-	85	-	ns
14	tCW	Chip Selection to End of Write	45	-	60	-	70	-	ns
15	tAW	Address Valid to End of Write	45	-	60	-	70	-	ns
16	tBW	/LB, /UB Valid to End of Write	45	-	60	-	70	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	40	-	50	-	55	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	20	0	25	0	30	ns
21	tDW	Data to Write Time Overlap	25	-	30	-	35	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C / -40°C to 85°C, unless otherwise specified

PARAMETER		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	t _{CLZ} ,t _{OLZ} ,t _{BLZ} ,t _{CHZ} ,t _{OHZ} ,t _{BHZ} ,t _{WHZ} ,t _{OW}	CL = 5pF + 1TTL Load
	Other	CL = 30pF + 1TTL Load

AC TEST LOADS

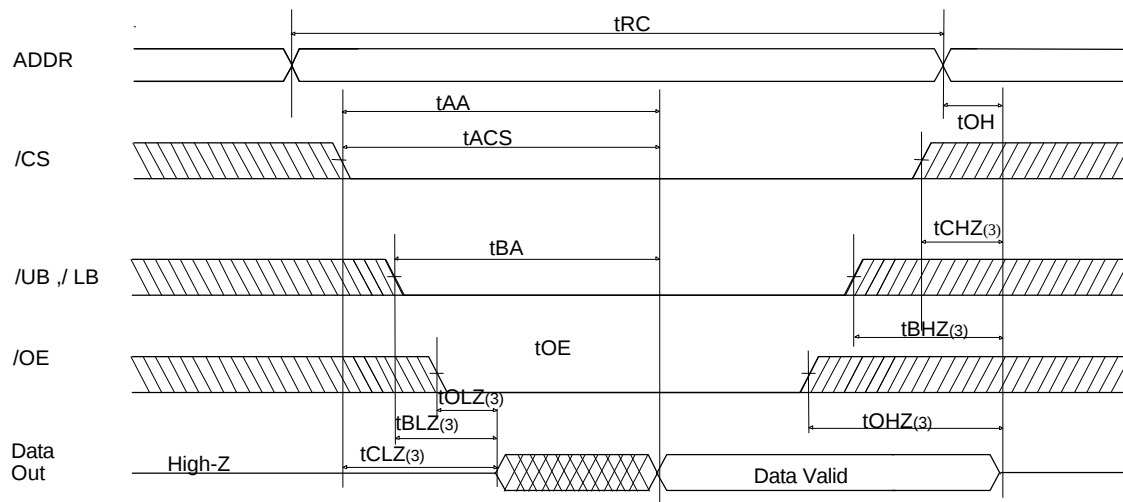


Note

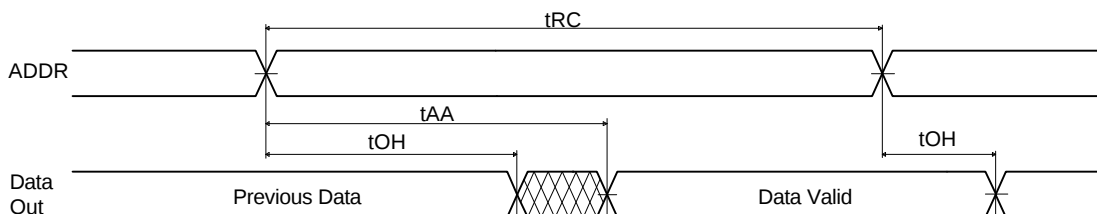
1. Including jig and scope capacitance

TIMING DIAGRAM

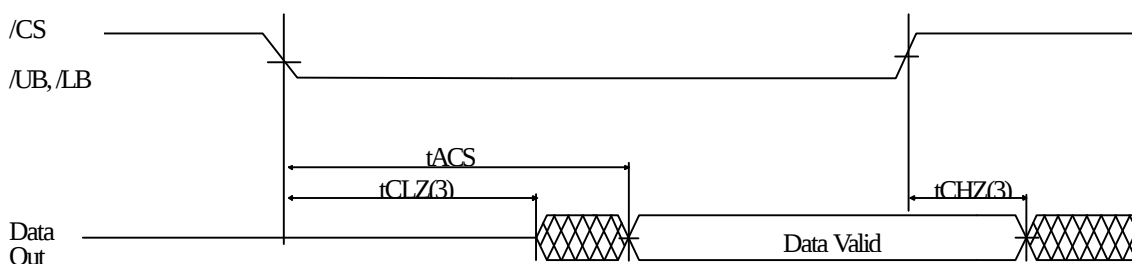
READ CYCLE 1(Note 1,4)



READ CYCLE 2(Note 1,2,4)



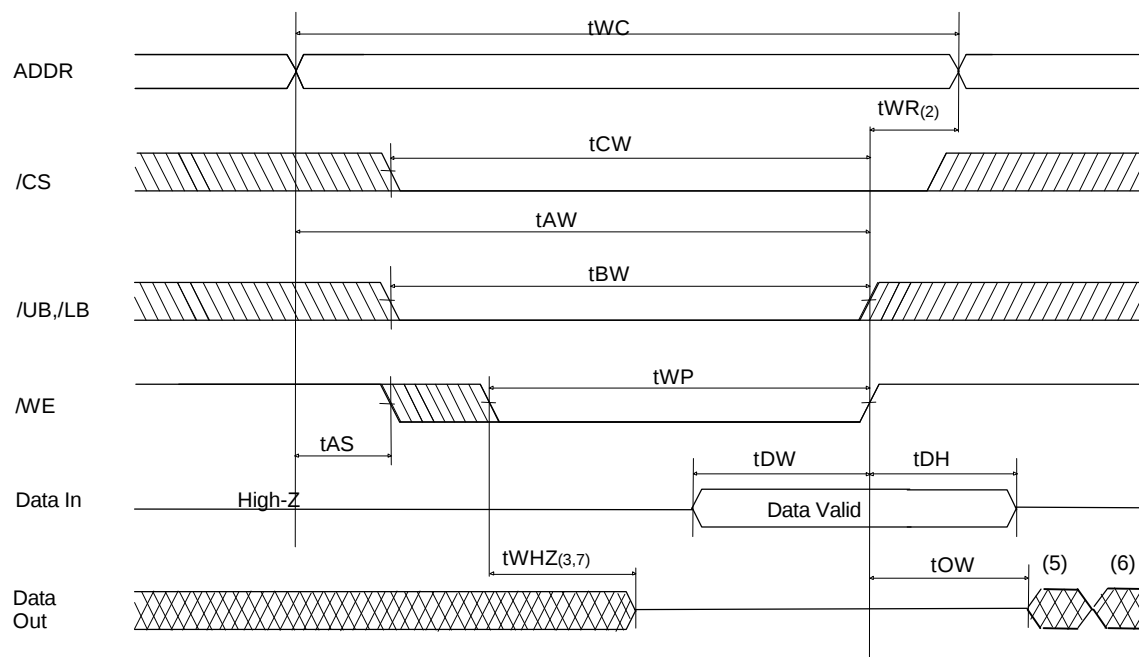
READ CYCLE 3(Note 1,2,4)



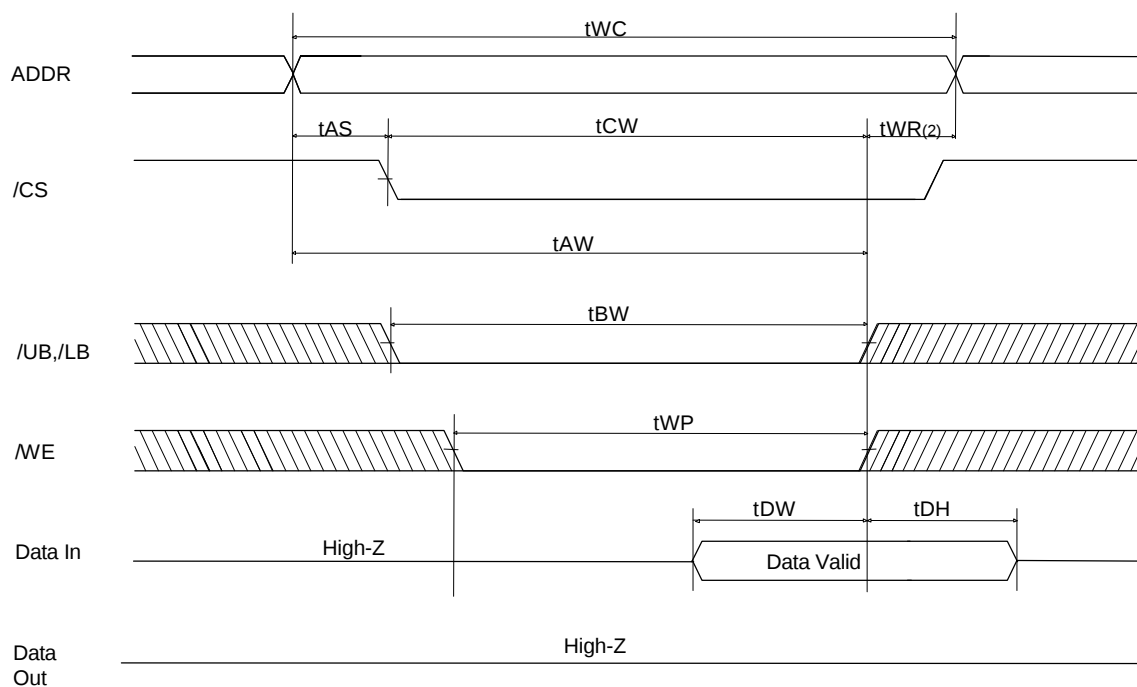
Notes:

1. A read occurs during the overlap of a low /OE, a high /WE, a low /CS1 and low /UB and /or /LB
2. /OE = V_{IL}
3. Transition is measured $\pm 200\text{mV}$ from steady state voltage.
This parameter is sampled and not 100% tested.
4. /CS in high for the standby, low for active
/UB and /LB in high for the standby, low for active

WRITE CYCLE 1 (1,4,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,8) (/CS Controlled)



Notes:

1. A write occurs during the overlap of a low /WE, a low /CS1 and low /UB and /or /LB.
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured +200mV from steady state.
This parameter is sampled and not 100% tested.
8. /CS in high for the standby, low for active
/UB and /LB in high for the standby, low for active

DATA RETENTION ELECTRIC CHARACTERISTIC

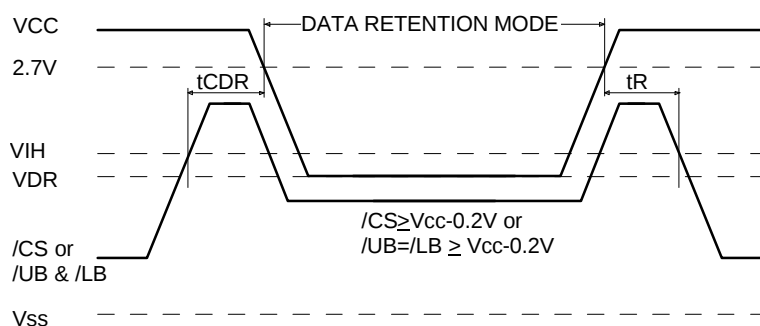
TA = 0°C to 70°C / -40°C to 85°C

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDR	Vcc for Data Retention	/CS ≥ Vcc - 0.2V or /UB=/LB ≥ Vcc-0.2V, VIN ≥ Vcc-0.2V or VIN ≤ Vss+0.2V	1.2	-	3.3	V
ICCDR	Data Retention Current	Vcc=1.5V, /CS ≥ Vcc - 0.2V or /UB=/LB ≥ Vcc-0.2V, VIN ≥ Vcc-0.2V or VIN ≤ Vss+0.2V	LL	-	15	uA
			SL	-	8	uA
TCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
TR	Operating Recovery Time		tRC(2)	-	-	ns

Notes:

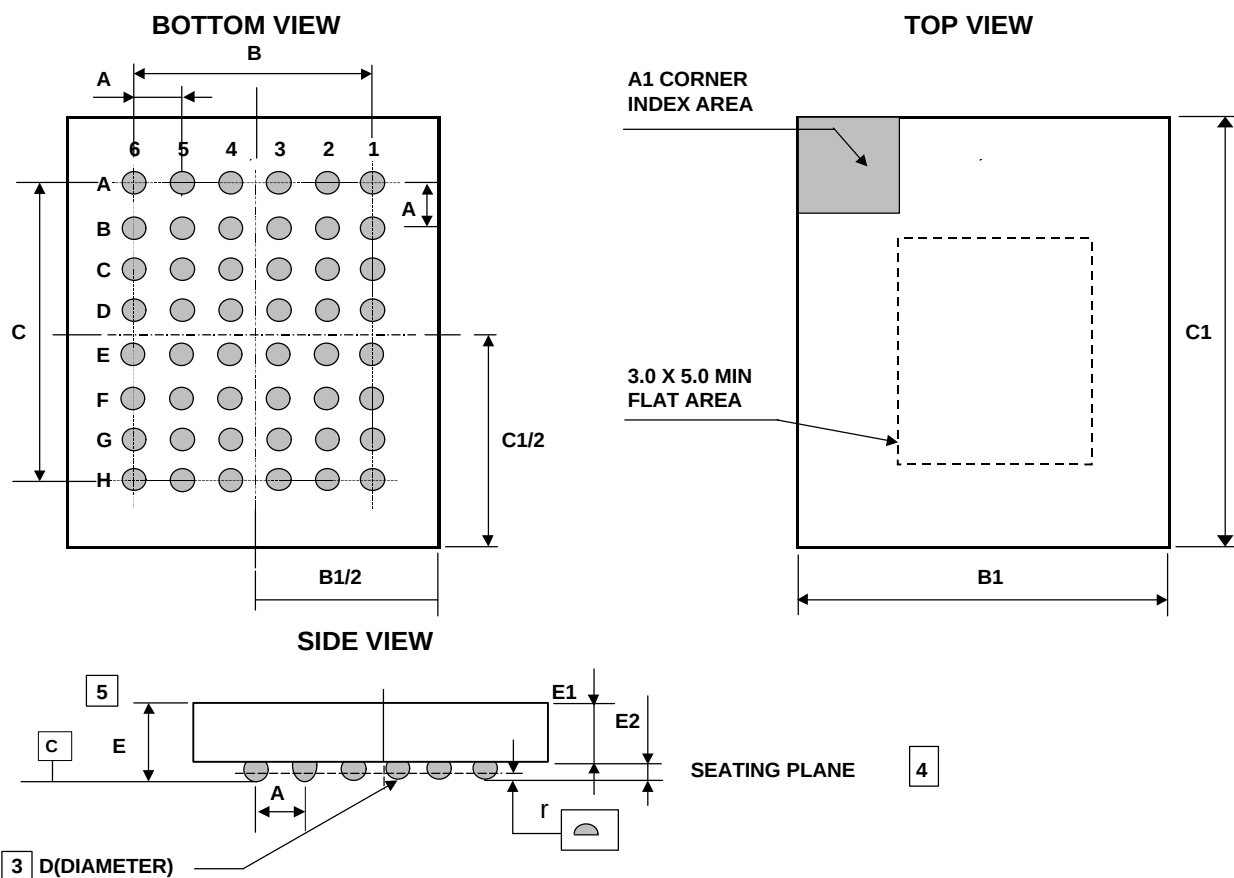
1. Typical values are under the condition of TA = 25°C .
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

48ball Micro Ball Grid Array Package(M)



Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	-	3.75	-
B1	-	7.4	-
C	-	5.25	-
C1	-	8.5	-
D	0.3	0.35	0.4
E	0.85	0.9	0.95
E1	0.6	0.65	0.7
E2	0.2	0.25	0.3
r	-	-	0.08

Note

1. DIMENSIONING AND TOLERANCING PER ASME Y14. 5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION "D" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. THIS IS A CONTROLLING DIMENSION.

MARKING INSTRUCTION

Package	Marking Example
uBGA	H Y U F 6 8 0 4 A c s s t y w w p x x x x x K O R ○

Index

- **HYUF6804A** : Part Name
- **c** : Power Consumption
 - D : Low Low Power
 - S : Super Low Power
- **ss** : Speed
 - 55 : 55ns
 - 70 : 70ns
 - 85 : 85ns
- **t** : Temperature
 - C : Commercial (-0 ~ 70 °C)
 - I : Industrial (-40 ~ 85 °C)
- **y** : Year (ex : 0 = year 2000, 1= year 2001)
- **ww** : Work Week (ex : 12 = work week 12)
- **p** : Process Code
- **xxxxx** : Lot No.
- **KOR** : Origin Country

Note

- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item