

Document Title**32K x8 bit 2.7~5.5V Low Power Slow SRAM**Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
00	Initial	Feb.05.2001	Preliminary
01	Revised - Change LL-Part Isb1 Limit @E.T/I.T, 4.5~5.5V : 15uA => 20uA	Feb.13.2001	Final
02	Revised - Marking Information Change : SOP Type - Voh Limit Change : 2.4V => 2.2V @2.7~3.6V	Feb.21.2001	Final
03	Changed Logo - HYUNDAI -> hynix - Marking Information Change	Apr.30.2001	Final
04	Revised - Iccdr Limit Add : 2uA @40°C	May.23.2001	Final

DESCRIPTION

The HY62WT08081E is a high-speed, low power and 32,786 X 8-bits CMOS Static Random Access Memory fabricated using Hynix's high performance CMOS process technology. It is suitable for use in low voltage operation and battery back-up application. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt.

FEATURES

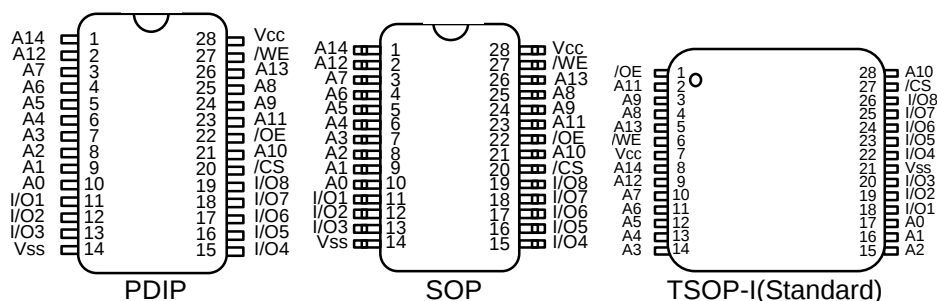
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(LL-part)
 - 2.0V(min.) data retention
- Standard pin configuration
 - 28 pin 600mil PDIP
 - 28 pin 330mil SOP
 - 28 pin 8x13.4 mm TSOP-I (Standard)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA) LL-part	Temperature (°C)
HY62WT08081E-C	4.5~5.5	55/70	10	10	0~70(Normal)
	2.7~3.6	70*/85	2	5	
HY62WT08081E-E	4.5~5.5	55/70	10	20	-25~85(Extended)
	2.7~3.6	70*/85	2	8	
HY62WT08081E-I	4.5~5.5	55/70	10	20	-40~85(Industrial)
	2.7~3.6	70*/85	2	8	

Note 1. Current value is max.

* 70ns is available with 30pF test load

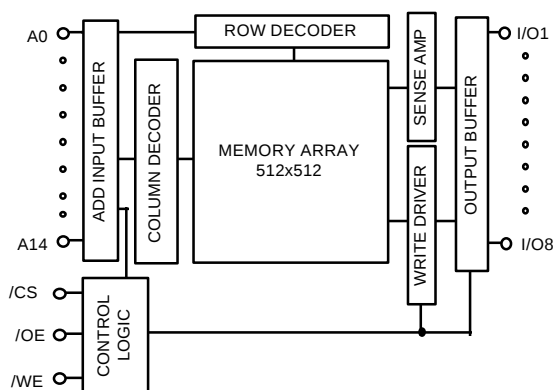
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed		Power	Temp	Package
	4.5~5.5V	2.7~3.6V			
HY62WT08081E-DPC	55/70	70*/85	LL-part	0 to 70°C	PDIP
HY62WT08081E-DPE				-25 to 85°C	
HY62WT08081E-DPI				-40 to 85°C	
HY62WT08081E-DGC				0 to 70°C	SOP
HY62WT08081E-DGE				-25 to 85°C	
HY62WT08081E-DGI				-40 to 85°C	
HY62WT08081E-DTC				0 to 70°C	TSOP-I Standard
HY62WT08081E-DTE				-25 to 85°C	
HY62WT08081E-DTI				-40 to 85°C	

Note * 70ns is available with 30pF test load

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter		Rating	Unit
V _{CC} , V _{IN} , V _{OUT}	Power Supply, Input/Output Voltage	4.5~5.5V	-0.3 to 7.0	V
		2.7~3.6V	-0.3 to 4.6	V
T _A	Operating Temperature	HY62WT08081E-C	0 to 70	°C
		HY62WT08081E-E	-25 to 85	°C
		HY62WT08081E-I	-40 to 85	°C
T _{STG}	Storage Temperature		-65 to 150	°C
P _D	Power Dissipation		1.0	W
I _{OUT}	Data Output Current		50	mA
T _{SOLDER}	Lead Soldering Temperature & Time		260 •10	°C•sec

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONSV_{CC} = 4.5~5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3(1)	-	0.8	V

Note1. V_{IL} = -3.0V for pulse width less than 50nsV_{CC} = 2.7~3.6V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Power Supply Voltage	2.7	3.0/3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3(1)	-	0.6	V

Note1. V_{IL} = -1.5V for pulse width less than 50ns**TRUTH TABLE**

/CS	/WE	/OE	Mode	I/O Operation
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note

1. H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

V_{CC} = 4.5 ~ 5.5V, T_A = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) / -40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}		-1	-	1	uA
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS = V _{IH} or /OE = V _{IH} or /WE = V _{IL}		-1	-	1	uA
I _{CC}	Operating Power Supply Current	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA		-	-	10	mA
I _{CC1}	Average Operating Current	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , Min. Duty Cycle = 100%, I _{I/O} = 0mA		-	-	50	mA
I _{SB}	TTL Standby Current (TTL Inputs)	/CS= V _{IH} , V _{IN} = V _{IH} or V _{IL}		-	-	1	mA
I _{SB1}	CMOS Standby Current (CMOS Inputs)	/CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V	0~ 70°C	-	-	10	uA
			-25~ 85°C or -40~ 85°C	-	-	20	uA
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -1.0mA		2.4	-	-	V

Note : Typical values are at V_{CC} = 5.0V, T_A = 25°C

V_{CC} = 2.7~3.6V, T_A = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) / -40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}		-1	-	1	uA
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS = V _{IH} or /OE = V _{IH} or /WE = V _{IL}		-1	-	1	uA
I _{CC}	Operating Power Supply Current	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA		-	-	2	mA
I _{CC1}	Average Operating Current	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , Min. Duty Cycle = 100%, I _{I/O} = 0mA		-	-	30	mA
I _{SB}	TTL Standby Current (TTL Inputs)	/CS= V _{IH} , V _{IN} = V _{IH} or V _{IL}		-	-	0.3	mA
I _{SB1}	CMOS Standby Current (CMOS Inputs)	/CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V	0~ 70°C	-	-	5	uA
			-25~ 85°C or -40~ 85°C	-	-	8	uA
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -1.0mA		2.2	-	-	V

Note : Typical values are at V_{CC} = 3.0/3.3V, T_A = 25°C

AC CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) / -40°C to 85°C (Industrial)
unless otherwise specified.

#	Symbol	Parameter	-55		-70		Unit
			Min.	Max.	Min.	Max.	
READ CYCLE							
1	tRC	Read Cycle Time	55	-	70	-	ns
2	tAA	Address Access Time	-	55	-	70	ns
3	tACS	Chip Select Access Time	-	55	-	70	ns
4	tOE	Output Enable to Output Valid	-	25	-	35	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	ns
7	tCHZ	Chip Disable to Output in High Z	0	20	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	30	ns
9	tOH	Output Hold from Address Change	5	-	5	-	ns
WRITE CYCLE							
10	tWC	Write Cycle Time	55	-	70	-	ns
11	tCW	Chip Selection to End of Write	45	-	60	-	ns
12	tAW	Address Valid to End of Write	45	-	60	-	ns
13	tAS	Address Set-up Time	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	50	-	ns
15	tWR	Write Recovery Time	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	25	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	ns

V_{CC} = 2.7~3.6V, T_A = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) / -40°C to 85°C (Industrial)
unless otherwise specified.

#	Symbol	Parameter	-70*		-85		Unit
			Min.	Max.	Min	Max.	
READ CYCLE							
1	tRC	Read Cycle Time	70	-	85	-	ns
2	tAA	Address Access Time	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	35	-	45	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	ns
7	tCHZ	Chip Disable to Output in High Z	0	30	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	30	ns
9	tOH	Output Hold from Address Change	5	-	5	-	ns
WRITE CYCLE							
10	tWC	Write Cycle Time	70	-	85	-	ns
11	tCW	Chip Selection to End of Write	60	-	75	-	ns
12	tAW	Address Valid to End of Write	60	-	75	-	ns
13	tAS	Address Set-up Time	0	-	0	-	ns
14	tWP	Write Pulse Width	50	-	60	-	ns
15	tWR	Write Recovery Time	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	25	0	30	ns
17	tDW	Data to Write Time Overlap	30	-	40	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	ns

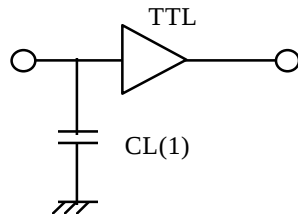
Note * 70ns is available with 30pF test load

AC TEST CONDITIONS

$T_A = 0^{\circ}\text{C}$ to 70°C (Normal) / -25°C to 85°C (Extended) / -40°C to 85°C (Industrial)
unless otherwise specified.

Parameter		Value
Input Pulse Level	$V_{CC} = 4.5\sim 5.5\text{V}$	0.8V to 2.4V
	$V_{CC} = 2.7\sim 3.6\text{V}$	0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	$t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW}$	$CL = 5\text{pF} + 1\text{TTL Load}$
	Others	$CL = 100\text{pF} + 1\text{TTL Load}$
		$CL^* = 30\text{pF} + 1\text{TTL Load}$

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

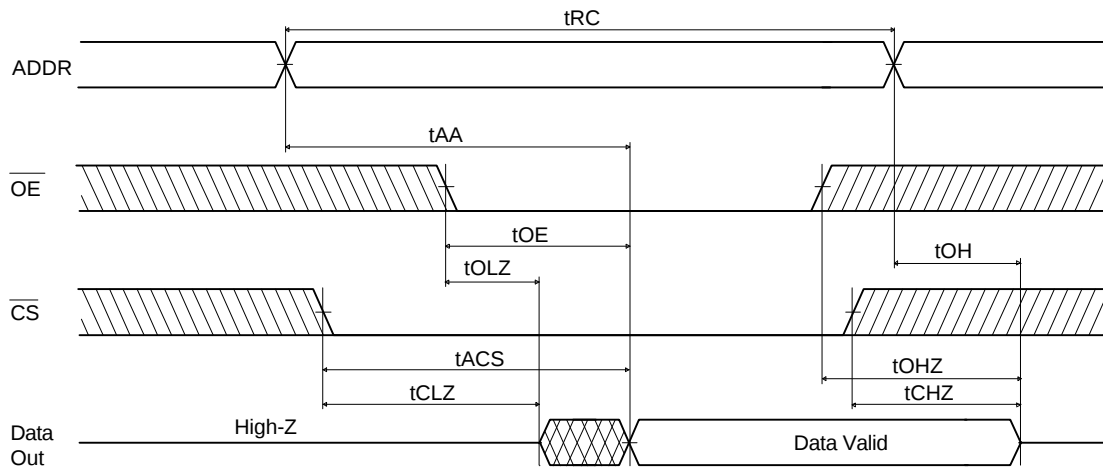
$T_A = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O} = 0\text{V}$	8	pF

Note : These parameters are sampled and not 100% tested

TIMING DIAGRAM

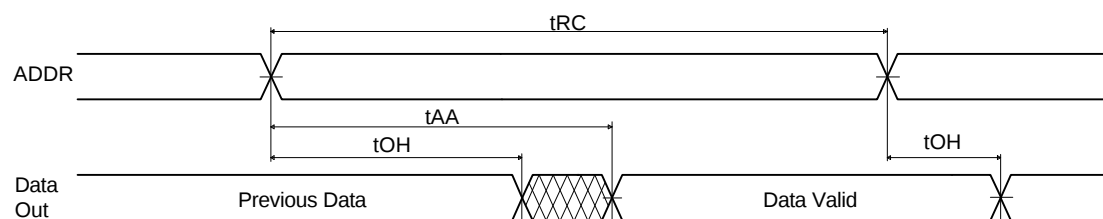
READ CYCLE 1



Note(READ CYCLE):

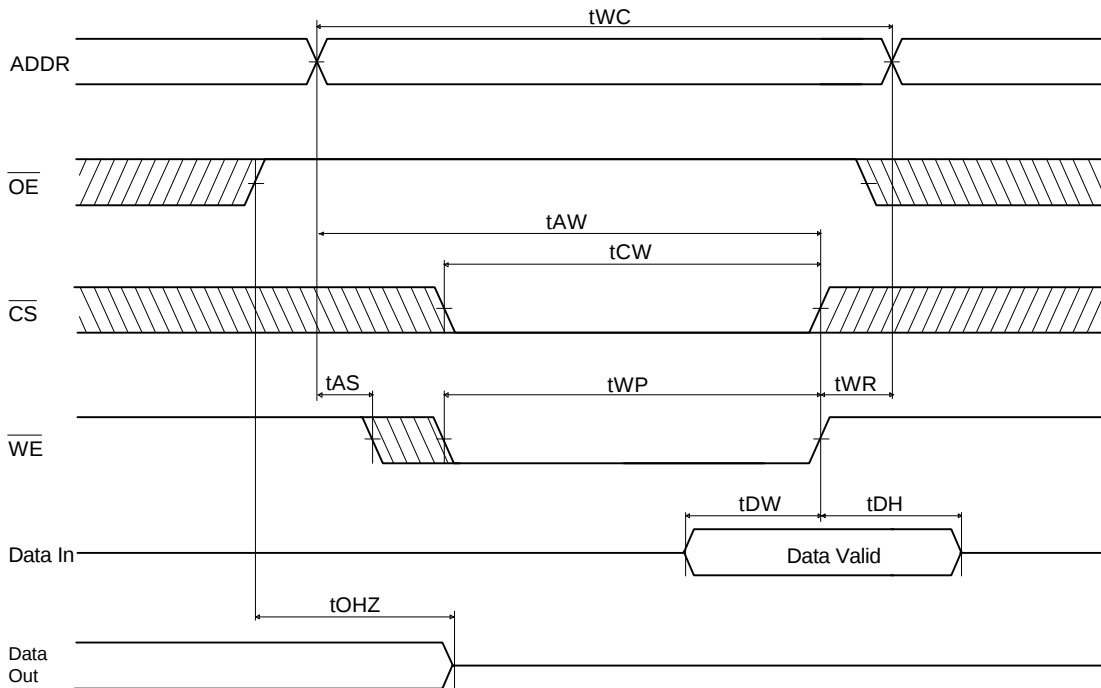
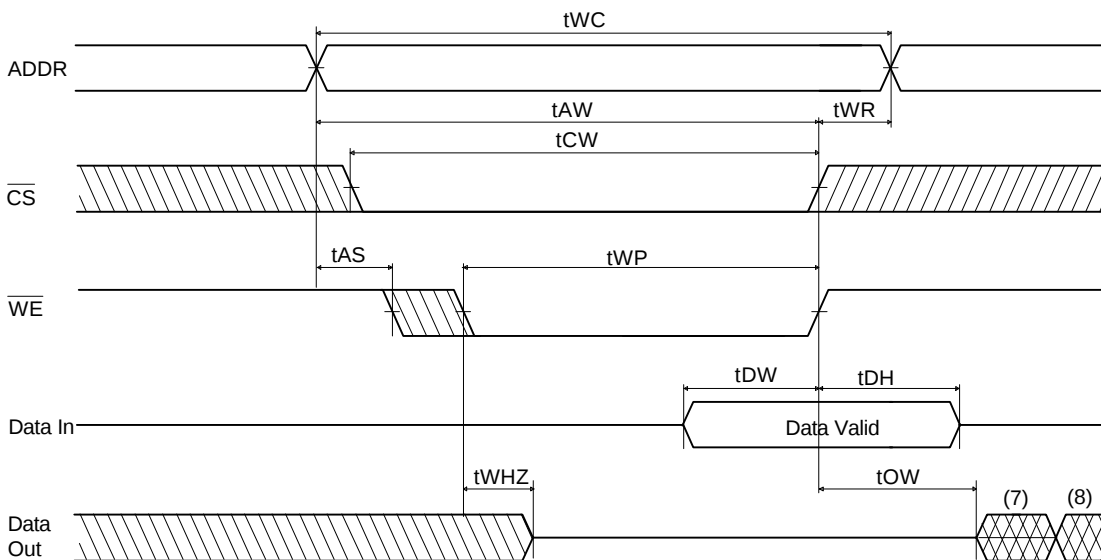
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for the read cycle.

READ CYCLE 2



Note(READ CYCLE):

1. $\overline{WE}$ is high for the read cycle.
2. Device is continuously selected $\overline{CS} = V_{IL}$.
3. $\overline{OE} = V_{IL}$.

WRITE CYCLE 1 (/OE Clocked)

WRITE CYCLE 2 (/OE Low Fixed)


Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{cw} is measured from the later of /CS going low to the end of write .
3. t_{as} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of the latest written data in this write cycle.
8. DOUT is the read data of the new address.

DATA RETENTION CHARACTERISTIC

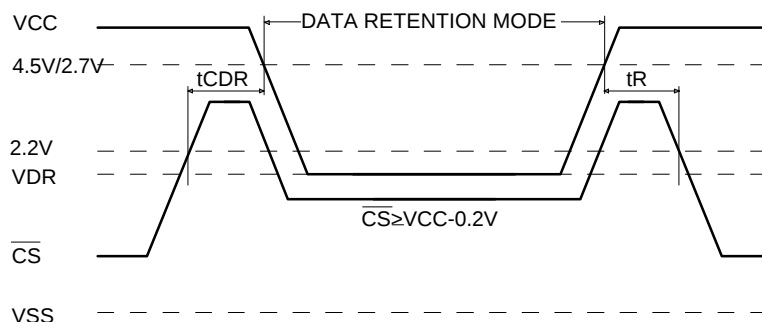
T_A = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) / -40°C to 85°C (Industrial)
unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ ⁽¹⁾	Max	Unit
VDR	V _{CC} for Data Retention	$CS \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$	2.0	-	-	V
I _{CCDR} (3)	Data Retention Current	$V_{CC} = 3.0V$, $/CS \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$	0~ 70°C	0.5	5	uA
			-25~ 85°C or -40~ 85°C	0.5	8	uA
t _{CDR}	Chip Deselect to Data Retention Time	See Data Retention	0	-	-	ns
t _R	Operating Recovery Time	Timing Diagram	t _{RC} (2)	-	-	ns

Notes

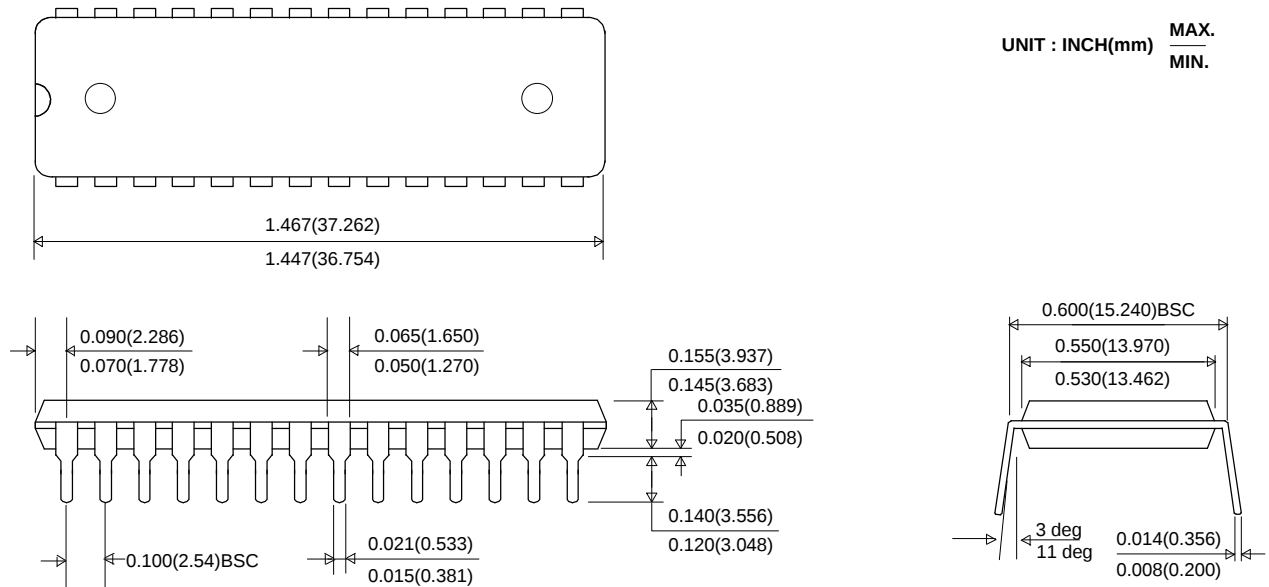
1. Typical values are under the condition of T_A = 25°C.
2. t_{RC} is read cycle time.
3. I_{ccdr} : 2uA at T_a < 40°C

DATA RETENTION TIMING DIAGRAM

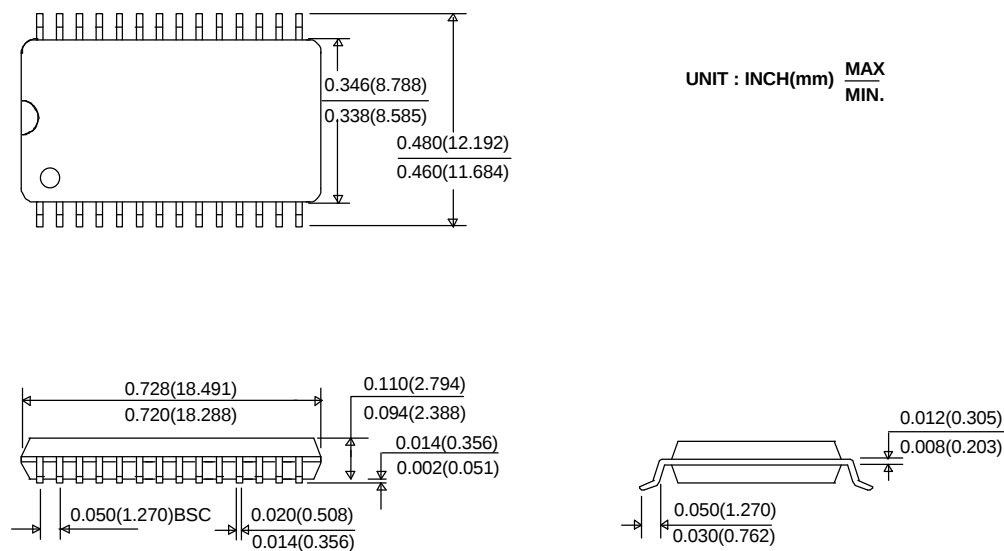


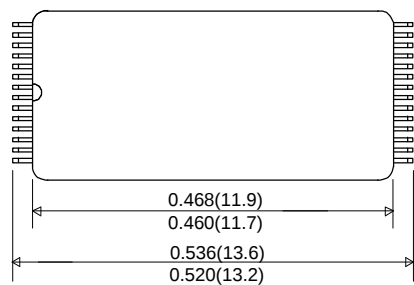
PACKAGE INFORMATION

28pin 600mil Dual In-Line Package(Blank)

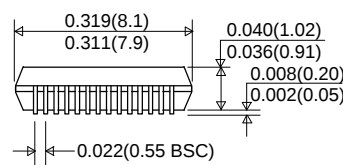
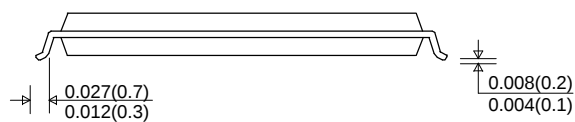


28pin 330mil Small Outline Package(FW)



28pin 8x13.4mm Thin Small Outline Package Standard(T)


UNIT : INCH(mm) $\frac{\text{MAX.}}{\text{MIN.}}$



Package	Marking Example
PDIP	Diagram showing the marking layout for a PDIP package. The marking is arranged in three rows of characters within a rectangular area. The first row contains 'h y n i x' followed by two empty boxes, then 'y y w w p'. The second row contains 'H Y 6 2 W T 0 8 1 E c s s t'. The third row contains 'K O R E A' followed by eight empty boxes. There are two circles on the left side of the marking area, one above and one below the first row.
SOP	Diagram showing the marking layout for a SOP package. The marking is arranged in three rows of characters within a rectangular area. The first row contains 'h y n i x' followed by two empty boxes, then 'y y w w p'. The second row contains 'H Y 6 2 W T 0 8 1 E c s s t'. The third row contains 'K O R E A' followed by eight empty boxes. There are two circles on the left side of the marking area, one above and one below the first row.
TSOP-I	Diagram showing the marking layout for a TSOP-I package. The marking is arranged in three rows of characters within a rectangular area. The first row contains 'h y n i x' followed by two empty boxes, then 'y y w w p'. The second row contains 'H Y 6 2 W T 0 8 1 E c s s t'. The third row contains 'K O R E A' followed by eight empty boxes. There are two circles on the left side of the marking area, one above and one below the first row.

• hynix	: hynix Logo	
• KOREA	: Origin Country	
• HY62WT081E	: Part Name	
	- HY62WT081E	: 2.7~5.5V
• yy	: Year (ex : 00 = year 2000, 01 = year 2001)	
• ww	: Work Week (ex : 12 = ww12)	
• p	: Process Code	
• c	: Power Consumption	
	- L	: Low Power
	- D	: Low Low Power
• ss	: Speed	
	- 55	: 55ns @ 4.5~5.5V 70ns @ 2.7~3.6V
	- 70	: 70ns @ 4.5~5.5V 85ns @ 2.7~3.6V
• t	: Temperature	
	- C	: Commercial (0 ~ 70 °C)
	- E	: Extended (-25 ~ 85 °C)
	- I	: Industrial (-40 ~ 85 °C)
• xxxxxxxx	: Lot Number	

- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item (Except hynix)