



GENERAL DESCRIPTION



The ICS87973I-147 is a LVC MOS/LV TTL clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87973I-147 has three selectable inputs and provides 14 LVC MOS/LV TTL outputs.

The ICS87973I-147 is a highly flexible device. The three selectable inputs (1 differential and 2 single ended inputs) are often used in systems requiring redundant clock sources. Up to three different output frequencies can be generated among the three output banks.

The three output banks and feedback output each have their own output dividers which allows the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. In addition, 2 outputs in Bank C (QC2, QC3) can be selected to be inverting or non-inverting. The output frequency range is 10MHz to 150MHz. The input frequency range is 6MHz to 120MHz.

The ICS87973I-147 also has a QSYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period prior to coincident rising edges of Bank A and Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

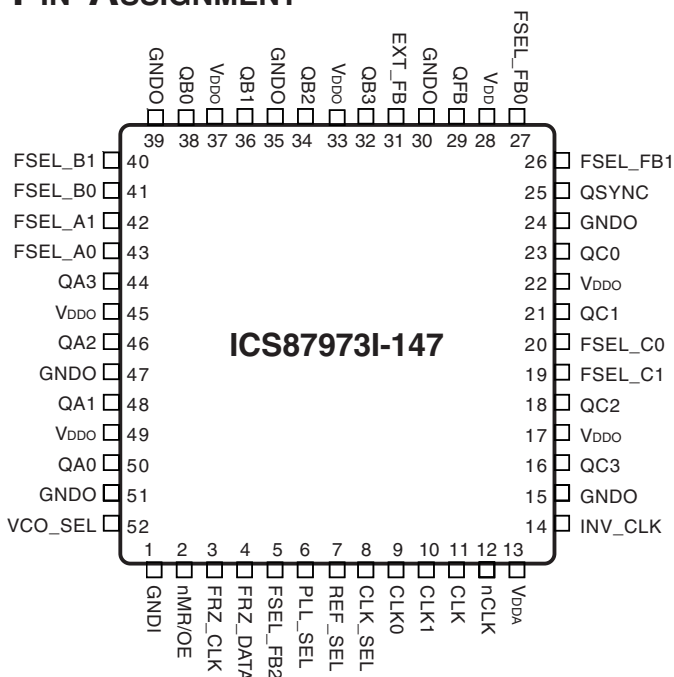
Example Applications:

1. *System Clock generator:* Use a 16.66MHz reference clock to generate eight 33.33MHz copies for PCI and four 100MHz copies for the CPU or PCI-X.
2. *Line Card Multiplier:* Multiply differential 62.5MHz from a back plane to single-ended 125MHz for the line Card ASICs and Gigabit Ethernet Serdes.
3. *Zero Delay buffer for Synchronous memory:* Fan out up to twelve 100MHz copies from a memory controller reference clock to the memory chips on a memory module with zero delay.

FEATURES

- Fully integrated PLL
- 14 LVC MOS/LV TTL outputs; (12) clock, (1) feedback, (1) sync
- Selectable LVC MOS/LV TTL or differential CLK, nCLK inputs
- CLK0, CLK1 can accept the following input levels: LVC MOS or LV TTL
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 10MHz to 150MHz
- VCO range: 240MHz to 500MHz
- Output skew: 200ps (maximum)
- Cycle-to-cycle jitter, (all banks ÷ 4): 55ps (maximum)
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Pin compatible with MPC973
- Compatible with PowerPC™ and Pentium™ Microprocessors

PIN ASSIGNMENT



52-Lead LQFP

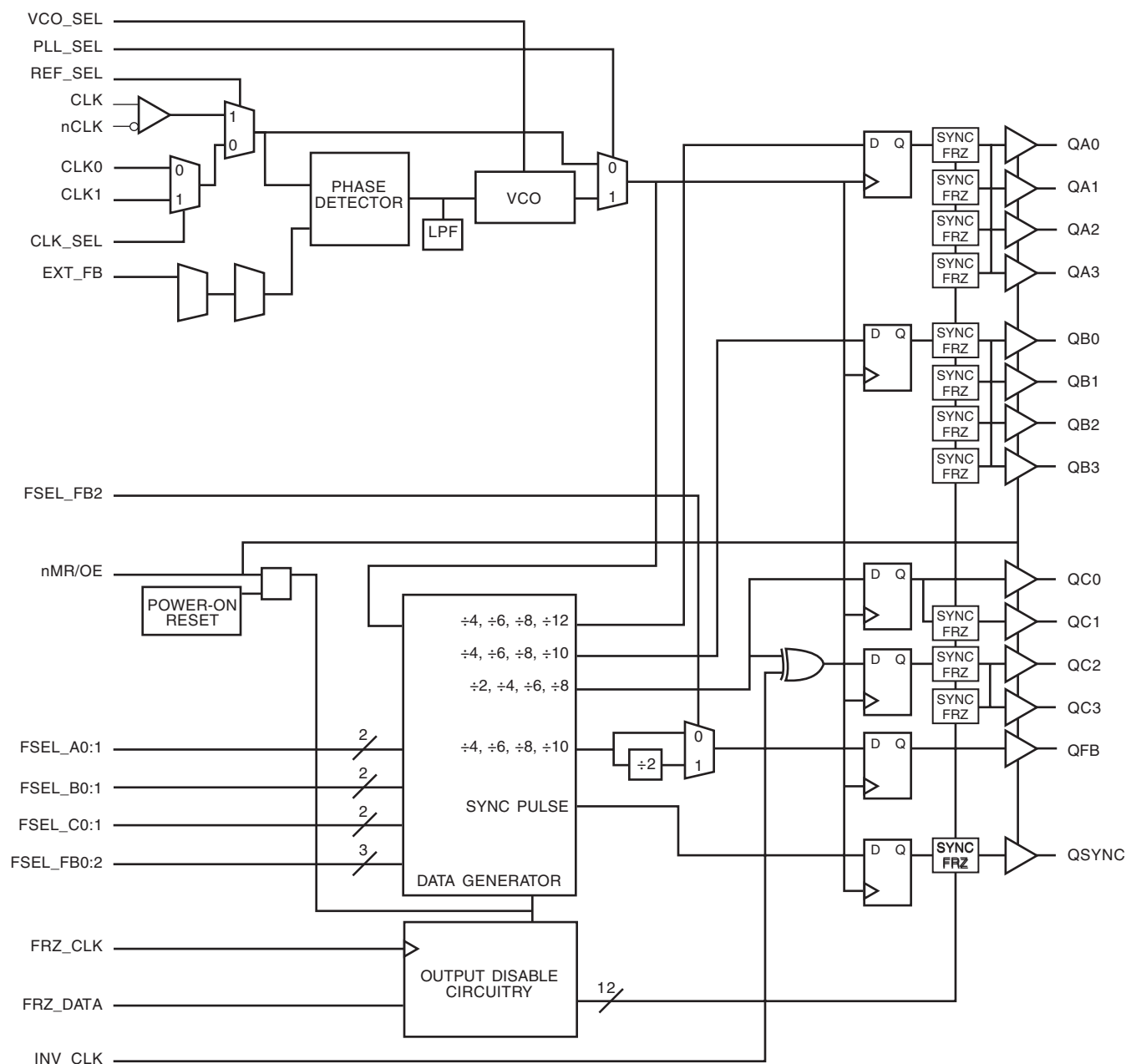
10mm x 10mm x 1.4mm package body

Y package

Top View



BLOCK DIAGRAM





SIMPLIFIED BLOCK DIAGRAM

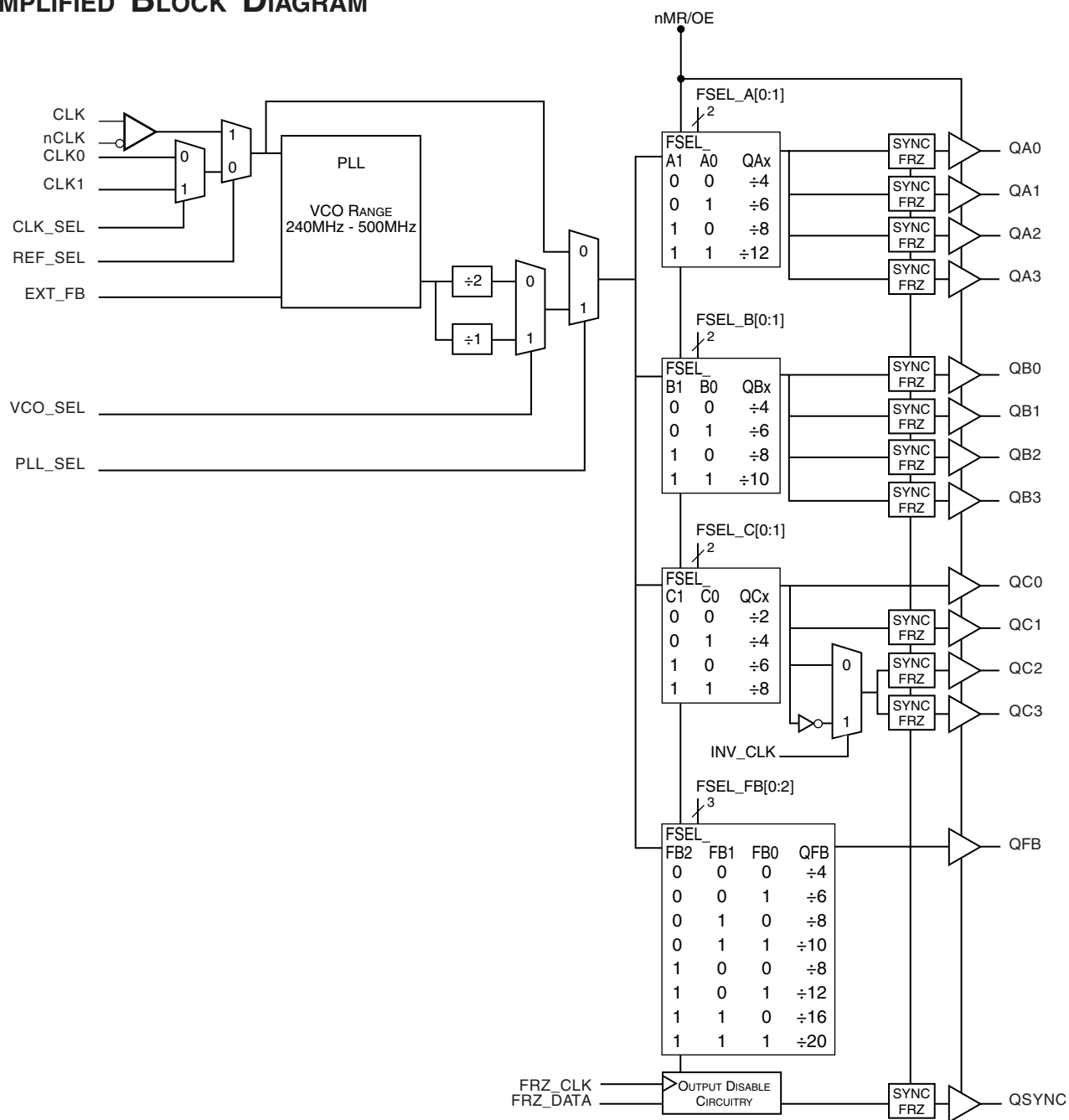




TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	GNDI	Power		Power supply ground.
2	nMR/OE	Input	Pullup	Master reset and output enable. When HIGH, enables the outputs. When LOW, resets the outputs to tristate and resets output divide circuitry. Enables and disables all outputs. LVC MOS / LV TTL interface levels.
3	FRZ_CLK	Input	Pullup	Clock input for freeze circuitry. LVC MOS / LV TTL interface levels.
4	FRZ_DATA	Input	Pullup	Configuration data input for freeze circuitry. LVC MOS / LV TTL interface levels.
5, 26, 27	FSEL_FB2, FSEL_FB1, FSEL_FB0	Input	Pullup	Select pins control Feedback Divide value. LVC MOS / LV TTL interface levels.
6	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL. LVC MOS / LV TTL interface levels.
7	REF_SEL	Input	Pullup	Selects between CLK0 or CLK1 and CLK, nCLK inputs. When HIGH, selects CLK, nCLK. When LOW, selects CLK0 or CLK1. LVC MOS / LV TTL interface levels.
8	CLK_SEL	Input	Pullup	Clock select input. Selects between CLK0 and CLK1 as phase detector reference. When LOW, selects CLK0. When HIGH, selects CLK1. LVC MOS / LV TTL interface levels.
9, 10	CLK0, CLK1	Input	Pullup	Reference clock inputs. LVC MOS / LV TTL interface levels.
11	CLK	Input	Pullup	Non-inverting differential clock input.
12	nCLK	Input		Inverting differential clock input. $V_{DD}/2$ default when left floating.
13	V_{DDA}	Power		Analog supply pin.
14	INV_CLK	Input	Pullup	Inverted clock select for QC2 and QC3 outputs. LVC MOS / LV TTL interface levels.
15, 24, 30, 35, 39, 47, 51	GNDO	Power		Power supply ground.
16, 18, 21, 23	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVC MOS / LV TTL interface levels.
17, 22, 33, 37, 45, 49	V_{DDO}	Power		Output supply pins.
19, 20	FSEL_C1, FSEL_C0	Input	Pullup	Select pins for Bank C outputs. LVC MOS / LV TTL interface levels.
25	QSYNC	Output		Synchronization output for Bank A and Bank C. Refer to Figure 1, Timing Diagrams. LVC MOS / LV TTL interface levels.
28	V_{DD}	Power		Core supply pins.
29	QFB	Output		Feedback clock output. LVC MOS / LV TTL interface levels.
31	EXT_FB	Input	Pullup	Extended feedback. LVC MOS / LV TTL interface levels.
32, 34, 36, 38	QB3, QB2, QB1, QB0	Output		Bank B clock outputs. 7Ω typical output impedance. LVC MOS / LV TTL interface levels.
40, 41	FSEL_B1, FSEL_B0	Input	Pullup	Select pins for Bank B outputs. LVC MOS / LV TTL interface levels.
42, 43	FSEL_A1, FSEL_A0	Input	Pullup	Select pins for Bank A outputs. LVC MOS / LV TTL interface levels.
44, 46, 48, 50	QA3, QA2, QA1, QA0	Output		Bank A clock outputs. 7Ω typical output impedance. LVC MOS / LV TTL interface levels.
52	VCO_SEL	Input	Pullup	Selects VCO. When HIGH, selects $VCO \div 1$. When LOW, selects $VCO \div 2$. LVC MOS / LV TTL interface levels.

NOTE: Pullup refer to internal input resistors. See table 2, Pin Characteristics, for typical values.



TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP} , $R_{PULLDOWN}$	Input Pullup/Pulldown Resistor			51		K Ω
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} , V_{DDA} , $V_{DDO} = 3.465V$			18	pF
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs	Inputs		Outputs	Inputs		Outputs
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	$\div 4$	0	0	$\div 4$	0	0	$\div 2$
0	1	$\div 6$	0	1	$\div 6$	0	1	$\div 4$
1	0	$\div 8$	1	0	$\div 8$	1	0	$\div 6$
1	1	$\div 12$	1	1	$\div 10$	1	1	$\div 8$

TABLE 3B. FEEDBACK CONFIGURATION SELECT FUNCTION TABLE

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	$\div 4$
0	0	1	$\div 6$
0	1	0	$\div 8$
0	1	1	$\div 10$
1	0	0	$\div 8$
1	0	1	$\div 12$
1	1	0	$\div 16$
1	1	1	$\div 20$

TABLE 3C. CONTROL INPUT SELECT FUNCTION TABLE

Control Pin	Logic 0	Logic 1
VCO_SEL	VCO/2	VCO
REF_SEL	CLK0 or CLK1	CLK, nCLK
CLK_SEL	CLK0	CLK1
PLL_SEL	BYPASS PLL	Enable PLL
nMR/OE	Master Reset/Output Hi Z	Enable Outputs
INV_CLK	Non-Inverted QC2, QC3	Inverted QC2, QC3

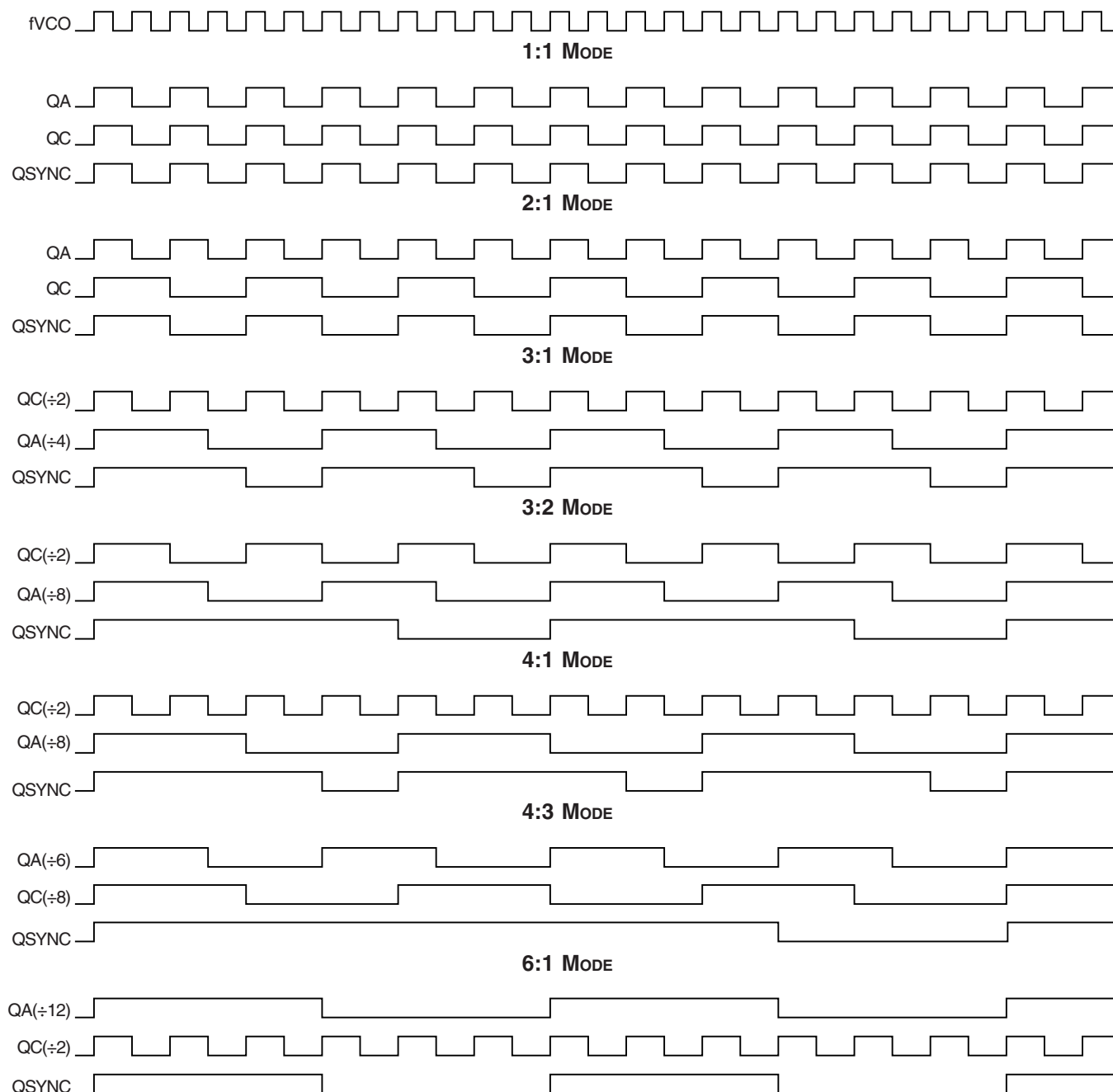


FIGURE 1. TIMING DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		2.935	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				225	mA
I_{DDA}	Analog Supply Current				20	mA

NOTE: Special thermal handling may be required in some configurations.

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVC MOS Inputs	2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	LVC MOS Inputs	-0.3		0.8	V
I_{IN}	Input Current				± 120	μA
V_{OH}	Output High Voltage	$I_{OH} = -20\text{mA}$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 20\text{mA}$			0.5	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1, 2	CLK, nCLK	0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	CLK, nCLK	$V_{DD} - 2V$		$V_{DD} - 0.6V$	V

NOTE 1: Common mode voltage is defined as V_{IH} of the differential signal.

NOTE 2: For single ended applications, the maximum input voltage for CLK and nCLK is $V_{DD} + 0.3V$.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK0, CLK1, CLK, nCLK; NOTE 1			120	MHz
		FRZ_CLK			20	MHz

NOTE 1: Input frequency depends on the feedback divide ratio to ensure "clock * Feedback Divide" is in the VCO range of 240MHz to 500MHz.



TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		$\div 2$			150	MHz
			$\div 4$			125	MHz
			$\div 6$			83.33	MHz
			$\div 8$			62.5	MHz
$t(\phi)$	Static Phase Offset; NOTE 1	CLK0	QFB $\div 8$ In Frequency = 50MHz	-10	145	300	ps
		CLK1		-65	90	245	ps
		CLK, nCLK		-130	18	165	ps
$t_{sk(o)}$	Output Skew; NOTE 2					200	ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 3, 4		All Banks $\div 4$			55	ps
f_{VCO}	PLL VCO Lock Range			240		500	MHz
t_{LOCK}	PLL Lock Time; NOTE 3					10	mS
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	150		700	ps
odc	Output Duty Cycle			45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 3			2		10	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 3			2		8	ns

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

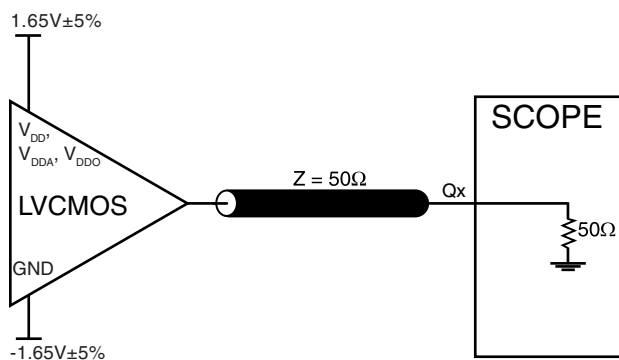
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

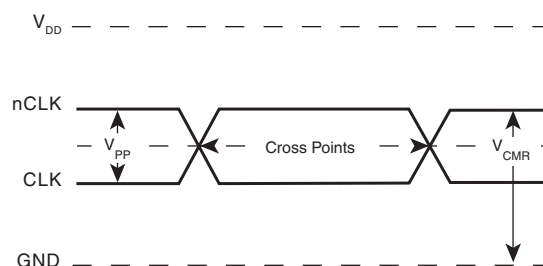
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



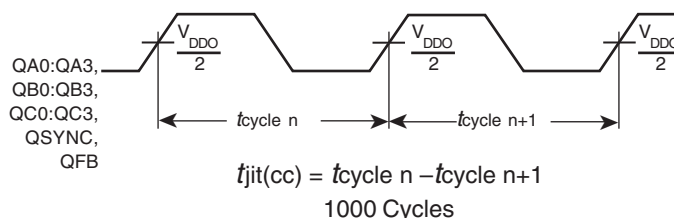
PARAMETER MEASUREMENT INFORMATION



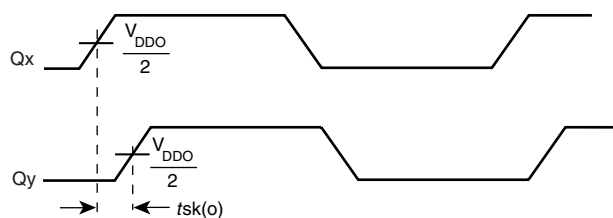
3.3V OUTPUT LOAD AC TEST CIRCUIT



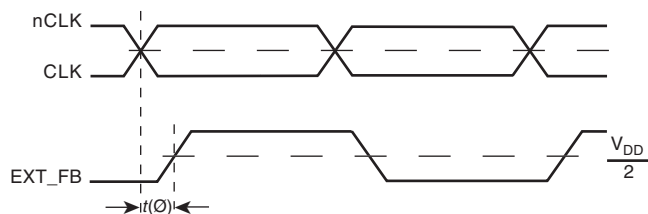
DIFFERENTIAL INPUT LEVEL



CYCLE-TO-CYCLE JITTER



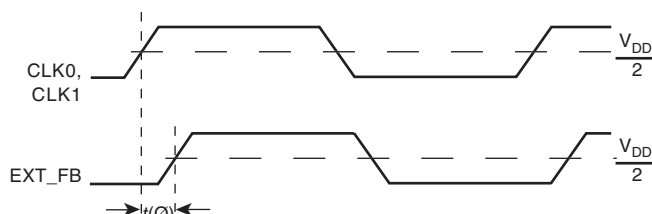
OUTPUT SKEW



$t(\emptyset) \text{ mean} = \text{Static Phase Offset}$

(where $t(\emptyset)$ is any random sample, and $t(\emptyset) \text{ mean}$ is the average of the sampled cycles measured on controlled edges)

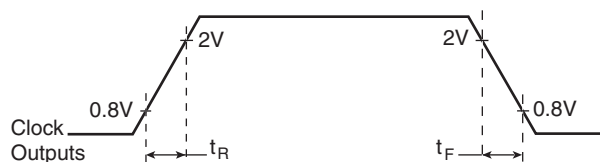
STATIC PHASE OFFSET (DIFFERENTIAL)



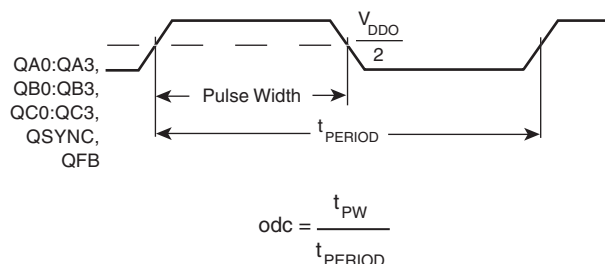
$t(\emptyset) \text{ mean} = \text{Static Phase Offset}$

(where $t(\emptyset)$ is any random sample, and $t(\emptyset) \text{ mean}$ is the average of the sampled cycles measured on controlled edges)

STATIC PHASE OFFSET (LVCMOS)



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/ PULSE WIDTH PERIOD



APPLICATION INFORMATION

USING THE OUTPUT FREEZE CIRCUITRY

OVERVIEW

To enable low power states within a system, each output of ICS87973I-147 (Except QC0 and QFB) can be individually frozen (stopped in the logic "0" state) using a simple serial interface to a 12 bit shift register. A serial interface was chosen to eliminate the need for each output to have its own Output Enable pin, which would dramatically increase pin count and package cost. Common sources in a system that can be used to drive the ICS87973I-147 serial interface are FPGA's and ASICs.

PROTOCOL

The Serial interface consists of two pins, FRZ_Data (Freeze Data) and FRZ_CLK (Freeze Clock). Each of the outputs which can be frozen has its own freeze enable bit in the 12 bit shift register. The sequence is started by supplying a logic "0" start bit followed by 12NRZ freeze enable bits. The period of each FRZ_DATA bit equals the period of the FRZ_CLK signal. The FRZ_DATA serial transmission should be timed so the ICS87973I-147 can sample each FRZ_DATA bit with the rising

edge of the FRZ_CLK signal. To place an output in the freeze state, a logic "0" must be written to the respective freeze enable bit in the shift register. To unfreeze an output, a logic "1" must be written to the respective freeze enable bit. Outputs will not become enabled/disabled until all 12 data bits are shifted into the shift register. When all 12 data bits are shifted in the register, the next rising edge of FRZ_CLK will enable or disable the outputs. If the bit that is following the 12th bit in the register is a logic "0", it is used for the start bit of the next cycle; otherwise, the device will wait and won't start the next cycle until it sees a logic "0" bit. Freezing and unfreezing of the output clock is synchronous (see the timing diagram below). When going into a frozen state, the output clock will go LOW at the time it would normally go LOW, and the freeze logic will keep the output low until unfrozen. Likewise, when coming out of the frozen state, the output will go HIGH only when it would normally go HIGH. This logic, therefore, prevents runt pulses when going into and out of the frozen state.

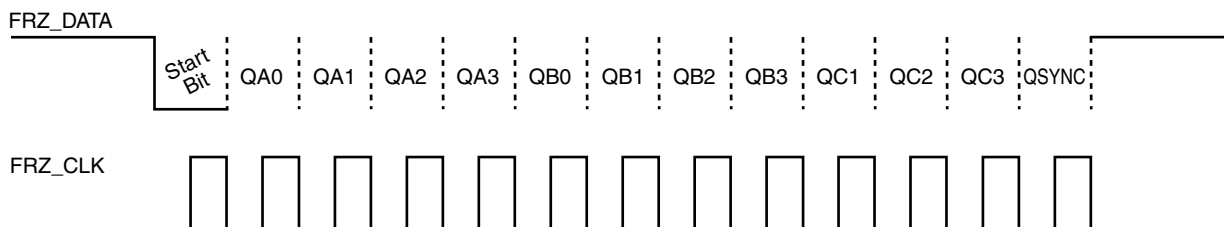


FIGURE 2A. FREEZE DATA INPUT PROTOCOL

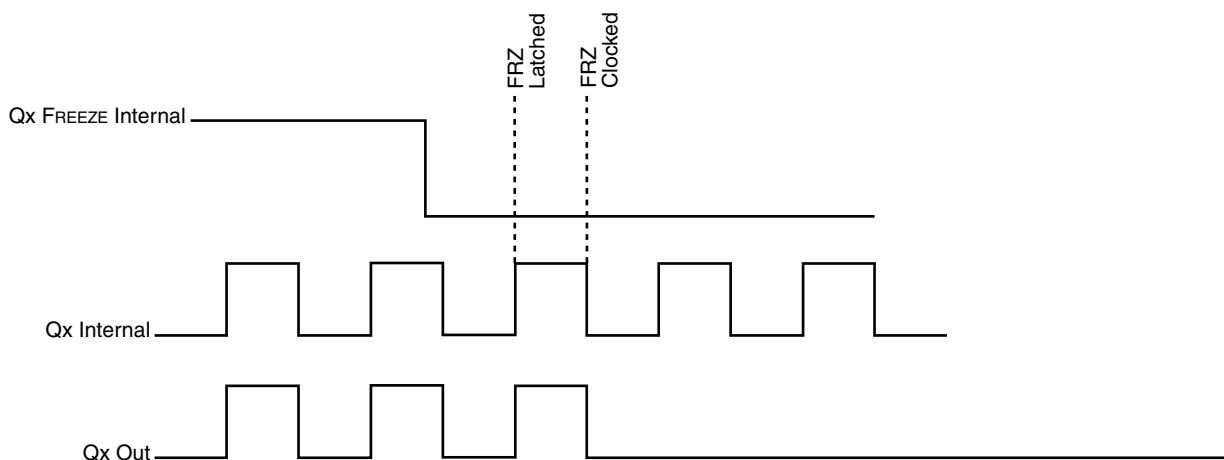


FIGURE 2B. OUTPUT DISABLE TIMING



POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87973I-147 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 3* illustrates how a 10Ω resistor along with a $10\mu F$ and a $.01\mu F$ bypass capacitor should be connected to each V_{DDA} pin.

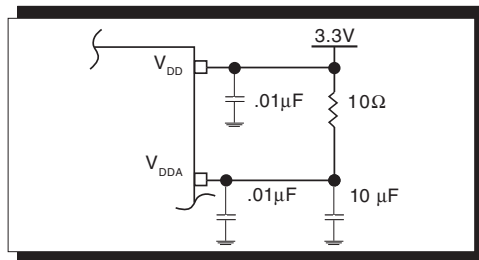


FIGURE 3. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 4 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors $R1$, $R2$ and $C1$. This bias circuit should be located as close as possible to the input pin. The ratio

of $R1$ and $R2$ might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

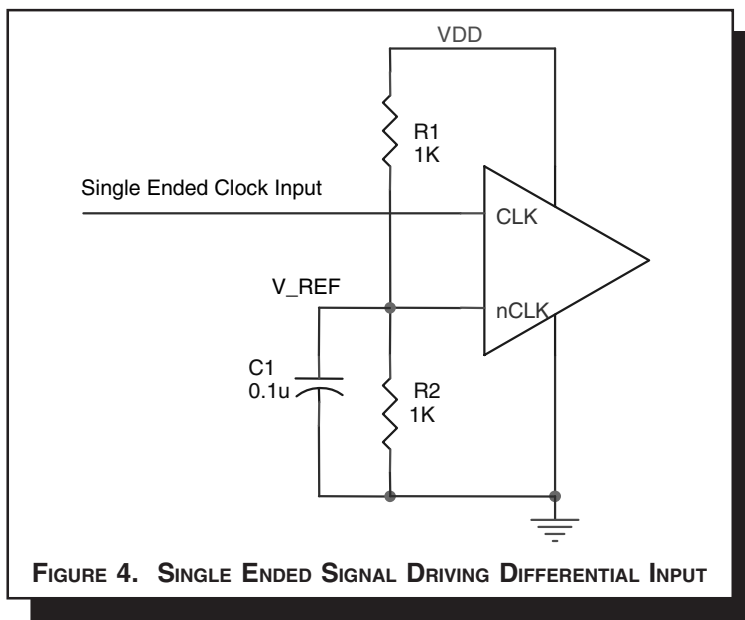


FIGURE 4. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 5A to 5D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 5A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

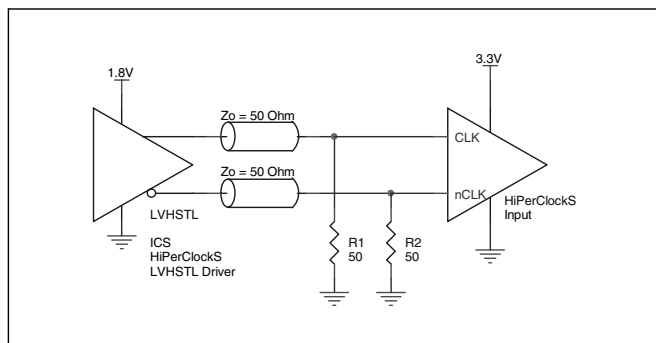


FIGURE 5A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER

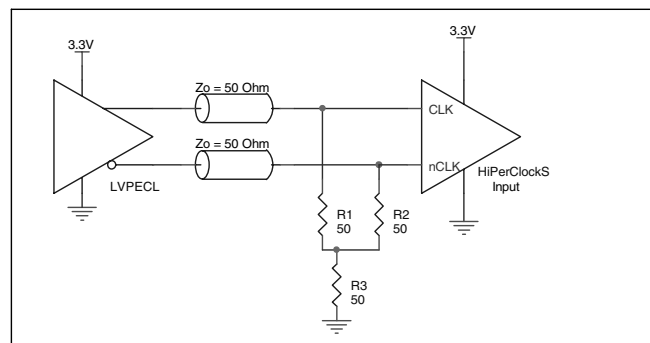


FIGURE 5B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

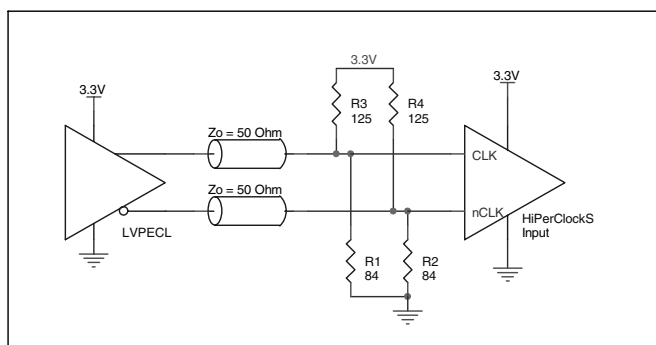


FIGURE 5C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

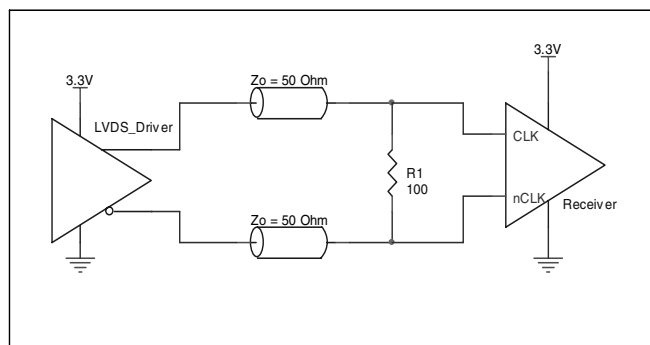


FIGURE 5D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER



SCHEMATIC EXAMPLE

Figure 6 shows a schematic example of using ICS87973I-147. This example shows general design of input, output termination, logic control input pull up/down and power supply filtering. In this example, the clock input is driven by an LVC MOS driver.

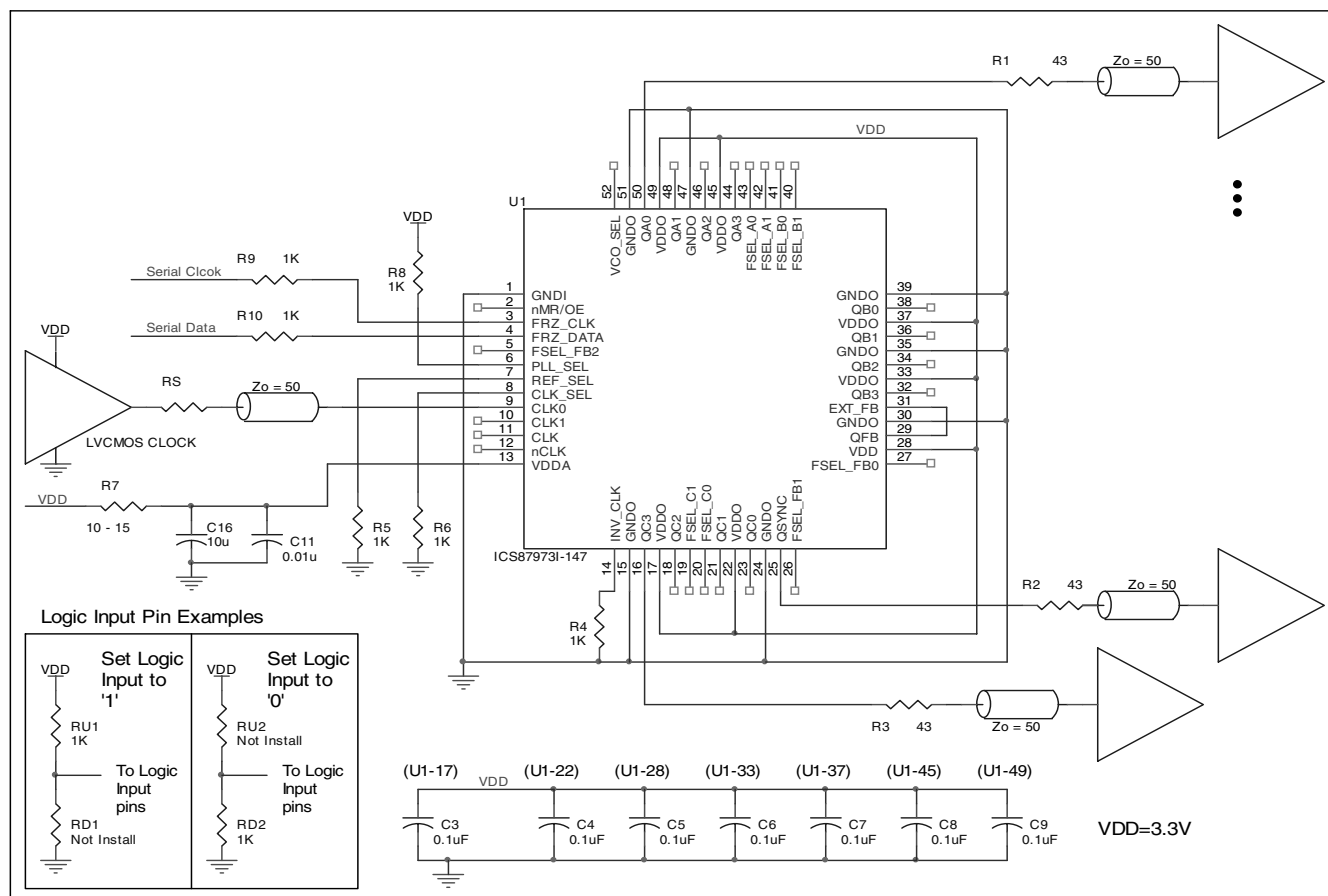


FIGURE 6. ICS87973I-147 SCHEMATIC EXAMPLE



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ICS87973I-147

LOW SKEW, 1-TO-12

LVC MOS / LV TTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87973I-147 is: 8364



Integrated
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ICS87973I-147

LOW SKEW, 1-TO-12

LVC MOS / LV TTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

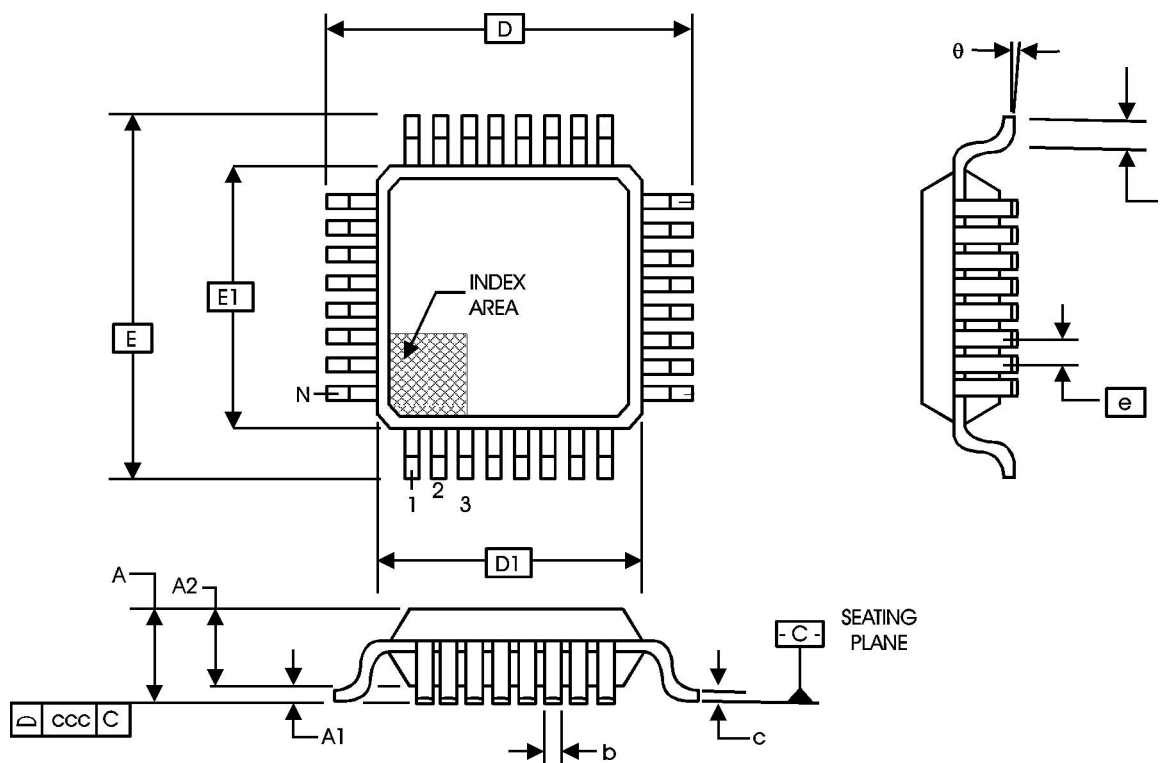


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N	52		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09	--	0.20
D	12.00 BASIC		
D1	10.00 BASIC		
E	12.00 BASIC		
E1	10.00 BASIC		
e	0.65 BASIC		
L	0.45	--	0.75
theta	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026



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ICS87973I-147

LOW SKEW, 1-TO-12
LVCMOS / LVTTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87973DYI-147	ICS7973DI147	52 Lead LQFP	160 per tray	-40°C to 85°C
ICS87973DYI-147T	ICS7973DI147	52 Lead LQFP on Tape and Reel	500	-40°C to 85°C

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