



## GENERAL DESCRIPTION



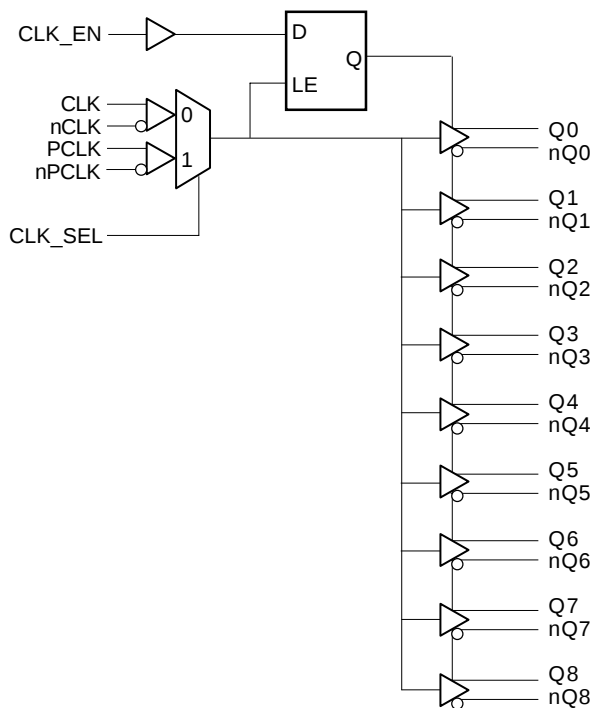
The ICS8521 is a low skew, 1-to-9 3.3V Differential-to-LVHSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8521 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output skew, part-to-part skew and crossover voltage characteristics make the ICS8521 ideal for today's most advanced applications, such as IA64 and static RAMs.

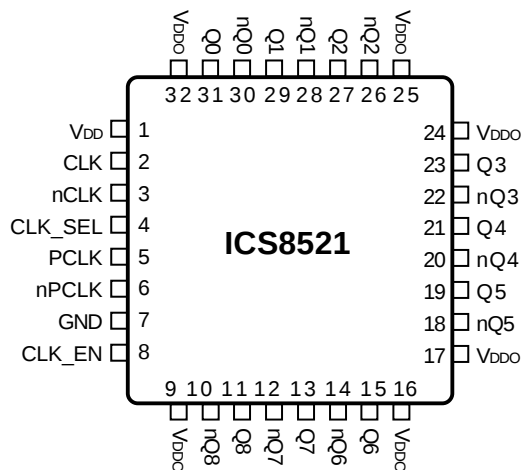
## FEATURES

- 9 LVHSTL outputs
- Selectable CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency up to 500MHz
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.8ns (maximum)
- $V_{OH} = 1.2V$  (maximum)
- 3.3V core, 1.8V output operating supply voltages
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**32-Lead LQFP**  
**7mm x 7mm x 1.4mm Package Body**  
**Y Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

| Number                   | Name             | Type   |          | Description                                                                                                                                                               |
|--------------------------|------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                        | V <sub>DD</sub>  | Power  |          | Positive supply pin. Connect to 3.3V.                                                                                                                                     |
| 2                        | CLK              | Input  | Pulldown | Non-inverting differential clock input.                                                                                                                                   |
| 3                        | nCLK             | Input  | Pullup   | Inverting differential clock input.                                                                                                                                       |
| 4                        | CLK_SEL          | Input  | Pulldown | Clock select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK. LVTTTL / LVCMOS interface levels.                                                 |
| 5                        | PCLK             | Input  | Pulldown | Non-inverting differential LVPECL clock input.                                                                                                                            |
| 6                        | nPCLK            | Input  | Pullup   | Inverting differential LVPECL clock input.                                                                                                                                |
| 7                        | GND              | Power  |          | Power supply ground. Connect to ground.                                                                                                                                   |
| 8                        | CLK_EN           | Input  | Pullup   | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS /LVTTTL interface levels. |
| 9, 16, 17,<br>24, 25, 32 | V <sub>DDO</sub> | Power  |          | Output supply pins. Connect to 1.8V.                                                                                                                                      |
| 10, 11                   | nQ8, Q8          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 12, 13                   | nQ7, Q7          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 14, 15                   | nQ6, Q6          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 18, 19                   | nQ5, Q5          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 20, 21                   | nQ4, Q4          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 22, 23                   | nQ3, Q3          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 26, 27                   | nQ2, Q2          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 28, 29                   | nQ1, Q1          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |
| 30, 31                   | nQ0, Q0          | Output |          | Differential output pair. LVHSTL interface level.                                                                                                                         |

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter               |                           | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|---------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       | CLK, nCLK,<br>PCLK, nPCLK |                 |         |         | 4       | pF    |
|                       |                         | CLK_EN, CLK_SEL           |                 |         |         | 4       | pF    |
|                       |                         |                           |                 |         |         |         |       |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                           |                 |         | 51      |         | KΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                           |                 |         | 51      |         | KΩ    |

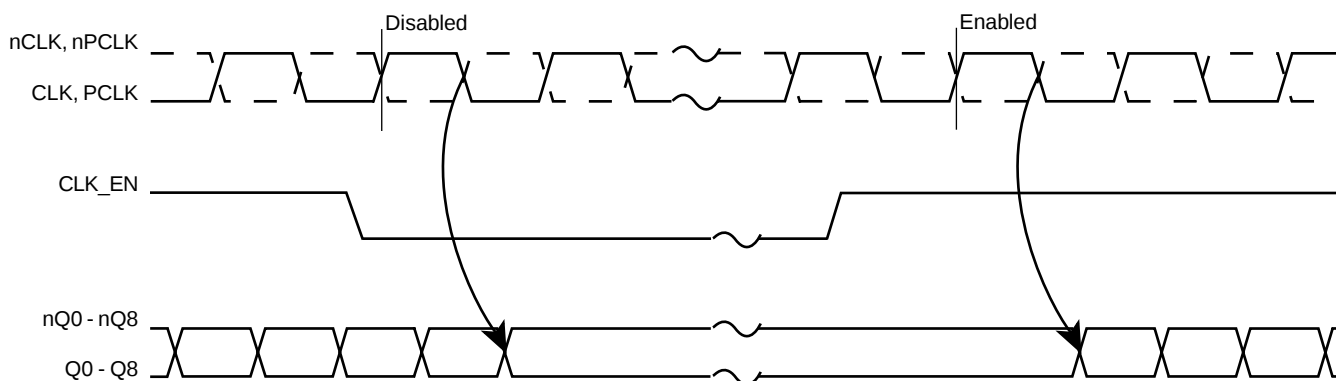


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

| Inputs |         |                  | Outputs       |                |
|--------|---------|------------------|---------------|----------------|
| CLK_EN | CLK_SEL | Selected Sourced | Q0 thru Q8    | nQ0 thru nQ8   |
| 0      | 0       | CLK, nCLK        | Disabled; LOW | Disabled; HIGH |
| 0      | 1       | PCLK, nPCLK      | Disabled; LOW | Disabled; HIGH |
| 1      | 0       | CLK, nCLK        | Enabled       | Enabled        |
| 1      | 1       | PCLK, nPCLK      | Enabled       | Enabled        |

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.



**FIGURE 1: CLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

| Inputs         |                | Outputs    |              | Input to Output Mode         | Polarity      |
|----------------|----------------|------------|--------------|------------------------------|---------------|
| CLK or PCLK    | nCLK or nPCLK  | Q0 thru Q8 | nQ0 thru nQ8 |                              |               |
| 0              | 1              | LOW        | HIGH         | Differential to Differential | Non Inverting |
| 1              | 0              | HIGH       | LOW          | Differential to Differential | Non Inverting |
| 0              | Biased; NOTE 1 | LOW        | HIGH         | Single Ended to Differential | Non Inverting |
| 1              | Biased; NOTE 1 | HIGH       | LOW          | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0              | HIGH       | LOW          | Single Ended to Differential | Inverting     |
| Biased; NOTE 1 | 1              | LOW        | HIGH         | Single Ended to Differential | Inverting     |

NOTE 1: Please refer to the Application Information section on page 8, Figure 9, which discusses wiring the differential input to accept single ended levels.



#### ABSOLUTE MAXIMUM RATINGS

|                                          |                           |
|------------------------------------------|---------------------------|
| Supply Voltage, $V_{DDX}$                | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W                  |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage   |                 | 1.6     | 1.8     | 2.0     | V     |
| $I_{DD}$  | Power Supply Current    |                 |         | 60      | 80      | mA    |

**TABLE 4B. LVCMOS DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter          | Test Conditions                           | Minimum | Typical | Maximum | Units   |
|----------|--------------------|-------------------------------------------|---------|---------|---------|---------|
| $V_{IH}$ | CLK_EN, CLK_SEL    |                                           | 2       |         | 3.765   | V       |
| $V_{IL}$ | CLK_EN, CLK_SEL    |                                           | -0.3    |         | 0.8     | V       |
| $I_{IH}$ | Input High Current | CLK_EN<br>$V_{IN} = V_{DD} = 3.465V$      |         |         | 5       | $\mu A$ |
|          |                    | CLK_SEL<br>$V_{IN} = V_{DD} = 3.465V$     |         |         | 150     | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK_EN<br>$V_{IN} = 0V, V_{DD} = 3.465V$  | -150    |         |         | $\mu A$ |
|          |                    | CLK_SEL<br>$V_{IN} = 0V, V_{DD} = 3.465V$ | -5      |         |         | $\mu A$ |

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol    | Parameter                               | Test Conditions                        | Minimum | Typical | Maximum         | Units   |
|-----------|-----------------------------------------|----------------------------------------|---------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                      | CLK<br>$V_{IN} = V_{DD} = 3.465V$      |         |         | 150             | $\mu A$ |
|           |                                         | nCLK<br>$V_{IN} = V_{DD} = 3.465V$     |         |         | 5               | $\mu A$ |
| $I_{IL}$  | Input Low Current                       | CLK<br>$V_{IN} = 0V, V_{DD} = 3.465V$  | -5      |         |                 | $\mu A$ |
|           |                                         | nCLK<br>$V_{IN} = 0V, V_{DD} = 3.465V$ | -150    |         |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage              |                                        | 0.15    |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage;<br>NOTE 1, 2 |                                        | 0.5     |         | $V_{DD} - 0.85$ | V       |

NOTE 1: For single ended applications, the maximum input voltage for CLK and nCLK is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS**,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

| Symbol    | Parameter                               | Test Conditions                            | Minimum | Typical | Maximum  | Units   |
|-----------|-----------------------------------------|--------------------------------------------|---------|---------|----------|---------|
| $I_{IH}$  | Input High Current                      | PCLK<br>$V_{DD} = V_{IN} = 3.465V$         |         |         | 150      | $\mu A$ |
|           |                                         | nPCLK<br>$V_{DD} = V_{IN} = 3.465V$        |         |         | 5        | $\mu A$ |
| $I_{IL}$  | Input Low Current                       | PCLK<br>$V_{DD} = 3.465V$ , $V_{IN} = 0V$  | -5      |         |          | $\mu A$ |
|           |                                         | nPCLK<br>$V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -150    |         |          | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage              |                                            | 0.3     |         | 1        | V       |
| $V_{CMR}$ | Common Mode Input Voltage;<br>NOTE 1, 2 |                                            | 1.5     |         | $V_{DD}$ | V       |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is  $V_{DD} + 0.3V$ .

**TABLE 4E. LVHSTL DC CHARACTERISTICS**,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

| Symbol      | Parameter                            | Test Conditions | Minimum                                  | Typical | Maximum                                  | Units |
|-------------|--------------------------------------|-----------------|------------------------------------------|---------|------------------------------------------|-------|
| $V_{OH}$    | Output High Voltage;<br>NOTE 1       |                 | 1.0                                      |         | 1.2                                      | V     |
| $V_{OL}$    | Output Low Voltage;<br>NOTE 1        |                 | 0                                        |         | 0.4                                      | V     |
| $V_{OX}$    | Output Crossover Voltage             |                 | $40\% \times (V_{OH} - V_{OL}) + V_{OL}$ |         | $60\% \times (V_{OH} - V_{OL}) + V_{OL}$ | V     |
| $V_{SWING}$ | Peak-to-Peak<br>Output Voltage Swing |                 | 0.6                                      |         | 1.1                                      | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to ground.

**TABLE 5. AC CHARACTERISTICS**,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$

| Symbol    | Parameter                    | Test Conditions    | Minimum | Typical | Maximum | Units |
|-----------|------------------------------|--------------------|---------|---------|---------|-------|
| $f_{MAX}$ | Maximum Output Frequency     |                    |         |         | 500     | MHz   |
| $t_{PD}$  | Propagation Delay; NOTE 1    | $f \leq 250MHz$    | 1       |         | 1.8     | ns    |
| $tsk(o)$  | Output Skew; NOTE 2, 4       |                    |         |         | 50      | ps    |
| $tsk(pp)$ | Part-to-Part Skew; NOTE 3, 4 |                    |         |         | 250     | ps    |
| $t_R$     | Output Rise Time             | 20% to 80% @ 50MHz | 300     |         | 700     | ps    |
| $t_F$     | Output Fall Time             | 20% to 80% @ 50MHz | 300     |         | 700     | ps    |
| odc       | Output Duty Cycle            |                    | 48      |         | 52      | %     |

All parameters measured at 250MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

Measured from  $V_{DD}/2$  to the output differential crossing point for single ended input levels.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

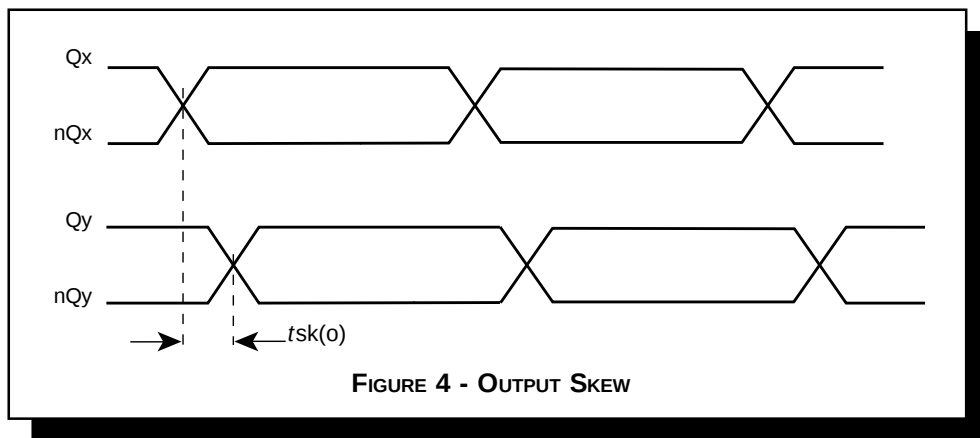
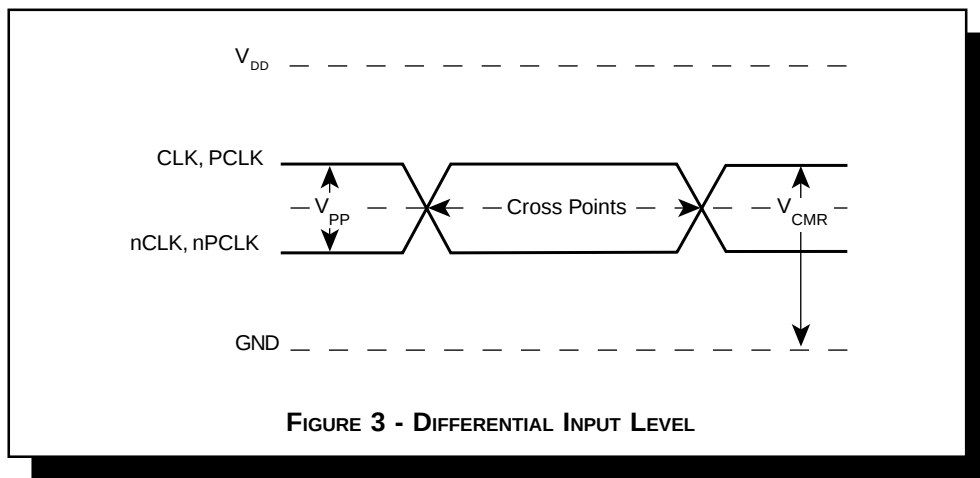
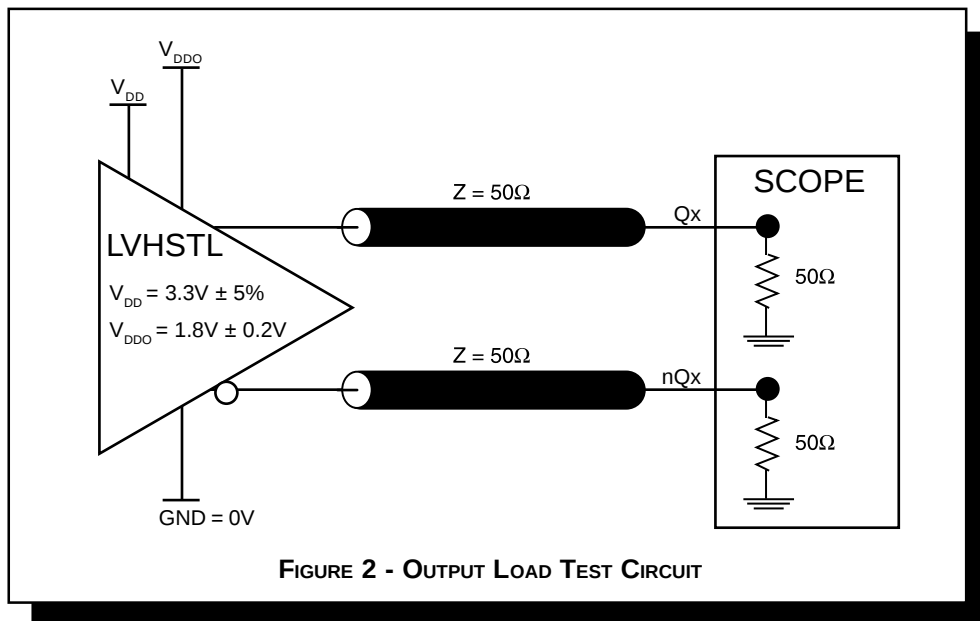
Measured at the output differential cross points.

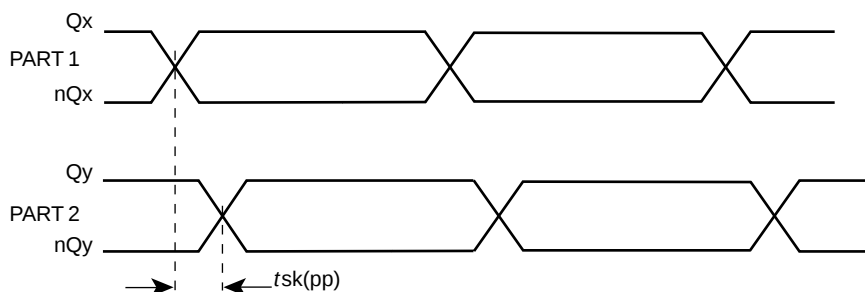
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the output are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



## PARAMETER MEASUREMENT INFORMATION

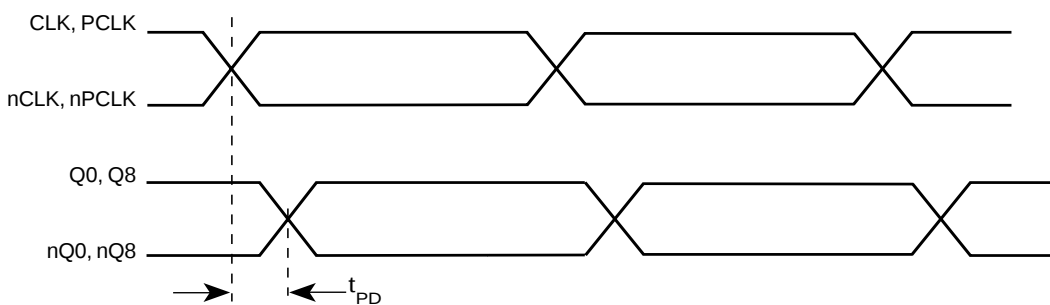




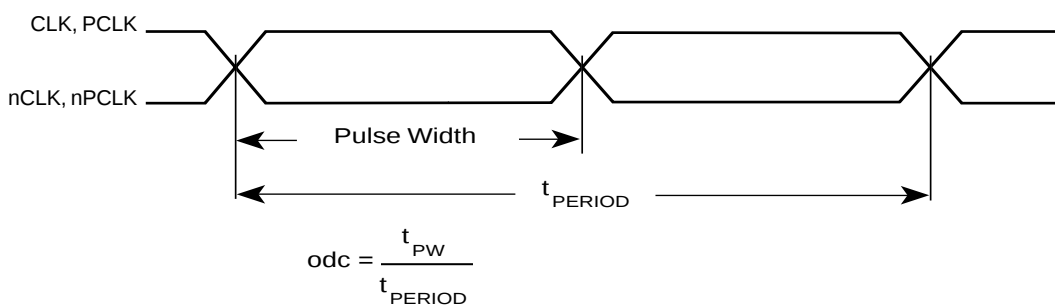
**FIGURE 5 - PART-TO-PART SKEW**



**FIGURE 6 - INPUT AND OUTPUT RISE AND FALL TIME**



**FIGURE 7 - PROPAGATION DELAY**



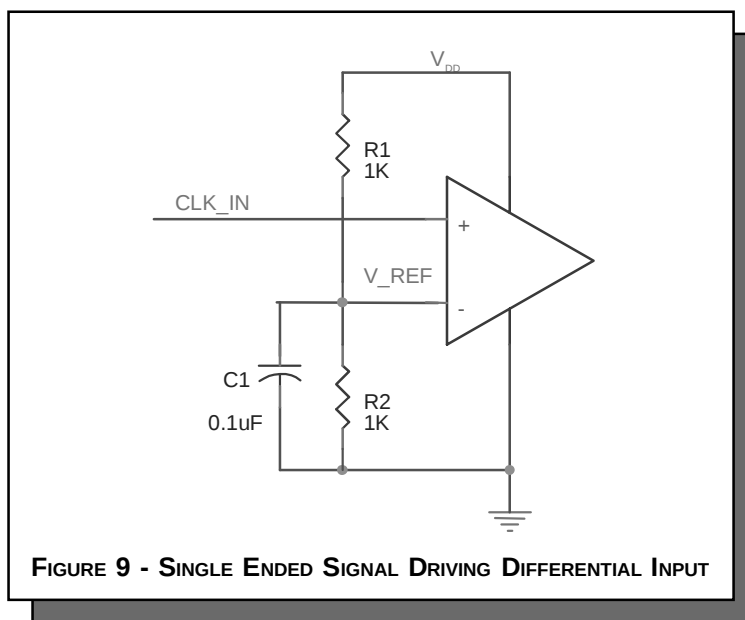
**FIGURE 8 - odc &  $t_{PERIOD}$**



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 9 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} \approx V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .





## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8521. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8521 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 80mA = 277.2mW$
- Power (outputs)<sub>MAX</sub> = **32mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $9 * 32mW = 288mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 277.2mW + 288mW = 565.2mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-ambient thermal resistance

$Pd\_total$  = Total device power dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below. Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.565W * 42.1^\circ C/W = 93.8^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 32-pin LQFP, Forced Convection**

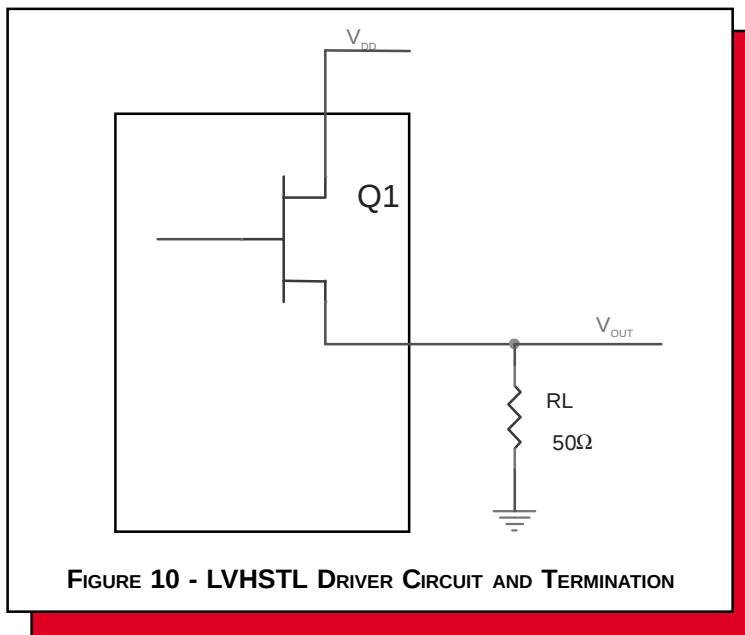
| $\theta_{JA}$ by Velocity (Linear Feet per Minute)                                                                  |          |          |          |
|---------------------------------------------------------------------------------------------------------------------|----------|----------|----------|
|                                                                                                                     | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards                                                                        | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards                                                                         | 47.9°C/W | 42.1°C/W | 39.4°C/W |
| <b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. |          |          |          |



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 10*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{DD} - 2V$ .

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MAX} / R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$$

$$Pd\_L = (V_{OL\_MAX} / R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$$

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{DD\_MAX} - 1.2V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{DD\_MAX} - 0.4V$

$$Pd\_H = (1.2V/50\Omega) * (2V - 1.2V) = \mathbf{19.2mW}$$

$$Pd\_L = (0.4V/50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{32mW}$$



## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|----------------------------------------------------|----------|----------|----------|
|                                                    | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8521 is: 944



Integrated  
Circuit  
Systems, Inc.

# ICS8521

LOW SKEW, 1-TO-9  
DIFFERENTIAL-TO-LVHSTL FANOUT BUFFER

## PACKAGE OUTLINE - Y SUFFIX

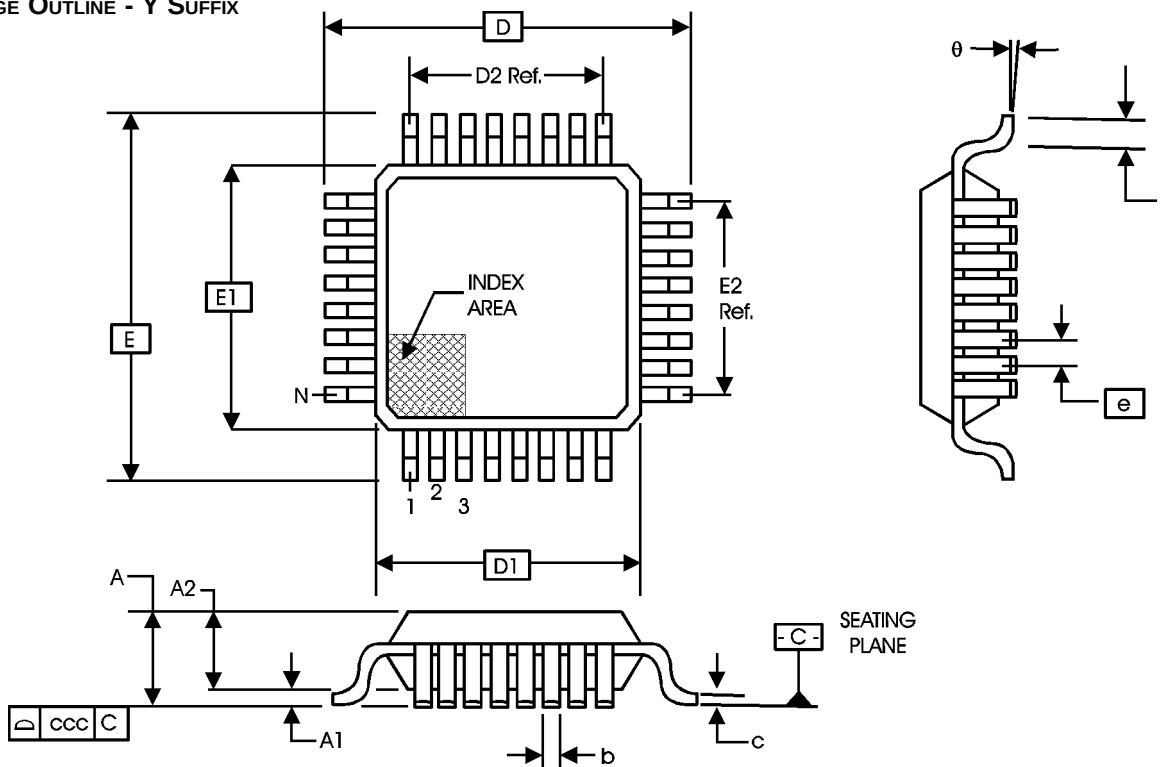


TABLE 6. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--------------------------------------------------|------------|---------|---------|
| SYMBOL                                           | BBA        |         |         |
|                                                  | MINIMUM    | NOMINAL | MAXIMUM |
| N                                                | 32         |         |         |
| A                                                | --         | --      | 1.60    |
| A1                                               | 0.05       | --      | 0.15    |
| A2                                               | 1.35       | 1.40    | 1.45    |
| b                                                | 0.30       | 0.37    | 0.45    |
| c                                                | 0.09       | --      | 0.20    |
| D                                                | 9.00 BASIC |         |         |
| D1                                               | 7.00 BASIC |         |         |
| D2                                               | 5.60 Ref.  |         |         |
| E                                                | 9.00 BASIC |         |         |
| E1                                               | 7.00 BASIC |         |         |
| E2                                               | 5.60 Ref.  |         |         |
| e                                                | 0.80 BASIC |         |         |
| L                                                | 0.45       | 0.60    | 0.75    |
| $\theta$                                         | 0°         | --      | 7°      |
| ccc                                              | --         | --      | 0.10    |

Reference Document: JEDEC Publication 95, MS-026



Integrated  
Circuit  
Systems, Inc.

# ICS8521

LOW SKEW, 1-TO-9  
DIFFERENTIAL-TO-LVHSTL FANOUT BUFFER

TABLE 7. ORDERING INFORMATION

| Part/Order Number | Marking   | Package                       | Count        | Temperature |
|-------------------|-----------|-------------------------------|--------------|-------------|
| ICS8521BY         | ICS8521BY | 32 Lead LQFP                  | 250 per tray | 0°C to 70°C |
| ICS8521BYT        | ICS8521BY | 32 Lead LQFP on Tape and Reel | 1000         | 0°C to 70°C |

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