



GENERAL DESCRIPTION

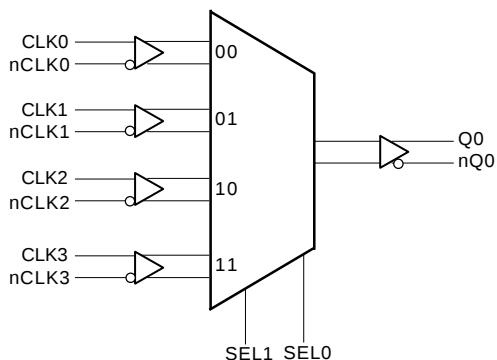


The ICS85357-01 is a 4:1 or 2:1 Differential-to-3.3V LVPECL / ECL clock multiplexer which can operate up to 750MHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85357-01 has 4 selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The device can operate using a 3.3V LVPECL ($V_{EE} = 0V$, $V_{CC} = 3.135V$ to $3.465V$) or 3.3V ECL ($V_{CC} = 0V$, $V_{EE} = -3.135V$ to $-3.465V$). The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. Leaving one input unconnected (pulled to logic low by the internal resistor) will transform the device into a 2:1 multiplexer. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects CLK0, nCLK0).

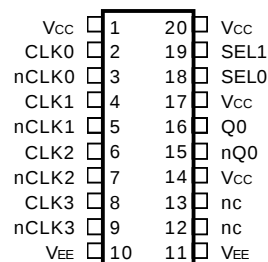
FEATURES

- High speed differential multiplexer. The device can be configured as either a 4:1 or 2:1 multiplexer
- 1 differential 3.3V LVPECL output
- 4 selectable CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency up to 750MHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLKx input
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 1.5ns (maximum)
- LVPECL mode operating voltage supply range:
 $V_{CC} = 3.135V$ to $3.465V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range:
 $V_{CC} = 0V$, $V_{EE} = -3.135V$ to $-3.465V$
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85357-01

20-Lead TSSOP

4.40mm x 6.50mm x 0.90mm body package

G Package

Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 14, 17, 20	V _{CC}	Power		Positive supply pins. Connect to 3.3V.
2	CLK0	Input	Pulldown	Non-inverting differential clock input.
3	nCLK0	Input	Pullup	Inverting differential clock input.
4	CLK1	Input	Pulldown	Non-inverting differential clock input.
5	nCLK1	Input	Pullup	Inverting differential clock input.
6	CLK2	Input	Pulldown	Non-inverting differential clock input.
7	nCLK2	Input	Pullup	Inverting differential clock input.
8	CLK3	Input	Pulldown	Non-inverting differential clock input.
9	nCLK3	Input	Pullup	Inverting differential clock input.
10, 11	V _{EE}	Power		Negative supply pins. Connect to ground.
12, 13	nc	Unused		No connect.
15, 16	nQ0, Q0	Output		Differential output pairs. LVPECL interface levels.
18	SEL0	Input	Pulldown	Clock select input. LVCMOS / LVTTTL interface levels.
19	SEL1	Input	Pulldown	Clock select input. LVCMOS / LVTTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance	CLK, nCLK, CLK1, nCLK1, CLK2, nCLK2, CLK3, nCLK3				4	pF
		SEL0, SEL1				4	pF
R _{PULLUP}	Input Pullup Resistor				51		KΩ
R _{PULLDOWN}	Input Pulldown Resistor				51		KΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs		Clock Out
SEL1	SEL0	CLK
0	0	CLK0, nCLK0
0	1	CLK1, nCLK1
1	0	CLK2, nCLK2
1	1	CLK3, nCLK3



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, V_O	-0.5V to $V_{CC} + 0.5V$
Package Thermal Impedance, θ_{JA}	73.2°C/W (0lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				35	mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0, SEL1	2		3.765	V
V_{IL}	Input Low Voltage	SEL0, SEL1	-0.3		0.8	V
I_{IH}	Input High Current	SEL0, SEL1 $V_{CC} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	SEL0, SEL1 $V_{CC} = 3.465V, V_{IN} = 0V$	-5			μA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, CLK2, CLK3 $V_{CC} = V_{IN} = 3.465V$			150	μA
		nCLK0, nCLK1, nCLK2, nCLK3 $V_{CC} = V_{IN} = 3.465V$			5	μA
I_{IL}	Input Low Current	CLK0, CLK1, CLK2, CLK3 $V_{CC} = 3.465V, V_{IN} = 0V$	-5			μA
		nCLK0, nCLK1, nCLK2, nCLK3 $V_{CC} = 3.465V, V_{IN} = 0V$	-150			μA
V_{PP}	Peak-to-Peak Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: Common mode input voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is $V_{CC} + 0.3V$.



TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 1.0$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				750	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq 750MHz$	1	1.2	1.5	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				150	ps
t_R	Output Rise Time	20% to 80% @50MHz	300	400	700	ps
t_F	Output Fall Time	20% to 80% @50MHz	300	400	700	ps
odc	Output Duty Cycle		47		53	%

All parameters measured at 500MHz unless noted otherwise.

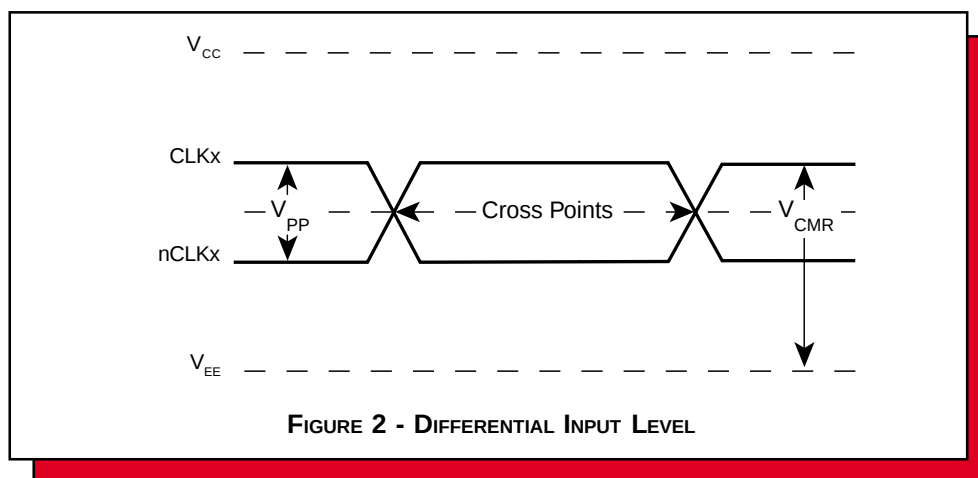
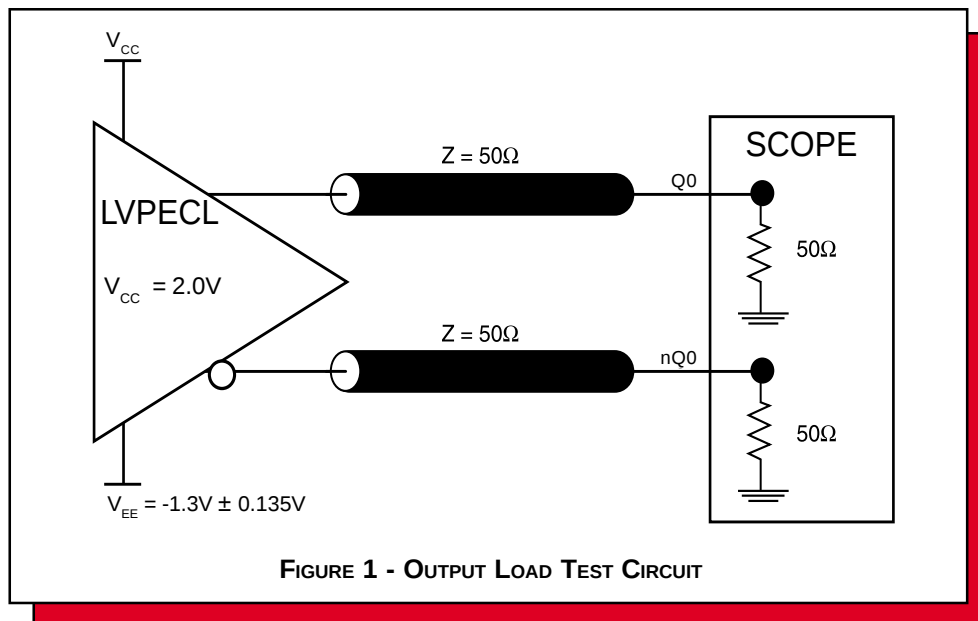
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



PARAMETER MEASUREMENT INFORMATION



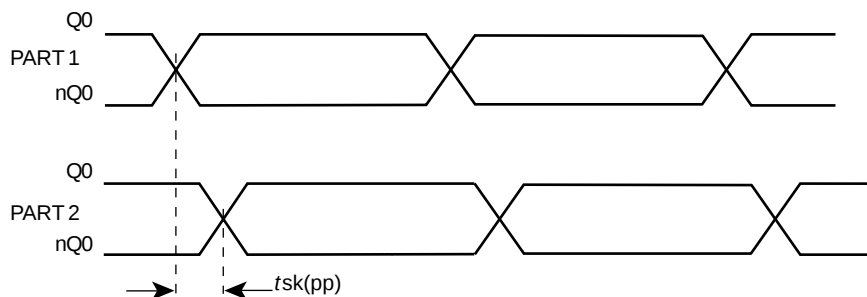


FIGURE 3- PART-TO-PART SKEW



FIGURE 4 - INPUT AND OUTPUT RISE AND FALL TIME

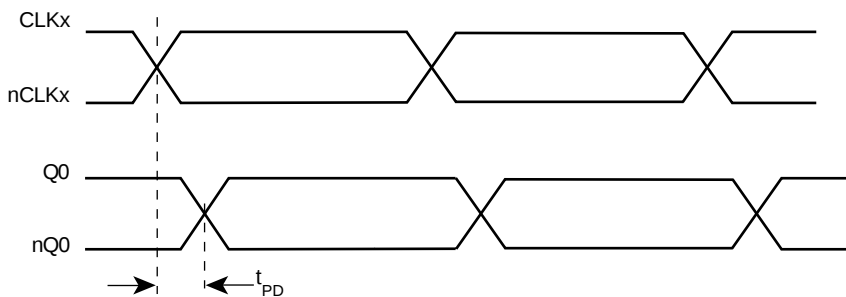


FIGURE 5 - PROPAGATION DELAY

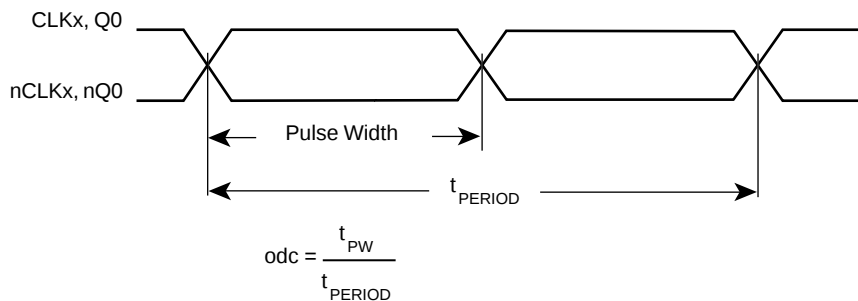


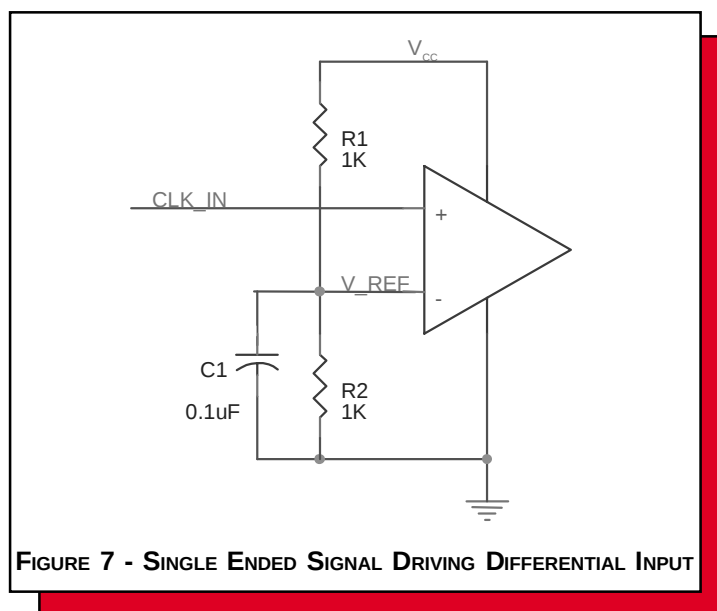
FIGURE 6 - odc & t_{PERIOD}



APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 7 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} \approx V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.





POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85357-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85357-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 35mA = 121.3mW$
- Power (outputs)_{MAX} = **30.2mW/Loaded Output pair**
If all outputs are loaded, the total power is $1 * 30.2mW = 30.2mW$

$$\text{Total Power}_{_MAX} (3.465V, \text{ with all outputs switching}) = 173.25mW + 120.8mW = 151.5mW$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = junction-to-ambient thermal resistance

Pd_total = Total device power dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.151W * 66.6^\circ C/W = 80.06^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

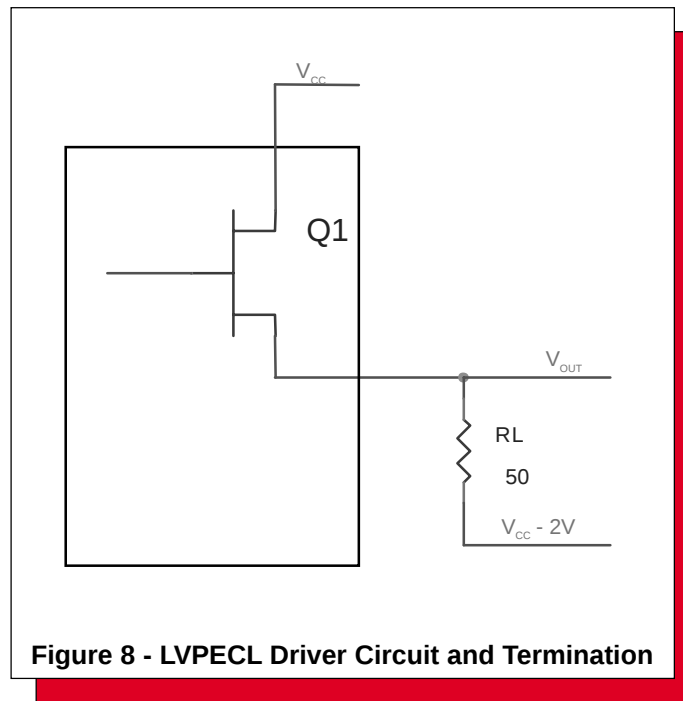
θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V)) / R_L] * (V_{CC_MAX} - V_{OH_MAX})$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V)) / R_L] * (V_{CC_MAX} - V_{OL_MAX})$$

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 1.0V$
Using $V_{CC_MAX} = 3.465V$, this results in $V_{OH_MAX} = 2.465V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$
Using $V_{CC_MAX} = 3.465V$, this results in $V_{OL_MAX} = 1.765V$

$$Pd_H = [(2.465V - (3.465V - 2V)) / 50\Omega] * (3.465V - 2.465V) = 20mW$$

$$Pd_L = [(1.765V - (3.465V - 2V)) / 50\Omega] * (3.465V - 1.765V) = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30.2mW$$



RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85357-01 is: 400



PACKAGE OUTLINE - G SUFFIX

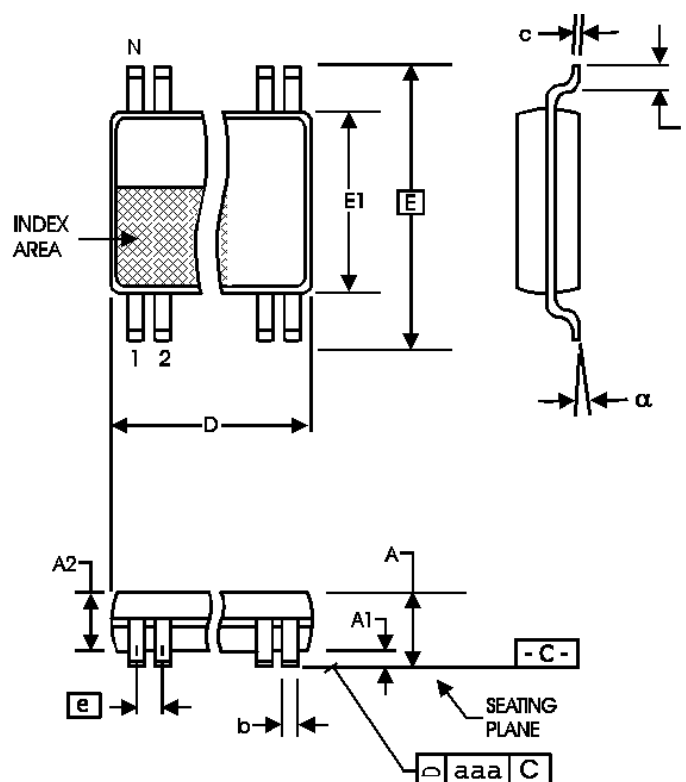


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



Integrated
Circuit
Systems, Inc.

ICS85357-01

4:1 OR 2:1

DIFFERENTIAL-TO-3.3V LVPECL / ECL CLOCK MULTIPLEXER

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85357AG-01	ICS85357AG-01	20 lead TSSOP	74 per tube	0°C to 70°C
ICS85357AG-01T	ICS85357AG-01	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C

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