

SRM2A256LLMX_{70/85/10}

256K-Bit Static RAM

- Low Supply Current
- Access Time 70ns/85ns/100ns
- 32,768 WordsX8-bit Asynchronous

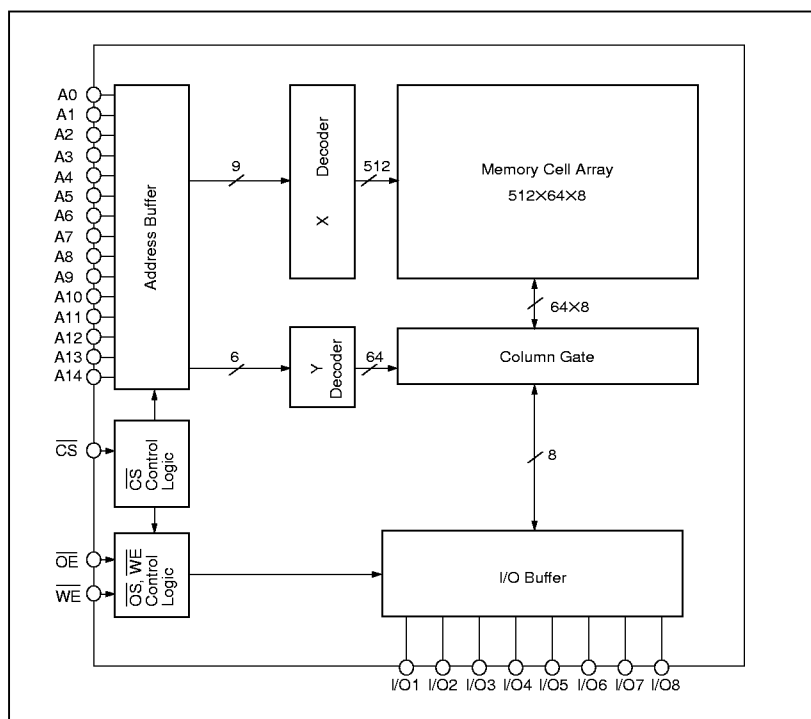
DESCRIPTION

The SRM2A256LLMX_{70/85/10} is a 32,768 wordsx8-bit asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

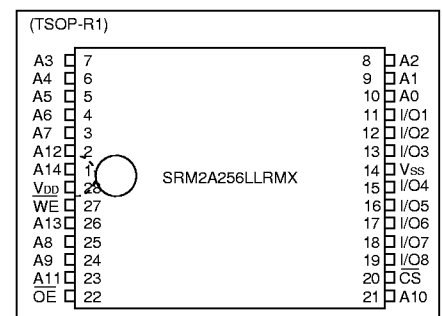
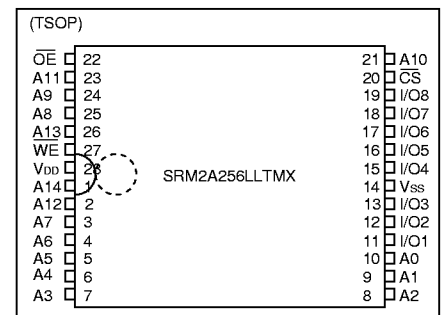
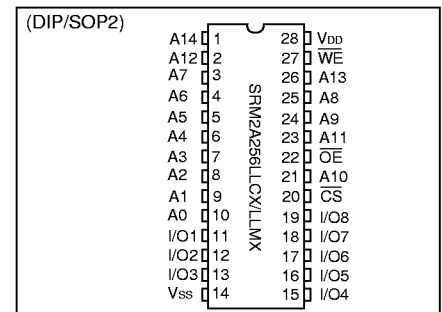
FEATURES

- Wide temperature range -25 to 85%
- Fast access time SRM2A256LLMX₇₀ 70ns
SRM2A256LLMX₈₅ 85ns
SRM2A256LLMX₁₀ 100ns
- Low supply current LL Version
- Completely static no clock required
- Single power supply 5V±10%
- TTL compatible inputs and outputs
- 3-state output
- Battery back-up operation
- Package SRM2A256LLCX_{70/85/10} DIP-28pin (plastic)
SRM2A256LLMX_{70/85/10} SOP2-28pin (plastic)
SRM2A256LLTMX_{70/85/10} TSOP(I)-28pin (plastic)
SRM2A256LLRMX_{70/85/10} TSOP(I)-28pin-R (plastic)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

A0 to A14	Address Input
WE	Write Enable
OE	Output Enable
CS	Chip Select
I/O1 to O8	Data Input/Output
VDD	Power Supply(+5V)
Vss	Power Supply(0V)

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage	V _I	-0.5* to 7.0	V
Input/Output voltage	V _{I/O}	-0.5* to V _{DD} +0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	-25 to 85	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s(Lead only)	—

* V_I, V_{I/O} (Min.)= -3V when pulse width is less or equal to 50ns

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=-25 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}		4.5	5.0	5.5	V
	V _{SS}		0	0	0	V
Input voltage	V _{IH}		2.2	—	V _{DD} +0.3	V
	V _{IL}		-0.3*	0	0.8	V

* V_{IL} (Min.)= -3V when pulse width is less or equal to 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=-25 to 85°C)

Parameter	Symbol	Conditions	SRM2A256LLMX70			SRM2A256LLMX85			SRM2A256LLMX10			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.	Max.	
Input leakage	V _{LI}	V _I =0 to V _{DD}	-1	—	1	-1	—	1	-1	—	1	μA
Output leakage	I _{LO}	CS=V _{IH} or WE=V _{IL} or OE=V _{IH} V _{I/O} =0 to V _{DD}	-1	—	1	-1	—	1	-1	—	1	μA
High level output voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V
Low level output voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	—	—	0.4	V
Standby supply current	I _{DDS}	CS=V _{IH}	—	0.5	3.0	—	0.5	3.0	—	0.5	3.0	mA
	I _{DDS1}	CS≥V _{DD} -0.2V	—	1	100	—	1	100	—	1	100	μA
Average operating current	I _{DDA}	V _I =V _{IL} , V _{IH} I _{I/O} =0mA, t _{cyc} =Min.	—	45	70	—	45	70	—	45	70	mA
	I _{DDA1}	V _I =V _{IL} , V _{IH} I _{I/O} =0mA, t _{cyc} =1μs	—	—	10	—	—	10	—	—	10	mA
Operating supply current	I _{DD0}	V _I =V _{IL} , V _{IH} I _{I/O} =0mA	—	—	10	—	—	10	—	—	10	mA

*: Typical values are measured at Ta=25°C and V_{DD}=5.0V

● Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C _{ADD}	V _{ADD} =0V	—	—	8	pF
Input Capacitance	C _I	V _I =0V	—	—	9	pF
I/O Capacitance	C _{I/O}	V _{I/O} =0V	—	—	10	pF

● AC Electrical Characteristics

○ Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=-25 to 85°C)

Parameter	Symbol	Conditions	SRM2A256LLMX70		SRM2A256LLMX85		SRM2A256LLMX10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	*1	70	—	85	—	100	—	ns
Address access time	t _{ACC}		—	70	—	85	—	100	ns
CS access time	t _{ACS}		—	70	—	85	—	100	ns
OE access time	t _{OE}		—	40	—	45	—	50	ns
CS output set time	t _{CLZ}	*2	10	—	10	—	10	—	ns
CS output floating	t _{CHZ}		—	30	—	30	—	35	ns
OE output set time	t _{OLZ}		0	—	0	—	0	—	ns
OE output floating	t _{OHZ}		—	30	—	30	—	35	ns
Output hold time	t _{OH}	*1	10	—	10	—	10	—	ns

SRM2A256LLMX70/85/10

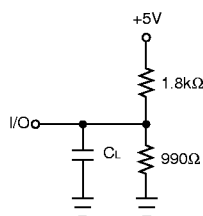
○ Write Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $T_a=-25$ to $85^\circ C$)

Parameter	Symbol	Conditions	SRM2A256LLMX70		SRM2A256LLMX85		SRM2A256LLMX10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	*1	70	—	85	—	100	—	ns
Chip select time	t_{CW}		60	—	70	—	80	—	ns
Address valid to end of write	t_{AW}		60	—	70	—	80	—	ns
Address setup time	t_{AS}		0	—	0	—	0	—	ns
Write pulse width	t_{WP}		55	—	65	—	75	—	ns
Address hold time	t_{WR}		0	—	0	—	0	—	ns
Input data set time	t_{DW}		30	—	35	—	40	—	ns
Input data hold time	t_{DH}		0	—	0	—	0	—	ns
Write to Output floating	t_{WHZ}	*2	—	30	—	30	—	35	ns
Output Active from end to write	t_{OW}		5	—	5	—	5	—	ns

*1 Test Conditions

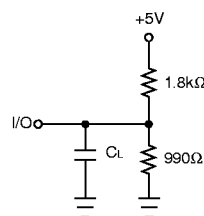
1. Input pulse level : 0.6V to 2.4V
2. $t_r=t_f=5ns$
3. Input and output timing reference levels : 1.5V
4. Output load : $C_L=100pF$



$C_L=100pF$ (Includes Jig Capacitance)

*2 Test Conditions

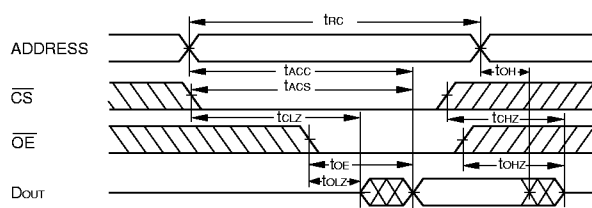
1. Input pulse level : 0.6V to 2.4V
2. $t_r=t_f=5ns$
3. Input timing reference levels : 1.5V
4. Output timing reference levels : 200mV (the level displaced from stable output voltage level)
5. Output load : $C_L=5pF$ (Includes Jig Capacitance)



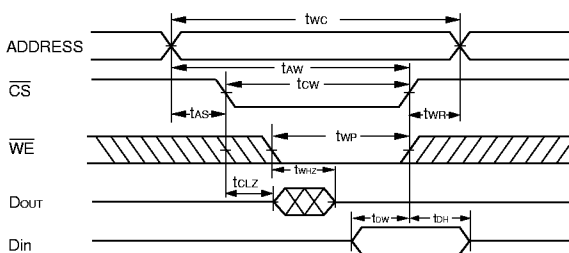
$C_L=5pF$ (Includes Jig Capacitance)

■ Timing chart

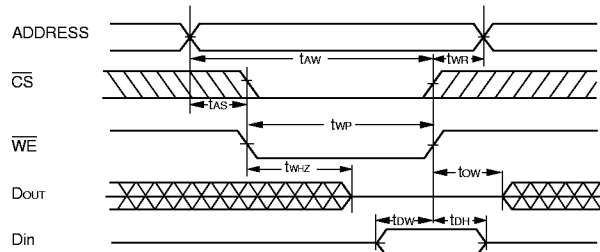
○ Read Cycle*1



○ Write Cycle(1) ($\overline{CS}$ Control)*2



○ Write Cycle(2) ($\overline{WE}$ Control)*3, *4



Note :

- *1 During read cycle time, $\overline{WE}$ is to be "H" level.
- *2 During write cycle time that is controlled by $\overline{CS}$, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L"
- *3 During write cycle time that is controlled by $\overline{WE}$, Output Buffer is in high impedance state if $\overline{OE}$ is "L" level.
- *4 When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

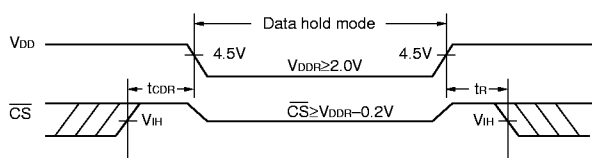
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V_{SS}=0V, Ta=-25 to 85°C)

Parameter	Symbol	Conditions	SRM2A256LLMX70			SRM2A256LLMX85			SRM2A256LLMX10			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Data retention supply voltage	V _{DDR}		2.0	—	5.5	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{DDR}	V _{DDR} =3V CS≥V _{DD} -0.2V	—	0.5	50	—	0.5	50	—	0.5	50	μA
Chip select data hold time	t _{CDR}		0	—	—	0	—	—	0	—	—	ns
Operation recovery time	t _R		5	—	—	5	—	—	5	—	—	ms

* : Typical values are measured at 25°C

Data retention timing



*When retaining data in standby mode, supply voltage can be lowered within a certain range, But read or write cycle cannot be performed while the supply voltage is low.

■ FUNCTIONS

● Truth Table

CS	OE	WE	DATA I/O	Mode	I _{DD}
H	X	X	Hi-Z	Standby	I _{DDS} , I _{DDS1}
L	X	L	D _{IN}	Write	I _{DDA} , I _{DDA1}
L	L	H	D _{OUT}	Read	I _{DDA} , I _{DDA1}
L	H	H	Hi-Z	Output disable	I _{DDA} , I _{DDA1}

X : "H" or "L"

● Read Mode

The data appear when the address is setted while holding CS="L", OE="L" and WE="H". When OE="H", DATA I/O terminals are in high impedance state, that makes circuit design and bus control easy.

● Write Mode

There are the following 3 ways of writing data into memory.

- (1) Hold CS="L" and WE="L", set address.
- (2) Hold CS="L" then set address and give "L" pulse to WE.
- (3) After setting addresses, give "L" pulse to both CS and WE.

In above any case data on the DATA I/O terminals are put into the SRM2A256LLMX70/85/10 when both CS and WE are in "L". Since DATA I/O terminals are high impedance when CS or OE="H", bus contention between data driver and memory outputs can be avoided.

When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

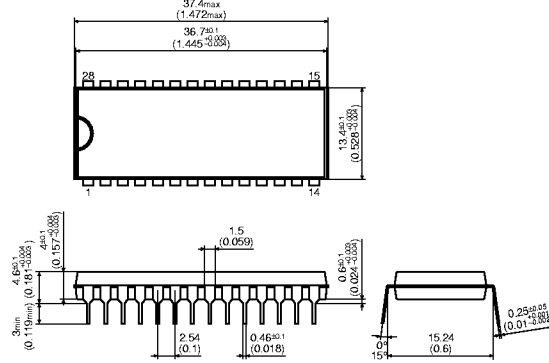
● Standby Mode

When CS is "L" the SRM2A256LLMX70/85/10 become in the standby mode. In this mode, data I/O terminals are Hi-Z and all inputs of addresses, WE and data can be any "H" or "L". When CS is over than V_{DD}-0.2V, the SRM2A256LLMX70/85/10 is in the data retention battery back-up mode, in this case, there is a small current in the SRM2A256LLMX70/85/10 which flow through the high resistances of the memory cells.

SRM2A256LLMX70/85/10

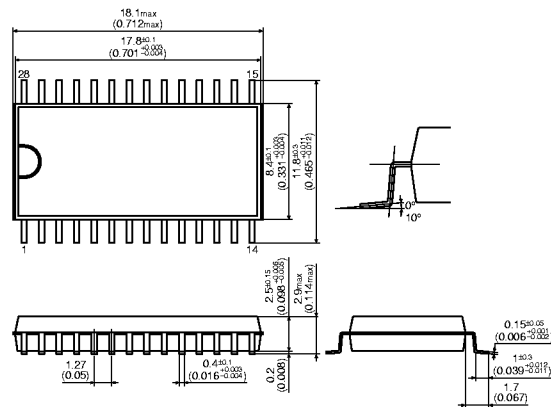
■ PACKAGE DIMENSIONS

Plastic DIP-28pin (600mil)*



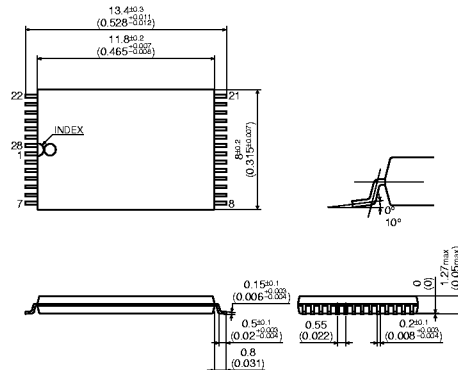
Unit : mm
(inch)

Plastic SOP2-28pin (450mil)



Unit : mm
(inch)

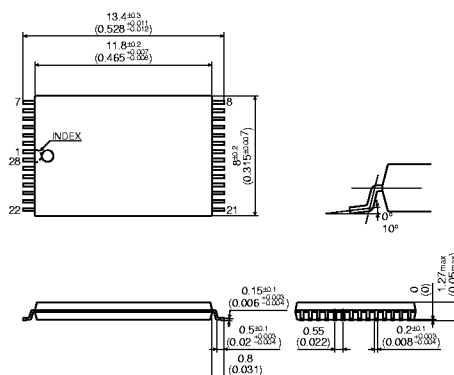
Plastic TSOP (I)-28pin*



Unit : mm
(inch)

* : The same characteristics as SRM2A256LLMX70/85/10.

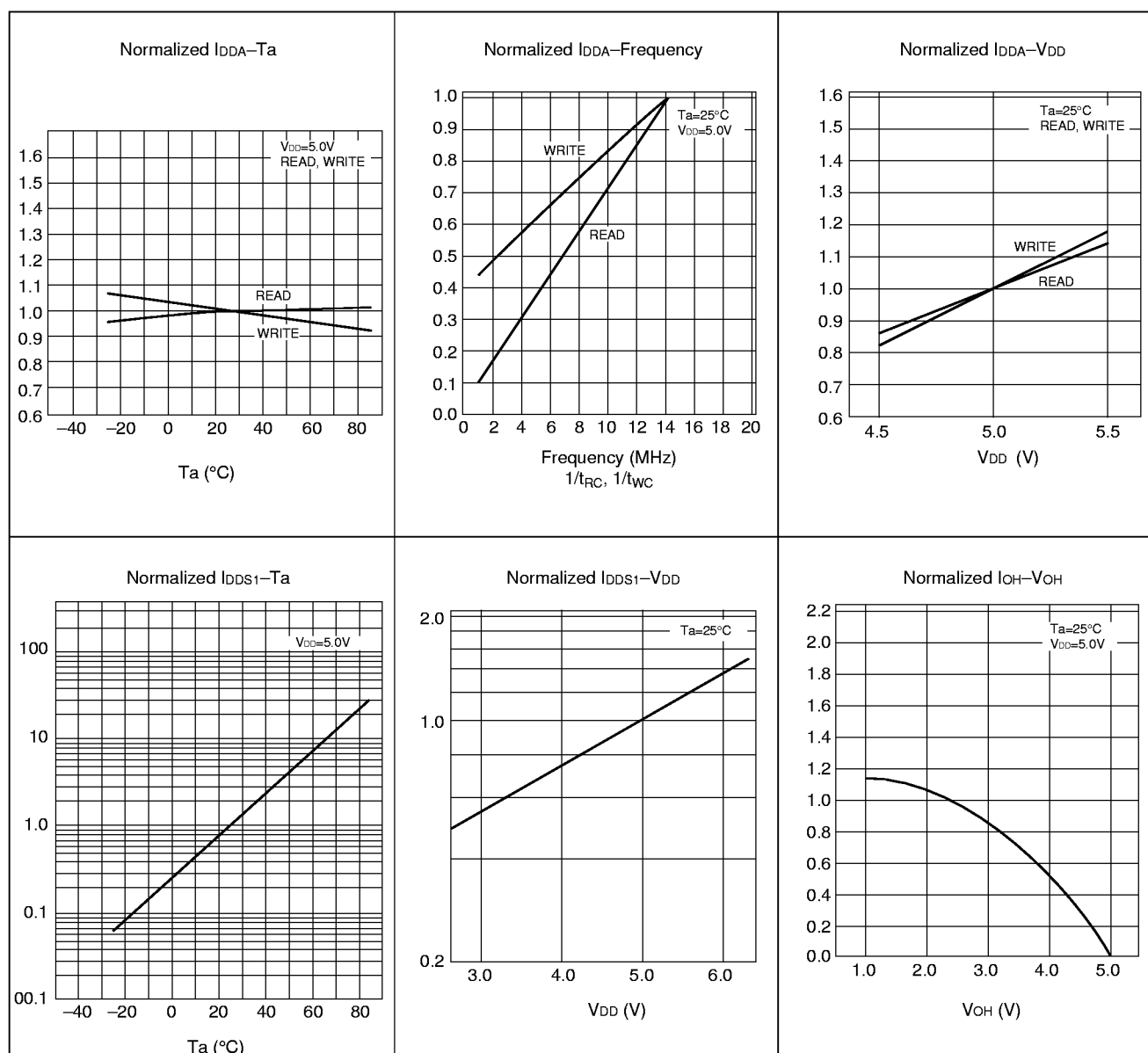
Plastic TSOP (I)-28pin-R1*



Unit : mm
(inch)

* : The same characteristics as SRM2A256LLMX70/85/10.

■ CHARACTERISTICS CURVES



SRM2A256LLMX70/85/10

