Contents

The S-2100R is a CMOS 64-bit serial FUSE ROM. It has a low standby current (0.3 μA max., V_{DD}=1.5 V) and has a wide operating voltage range. Data can be read serially by clock pulses from address 1 to address 64. All the addresses are initialized at "H" so writing into "L" can be done only once.

■ Features

- Low standby current (0.3 μA max., V_{DD}=1.5 V)
- Wide operating voltage range

■ Applications

- Pager ID ROM
- Cordless telephone
- Security equipment

■ Pin Assignment

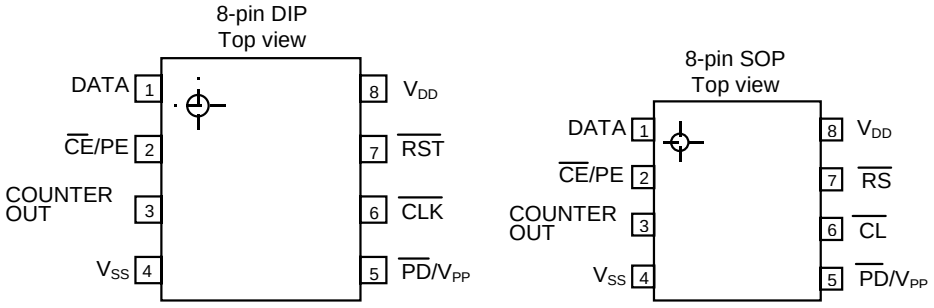


Figure 1

■ Block Diagram

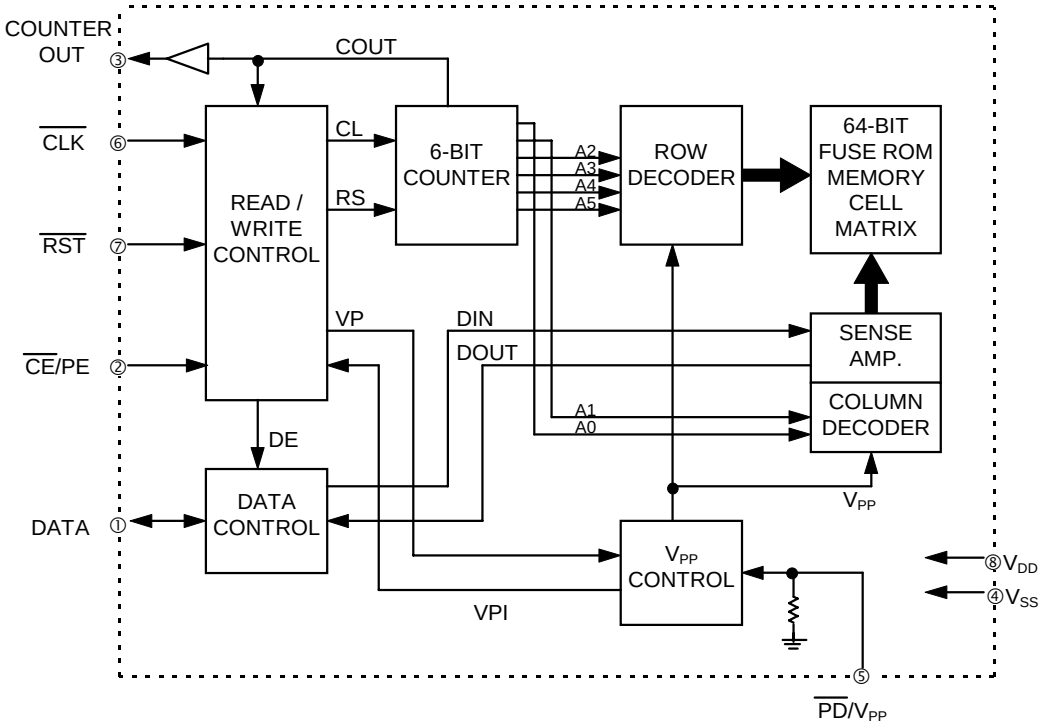


Figure 2

■ Terminal Description

Table 1

Pin No.	Symbol	Pin Name	Description
1	DATA	Data input/output terminal	Tri-state data input/output terminal
2	$\overline{CE}$/PE	Mode select terminal	Mode select terminal (Refer to operation mode table)
3	COUNTER OUT	Counter output terminal	6-bit counter; 64th bit detection output terminal
4	V_{SS}	Negative power supply terminal	Normally, connected to GND.
5	$\overline{P_D}/V_{PP}$	Program voltage input terminal	Input terminal of writing voltage to FUSE memory at 21 V. (Refer to operation mode table.) Pull-down resistor built in.
6	$\overline{CLK}$	Clock input terminal	Clock input terminal of 6-bit counter. Operates at the falling edge.
7	$\overline{RST}$	Reset input terminal	Reset input terminal of 6-bit counter. Operates at "L".
8	V_{DD}	Positive power supply terminal	Normally, connected to +1.1 to +5.5 V.

■ Mode Table

Table 2

Terminal / Read	$\overline{CE}$/PE	$\overline{P_D}/V_{PP}$	$\overline{CLK}$	$\overline{RST}$	DATA
Read	V_{SS}	V_{SS}	Input possible	Input possible	Data output
Counter hold	V_{DD}	V_{SS}	Input impossible	Input impossible	High impedance
Program	V_{DD}	V_{PP}	Input impossible	Input impossible	Data input

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to +6.5	V
P_D/V_{PP} input voltage	V_{PP}	-0.3 to 26	V
Input voltage	V_{IN}	V_{SS} -0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{SS} -0.3 to V_{DD}+0.3	V
Storage temperature under bias	V_{bias}	-30 to +85	°C
Storage temperature	V_{stg}	-40 to +125	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	Ta=25°C, Read, t_{CH}=15µs	1.1	1.5	5.5	V
		Ta=25°C, Write	4.5	5.0	5.5	V
High level input voltage	V_{IH}	Ta=25°C, Read	V_{DD}-0.3	—	V_{DD}	V
		Ta=25°C, Write	V_{DD}-0.3	—	V_{DD}	V
Low level input voltage	V_{IL}	Ta=25°C, Read	-0.3	—	0.3	V
		Ta=25°C, Write	-0.3	—	0.5	V
Operating temperature	V_{opr}		-20	—	70	°C

■ DC Electrical Characteristics

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current consumption	I_{DDO}	V_{DD}=1.5 V, f_{CLK}=50 kHz	—	—	20	μA
Standby current consumption	I_{DDS}	V_{DD}=1.5 V, $\overline{RST}$=V_{DD} $\overline{CLK}$=V_{DD}, $\overline{CE}$/PE=V_{SS}	—	—	0.3	μA
$\overline{P_D}$/V_{PP} input voltage	V_{PP}		20	21	22	V
$\overline{P_D}$/V_{PP} input current	I_{PP}		—	—	150	mA
Output current	I_{OH}	V_{DD}=1.1 to 5.5 V, V_{OH}=V_{DD}-0.3 V	-300	—	—	μA
	I_{OL}	V_{DD}=1.1 to 5.5 V, V_{OH}=0.3 V	300	—	—	μA
Pull-down resistance	R_D	V_{DD}=1.5 V	0.1	0.2	0.4	MΩ

■ AC Electrical Characteristics

1. Read mode

Table 6

(Ta=25°C, V_{DD}=1.5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{RST}$ hold time	t_{RH}	5.0	—	—	μs
Read cycle time	t_{RC}	2.0	—	—	μs
$\overline{CLK}$ hold time	t_{CH}	5.0	—	—	μs
Access time	t_{ACC}	—	—	5.0	μs
$\overline{CE}$/PE setup time	t_{CES}	2.0	—	—	μs
$\overline{RST}$ setup time	t_{RS}	5.0	—	—	μs
$\overline{CLK}$ setup time	t_{CS}	5.0	—	—	μs
$\overline{CE}$ access time	t_{CE}	—	—	5.0	μs
Output disable time	t_{WZ}	—	—	500	ns
$\overline{CLK}$ and $\overline{RST}$ inhibit time	t_{CRI}	—	—	500	ns

Load : 60 pF

2. Write mode

Table 7

(Ta=25°C, V_{DD}=5.0 V, V_{PP}=21 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CE-data setup time	t_{CDS}	0.5	—	—	μs
Data setup time	t_{DS}	0.5	—	—	μs
Data hold time	t_{DH}	0	—	—	μs
CE-data hold time	t_{CDH}	2.0	—	—	μs
V_{PP} rise time	t_r	20	—	—	μs
Program pulse width	t_{PW}	8.0	—	—	ms
V_{PP} rise slope	ΔV_{PP}	—	—	4	V/μs

■ Read Mode Operation

By setting the $\overline{CE}$/PE terminal to "L" level, the S-2100R enters the read mode. *1 Next, adding an $\overline{RST}$ pulse causes the contents of the memory bit of address 1 to be output at the DATA terminal; the rising of the $\overline{RST}$ pulse latches the data and stabilizes it. *2 Reading of addresses from 2 to 64 can be done by adding a $\overline{CLK}$ pulse sequentially after reading address 1. *3 As soon as address 64 has been read, the COUNTER OUT terminal outputs "H" level. When it finishes reading address 64, it does not accept any more $\overline{CLK}$ pulses and the counter does not operate. The data of address 64 is maintained till address 1 is read by the $\overline{RST}$ pulse.

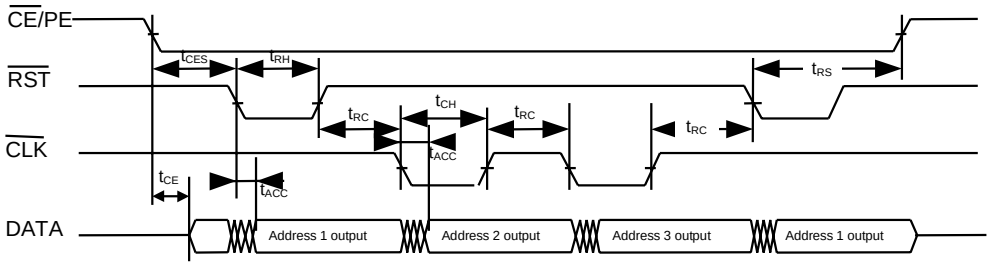


Figure 3 Read mode timing

*1 When both the $\overline{CLK}$ and $\overline{RST}$ terminals are at "H" level.
*2 When the $\overline{RST}$ terminal is at "L" level, the latch is transparent and the data is recognized by the rising of the $\overline{RST}$ pulse.
*3 Data read by the $\overline{CLK}$ pulse is latched at its rising.

■ Counter Hold Mode Operation

By setting the $\overline{CE}$/PE terminal to "H" level, the S-2100R enters the counter hold mode and the DATA terminal becomes high impedance. *4
In counter hold mode, the $\overline{CLK}$ and $\overline{RST}$ pulses which fall while the $\overline{CE}$/PE terminal is at "H" level are recognized to be invalid and there is no change in counter and data output. When the $\overline{CE}$/PE terminal is set to "L" level again, it returns to the condition in which it was before the counter hold mode.

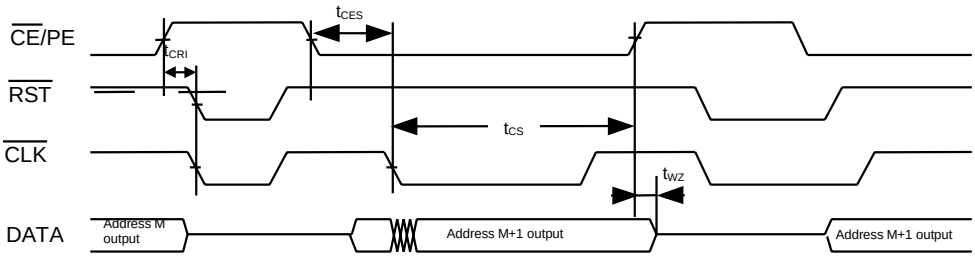


Figure 4 Counter hold mode timing

*4 When both the CLK and RST terminals are at "H" level.

■ Program Mode Operation

By setting the $\overline{CE}$/PE terminal to "H" level, the S-2100R enters the counter hold mode and at the same time enters the program mode. *5

Writing is done in program mode after selecting the address in read mode. *6 Select the address, and supply "H" level to the $\overline{CE}$/PE terminal and "L" level to the DATA terminal, with the writing pulse V_{PP} being supplied to the $\overline{P_D}/V_{PP}$ terminal. "L" level can be written into the selected address only once. *7 *8

If you coutinue writing from address 1 to 64, the output of the COUNTER OUT terminal goes to "H" level, just like in the read mode, and no more $\overline{CLK}$ pulses or writing pulses in program mode can be accepted.

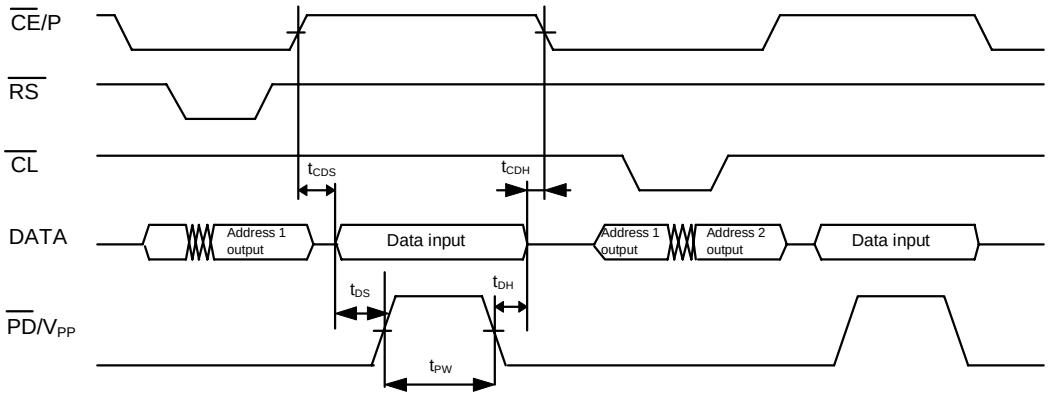


Figure 5 Program mode timing

*5 In program mode, operate at VDD=5.0 V to assure reliability of the data writing.

*6 The selection of addresses is possible only in read mode. Address 1 is selected by $\overline{RST}$ pulses and writing proceeds sequentially from address 1 by $\overline{CLK}$ pulse.

*7 All the memories are initially at "H" level, so writing into "L" can be done. When data is at "H" level, writing voltage cannot be supplied to the memory.

*8 Address 1 is selected again by the $\overline{RST}$ pulse. The addresses which are not written to "L" level are at "H" level, so writing "L" level in these addresses is possible.

■ Input Priority

In read mode, priority is given to either the $\overline{CLK}$ or $\overline{RST}$ terminal, whichever is entered first. Whichever pulse is input earlier is recognized to be valid from the rising till the end of the operation. If the pulse input later is at "L" level, the signal is ignored, even though the effective pulse input earlier rises. *9

If the $\overline{CLK}$ and $\overline{RST}$ pulses are input, the mode shifts from read mode to counter hold mode when both the $\overline{CLK}$ and the $\overline{RST}$ terminals go to "H" level. *10

If the $\overline{CLK}$ and $\overline{RST}$ pulses which are input in the counter hold mode are still at "L" level after setting the $\overline{CE}$/PE terminal to "L" level, these $\overline{CLK}$ and $\overline{RST}$ terminals are ignored. The mode shifts to read mode and data which is held before the shift is output at the DATA terminal. *11

In program mode, inputting the DATA terminal before the $\overline{CE}$/PE terminal goes to "H" level is prohibited. Also, charging the writing voltage from the P_D/V_{PP} terminal is prohibited when the $\overline{CE}$/PE terminal is at "L" level. In program mode, input to the DATA terminal muse be decided before charging the writing voltage. *12

*9 Input of the $\overline{CLK}$ and $\overline{RST}$ pulses is not recognized as valid unless both pulses are input at "H" level.

*10 The counter hold mode is entered when reading of the $\overline{CLK}$ and $\overline{RST}$ pulses has been finished and DATA output has been stabilized .

*11 No more $\overline{CLK}$ or $\overline{RST}$ pulses are accepted unless both the $\overline{CLK}$ and $\overline{RST}$ terminals are at "H" level.

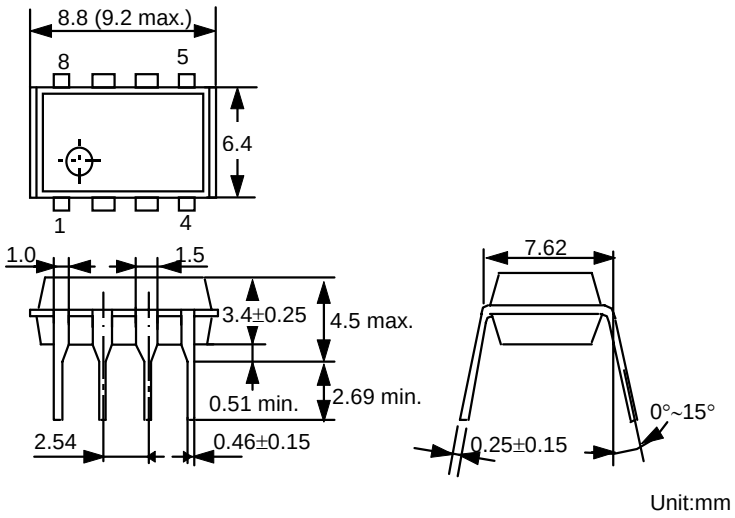
*12 If data input is changed while writing voltage is supplied, the S-2100R does not accept the changed data.

■ Notes

Memory should not be accessed for at least 10 μs after voltage is supplied and goes to V_{DD}.

■ Dimensions

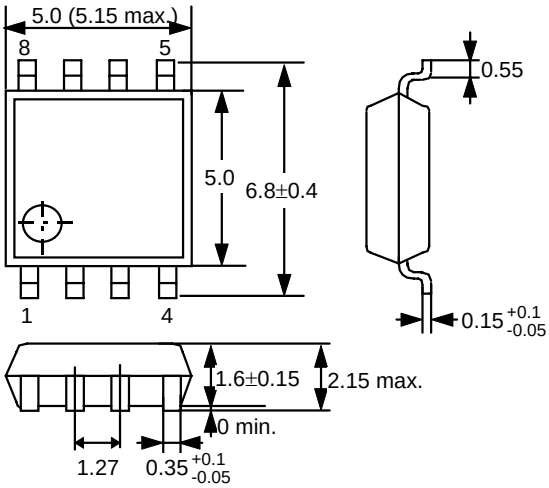
1. 8-pin DIP



Unit:mm

Figure 6

2. 8-pin SOP

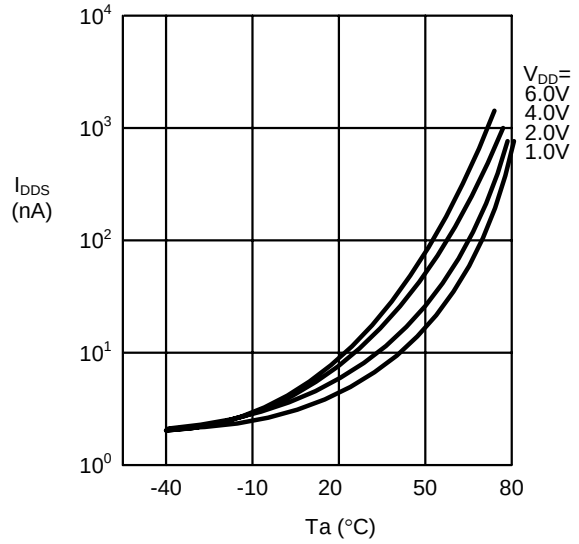


Unit: mm

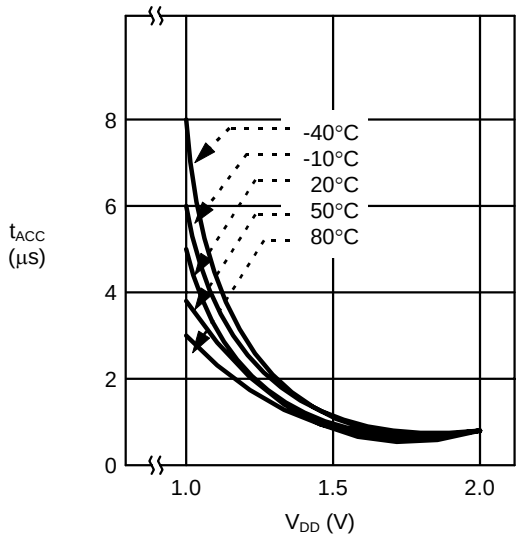
Figure 7

■ Characteristics

1. Standby current consumption I_{DDS}-
   Ambient temperature Ta



2. Access time t_{ACC}-
   Power supply voltage V_{DD}



3. Access time t_{ACC}-
   Power supply voltage V_{DD}