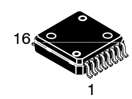
The RF Line
921 MHz - 960 MHz SiFET RF Integrated Power Amplifier

MHVIC910HR2

960 MHz, 10 W, 26 V
GSM CELLULAR
RF LDMOS INTEGRATED CIRCUIT



CASE 978-03
PFP-16

The MHVIC910HR2 integrated circuit is designed for GSM base stations, uses Motorola's newest High Voltage (26 Volts) LDMOS IC technology, and contains a three-stage amplifier. Target applications include macrocell (driver function) and microcell base stations (final stage). The device is in a PFP-16 Power Flat Pack package which gives excellent thermal performances through a solderable backside contact.

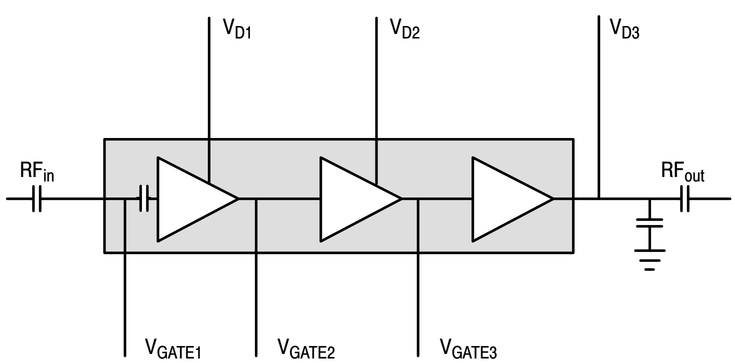
- Typical GSM Performance @ Full Frequency Band (921 - 960 MHz), 26 Volts
  Output Power - 40 dBm (CW) @ P1dB
  Power Gain - 39 dB @ P1dB
  Efficiency - 48% @ P1dB
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated ESD Protection
- Usable Frequency Range - 921 to 960 MHz
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	28	Vdc
Gate Supply Voltage	V_{GS}	6	Vdc
RF Input Power	P_{in}	5	dBm
Case Operating Temperature	T_C	- 30 to + 85	°C
Storage Temperature Range	T_{stg}	- 65 to + 150	°C
Operating Channel Temperature	T_{ch}	150	°C

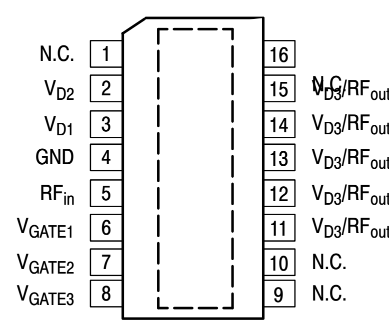
THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	°C/W



Functional Block Diagram

PIN CONNECTIONS



(Top View)
NOTE: Exposed backside flag is source terminal for transistors.

NOTE: MHVIC910HR2 Moisture Sensitivity Level (MSL) = 3.

For More Information On This Product, Go to: www.freescale.com

ESD PROTECTION CHARACTERISTICS

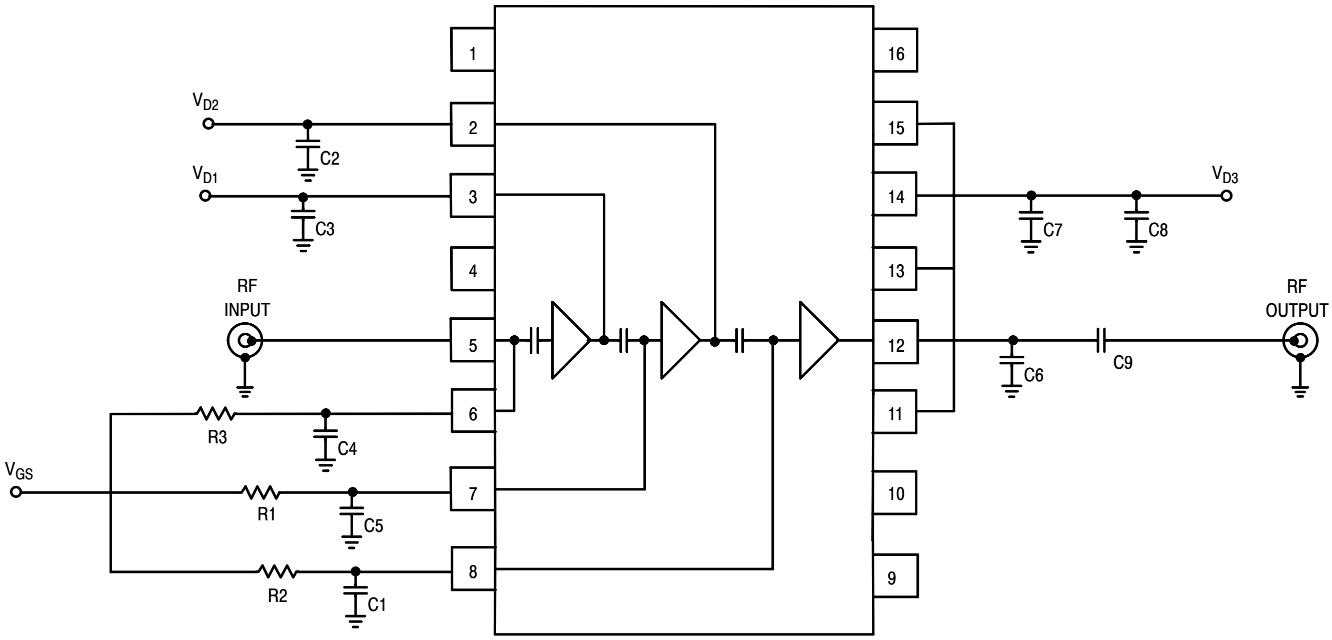
Test Conditions	Class
Human Body Model	0 (Minimum)
Machine Model	M2 (Minimum)

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	26	Vdc
3rd Stage Quiescent Current	I_{DQ3}	150	mA
2nd Stage Quiescent Current	I_{DQ2}	50	mA
1st Stage Quiescent Current	I_{DQ1}	25	mA

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 V, V_{GS} set for I_{DQ3} = 150 mA, T_A = 25°C matched to a 50 Ω system, frequency range 921 - 960 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	f_{RF}	921	—	960	MHz
Output Power @ 1 dB Compression Point	P @ 1dB	39	40	—	dBm
Power Gain @ P1dB	G @ 1dB	38	39	—	dB
Power Added Efficiency @ 1 dB Compression Point	PAE @ 1dB	43	48	—	%
Input Return Loss @ P1dB	IRL @ 1dB	—	-15	-10	dB
Gain Flatness @ 40 dBm Variation (T_C = -30 to +85°C @ 40 dBm)	G_F G_V	— —	.5 5	— —	dB dB
Load Stability (V_{DS} = 24 V to 28 V, P_{out} = P1dB Down to 0 dBm, All Phase Angles)	VSWR	10:1	—	—	—
Ruggedness (V_{DS} = 26 V, P_{out} = 42 dBm, Load VSWR = 10:1, All Phase Angles)	Ψ	No Damage After Test			



C1, C2, C3, C4, C5, C8	1 μF Surface Mount Chip Capacitors	J1, J2	Header (Break-away), HDR2X10STIMCSAFU
C6	4.7 pF AVX Chip Capacitor, ACCU-P (08051J4R7BBT)	J3, J4	SMA Connector 2052-1618-02 (Threaded)
C7	47 pF AVX Chip Capacitor, ACCU-P (08055K470JBTTR)	R1, R2, R3	100 Ω Chip Resistors (0402)
C9	33 pF AVX Chip Capacitor, ACCU-P (08053J330JBT)	PCB	Rogers 04350, 20 mils

Figure 1. 921-960 MHz Demo Board Schematic

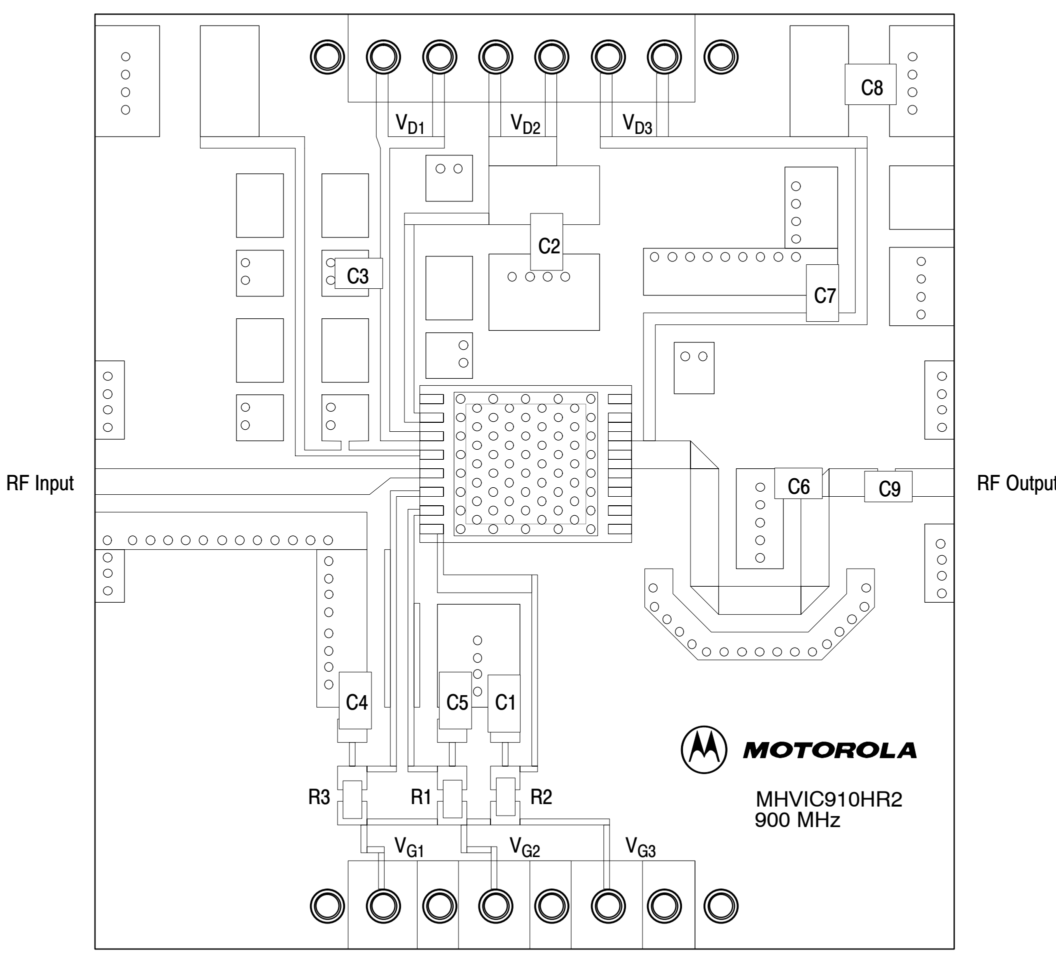


Figure 2. 921-960 MHz Demo Board Component Layout

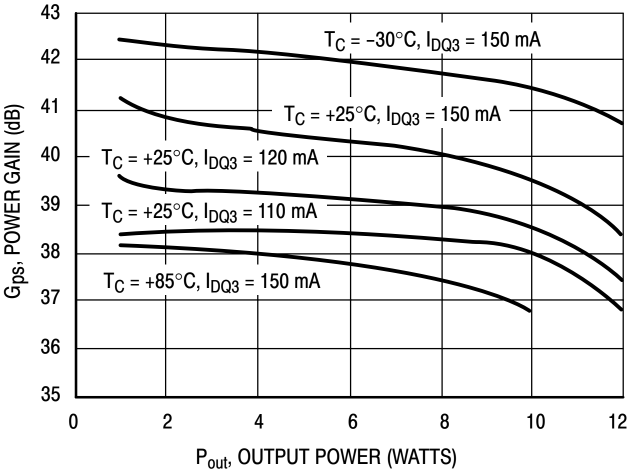


Figure 3. Power Gain versus Output Power

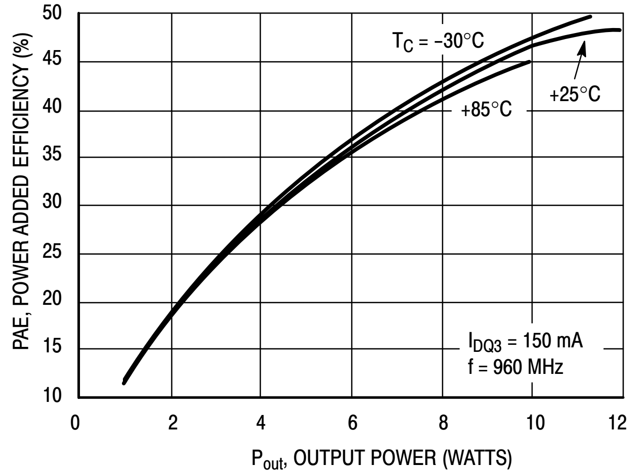


Figure 4. Power Added Efficiency versus Output Power

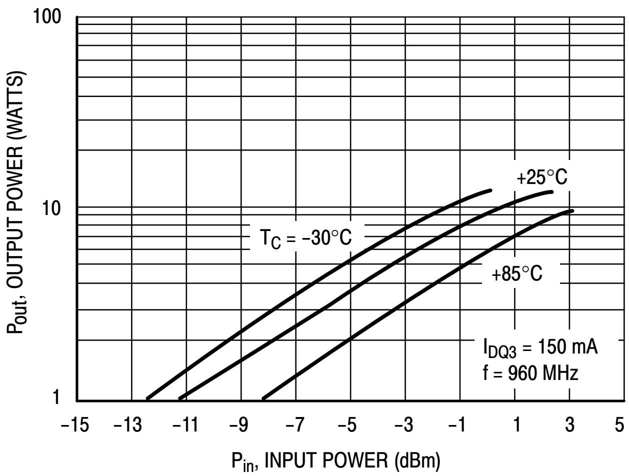


Figure 5. Output Power versus Input Power

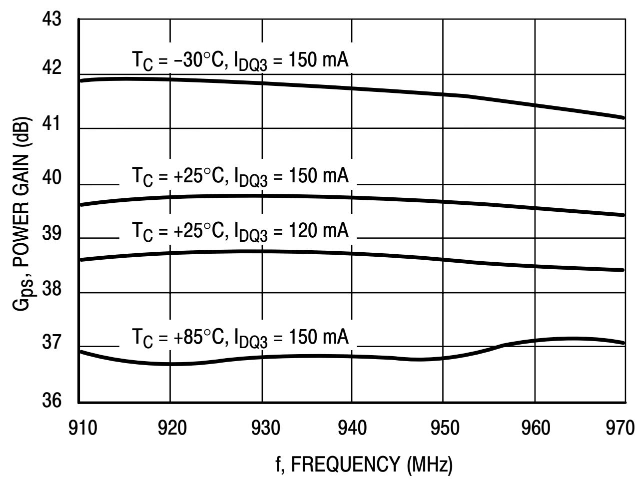


Figure 6. Power Gain versus Frequency
P_{out} = 10 W

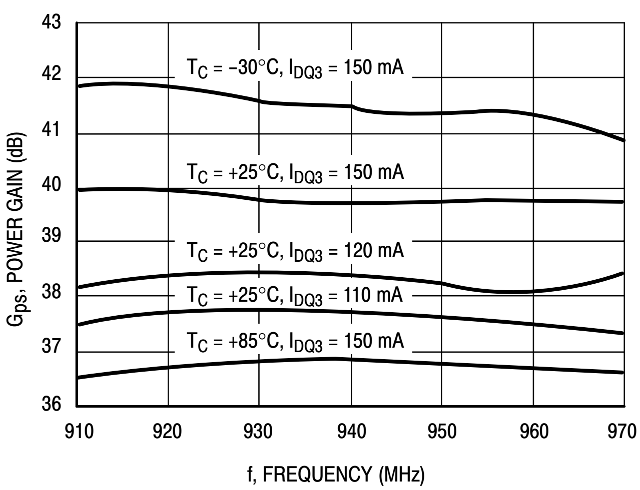


Figure 7. Power Gain versus Frequency
P_{out} = P1dB

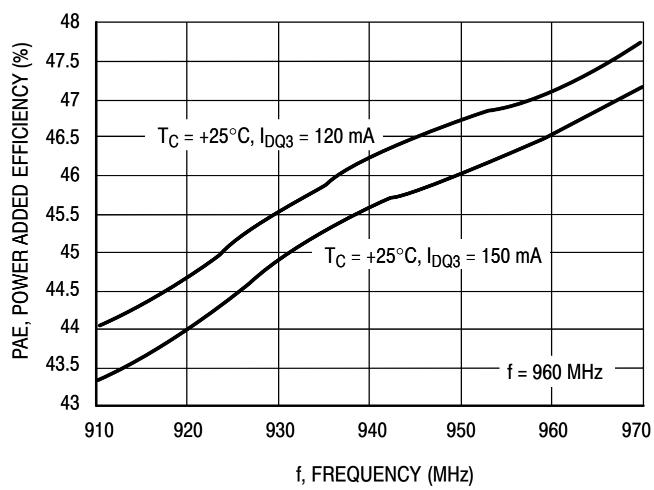


Figure 8. Power Added Efficiency versus Frequency
P_{out} = 10 W

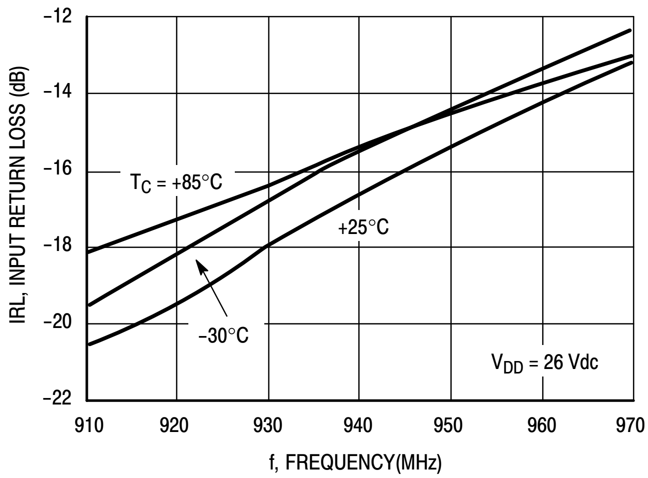


Figure 9. Input Return Loss versus Frequency P_{out} = 10 W

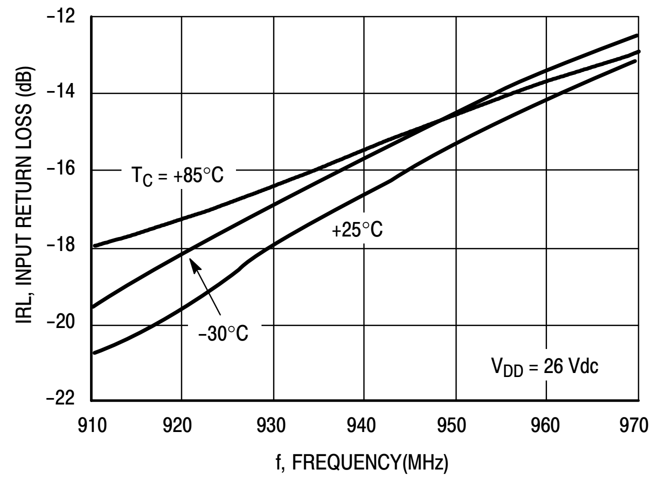


Figure 10. Input Return Loss versus Frequency P_{out} = P1dB

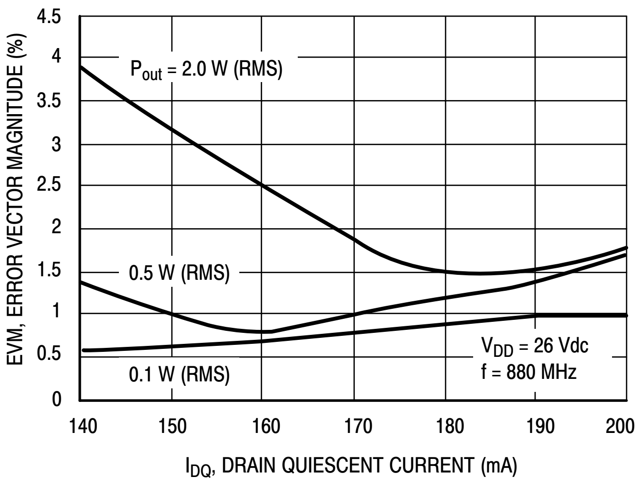


Figure 11. Error Vector Magnitude versus I_{DQ} Total

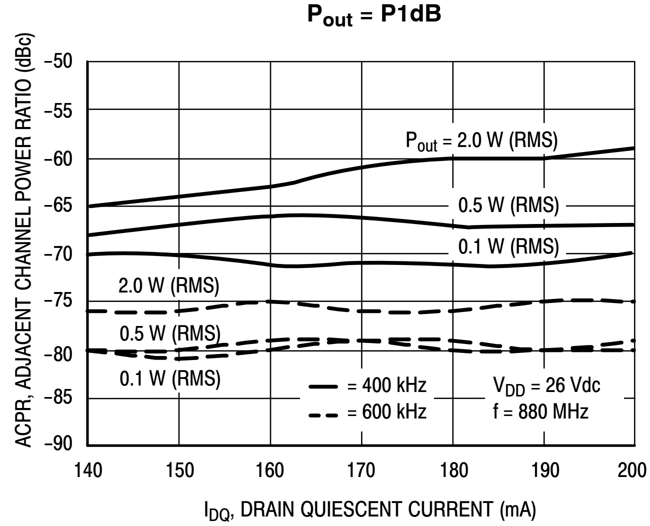


Figure 12. Adjacent Channel Power Ratio versus I_{DQ} Total

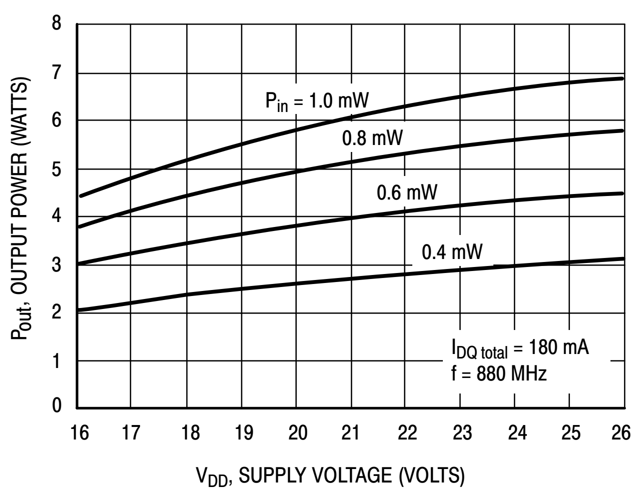


Figure 13. Output Power versus Supply Voltage

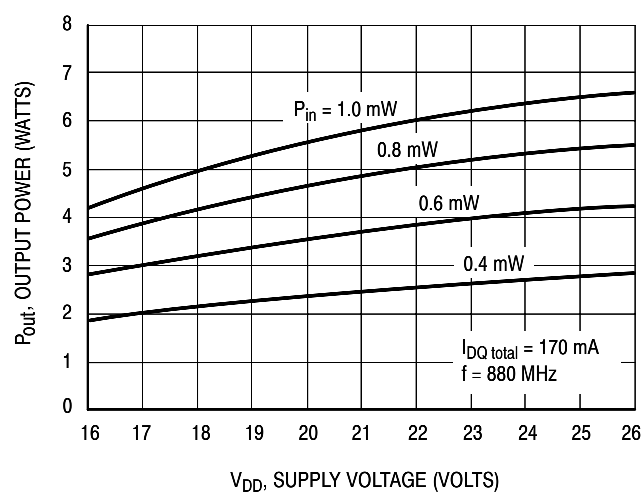


Figure 14. Output Power versus Supply Voltage

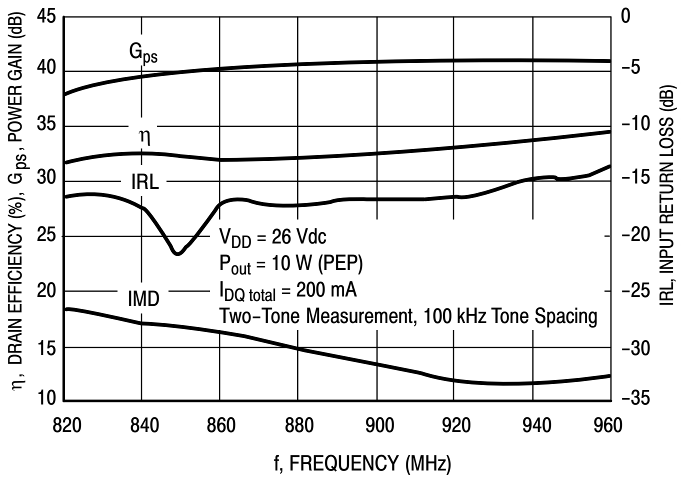


Figure 15. Two-Tone Broadband Performance

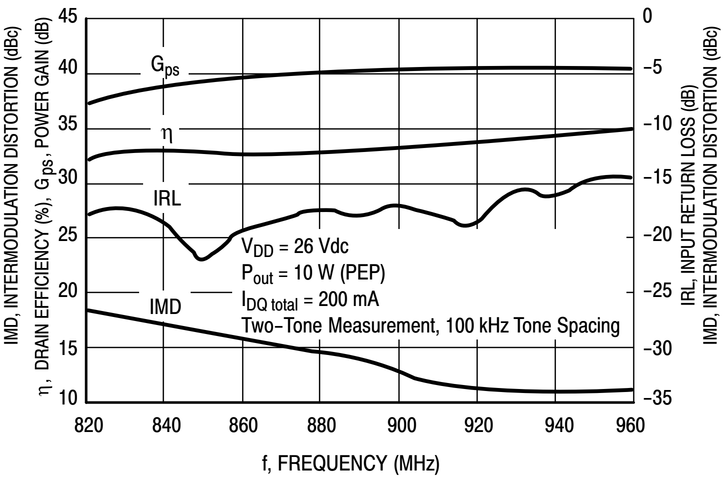


Figure 16. Two-Tone Broadband Performance

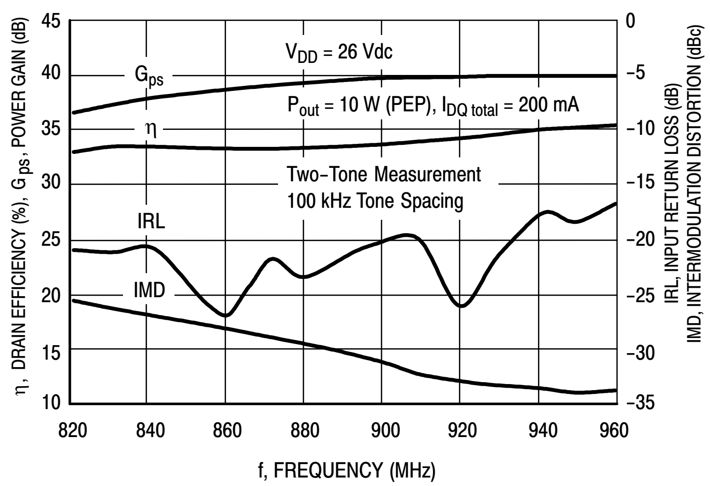


Figure 17. Two-Tone Broadband Performance

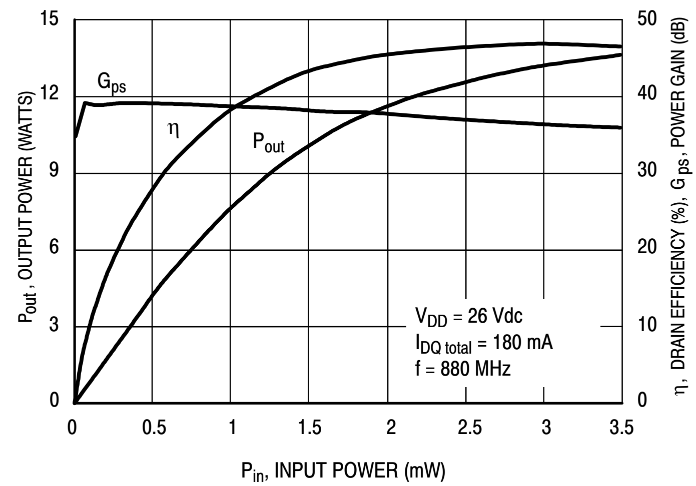


Figure 18. CW Performance @ 880 MHz

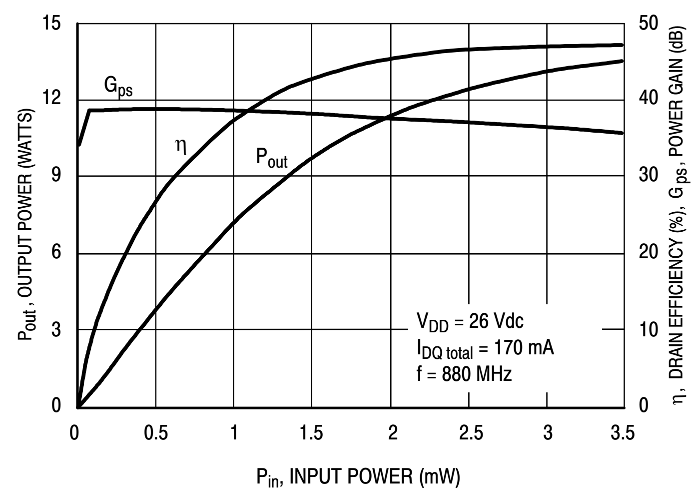


Figure 19. CW Performance @ 880 MHz

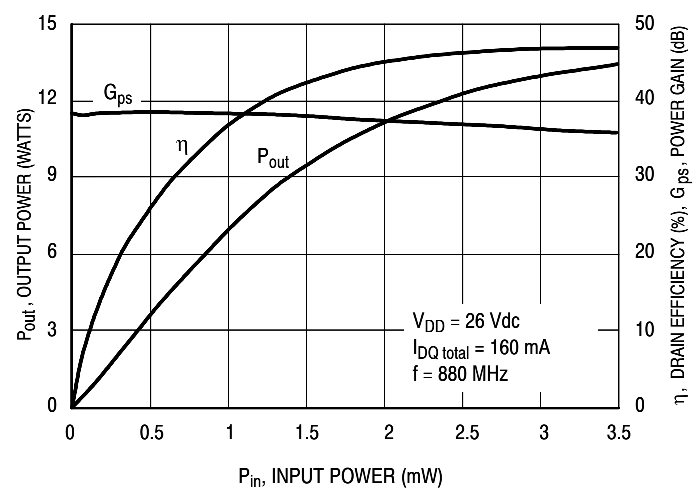


Figure 20. CW Performance @ 880 MHz

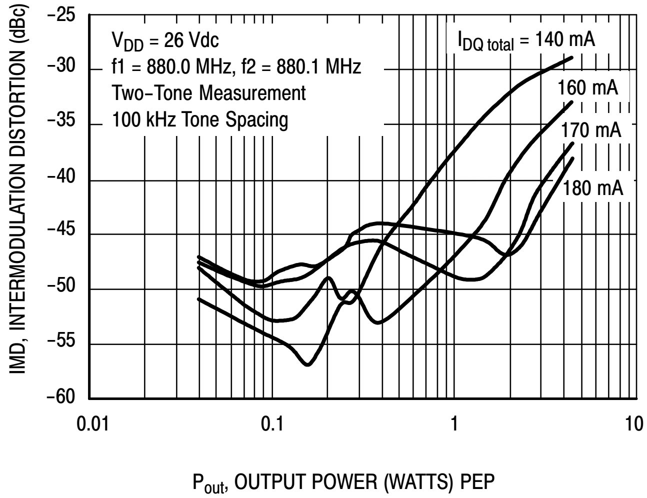
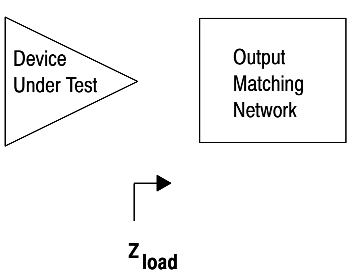


Figure 21. Intermodulation Distortion versus Output Power

V_{DD} = 26 V, I_{DQ} = 225 mA, P_{out} = 40 dBm

f MHz	Z_{load} Ω
900	7.81 + j4.61
920	7.27 + j4.90
940	6.77 + j5.23
960	6.31 + j5.59
980	5.90 + j5.96
1000	5.53 + j6.36

Z_{load} = Test circuit impedance as measured from drain to ground.



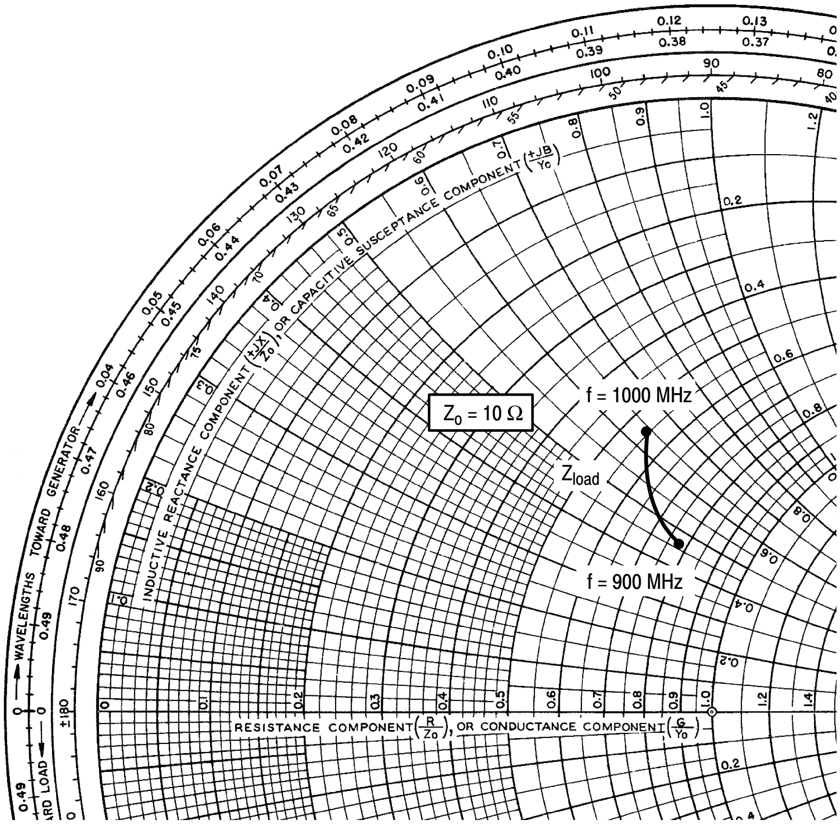
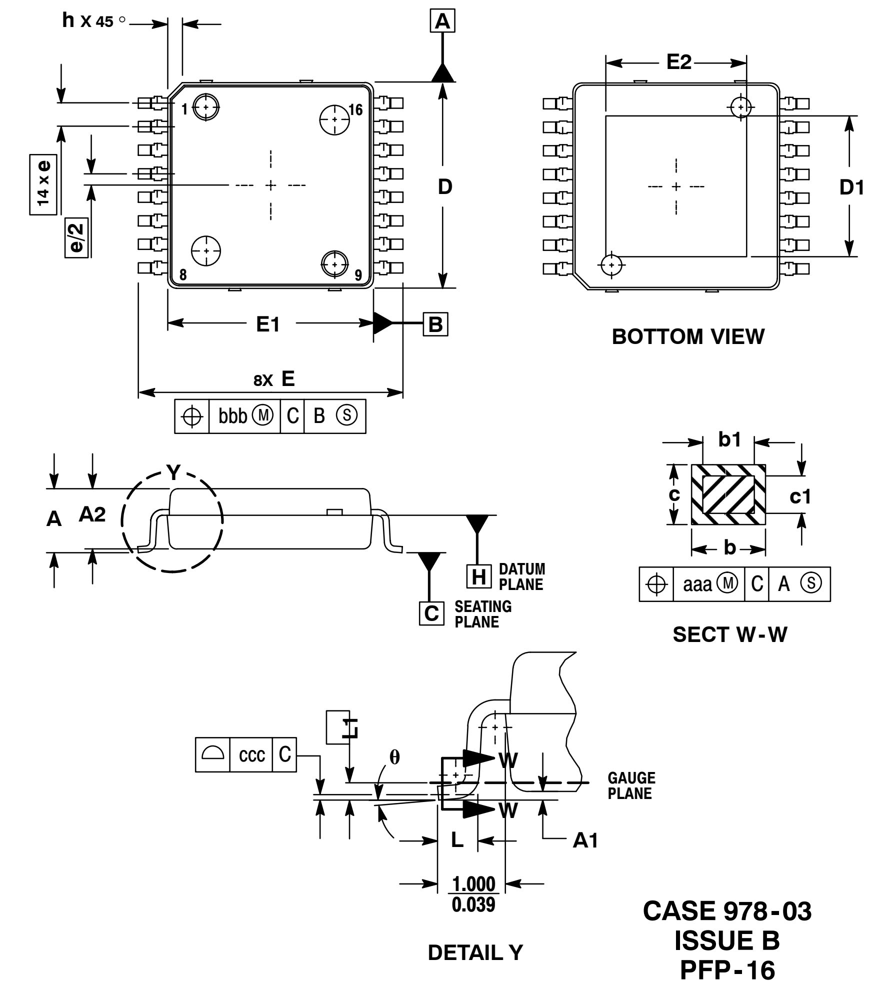


Figure 22. Series Equivalent Load Impedance

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978-03
ISSUE B
PFP-16

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81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
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