



74LVC573A

OCTAL D-TYPE LATCH HIGH PERFORMANCE

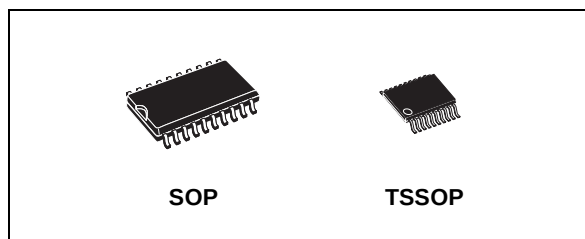
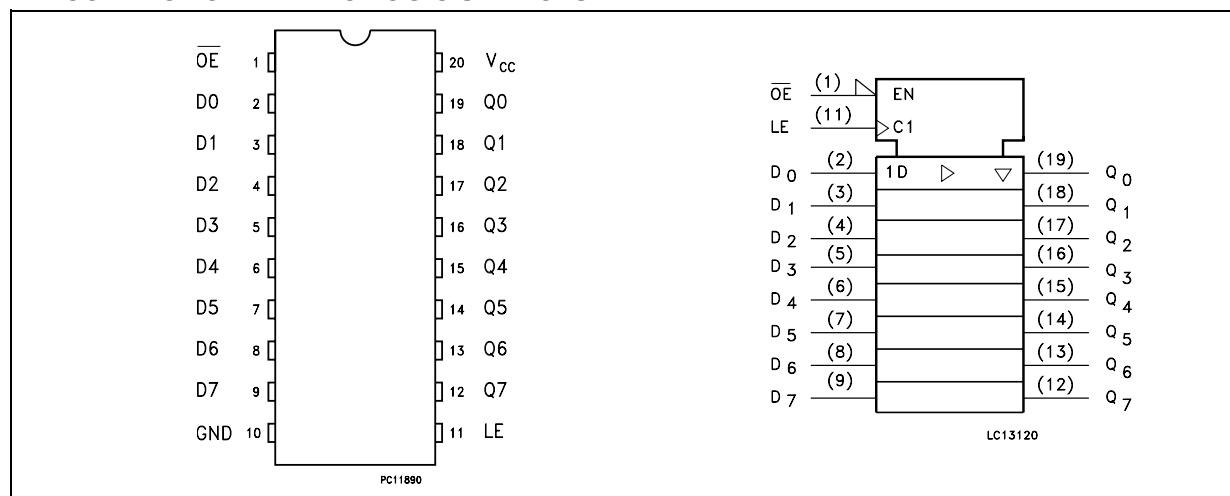
- 5V TOLERANT INPUTS
- HIGH SPEED: $t_{PD} = 6.8ns$ (MAX.) at $V_{CC} = 3V$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24mA$ (MIN) at $V_{CC} = 3V$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 1.65V$ to $3.6V$ (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 573
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
HBM > 2000V (MIL STD 883 method 3015);
MM > 200V

DESCRIPTION

The 74LVC573A is a low voltage CMOS OCTAL D-TYPE LATCH fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for 1.65 to 3.6 V_{CC} operations and low power and low noise applications.

These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). While the LE inputs is held at a high level, the Q

PIN CONNECTION AND IEC LOGIC SYMBOLS



ORDER CODES

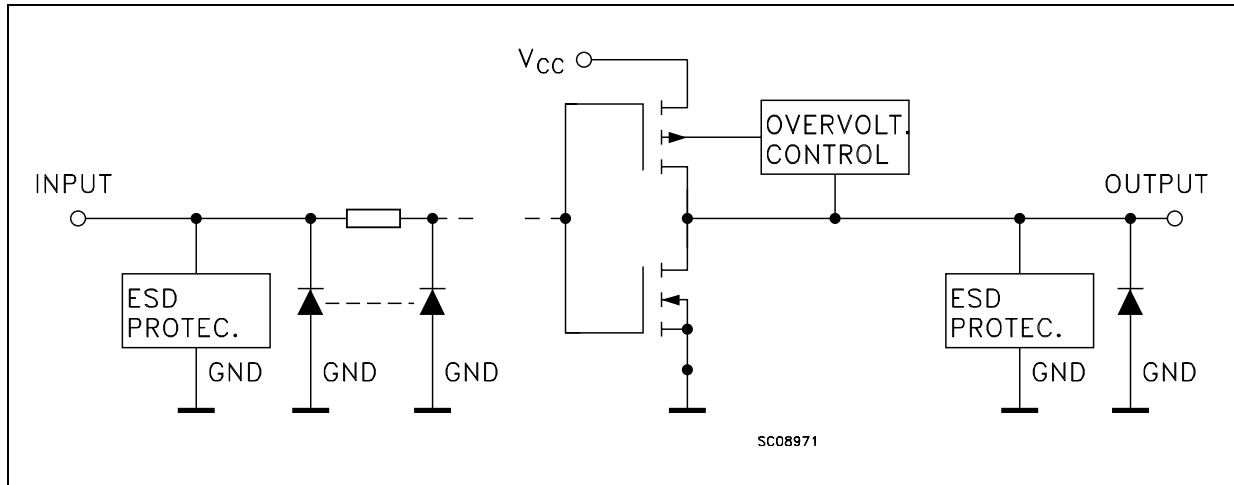
PACKAGE	TUBE	T & R
SOP	74LVC573AM	74LVC573AMTR
TSSOP		74LVC573ATTR

outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the ($\overline{OE}$) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

This device is designed to interface directly High Speed CMOS systems with TTL and NMOS components. It has more speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	OE	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUT
$\overline{\text{OE}}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage (V _{CC} = 0V)	-0.5 to +7.0	V
V _O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 50	mA
I _{OK}	DC Output Diode Current (note 2)	- 50	mA
I _O	DC Output Current	± 50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current per Supply Pin	± 100	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

1) I_O absolute maximum rating must be observed

2) V_O < GND

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	1.65 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage ($V_{CC} = 0V$)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 3.0$ to $3.6V$)	± 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 2.7$ to $3.0V$)	± 12	mA
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 2.3$ to $2.7V$)	± 8	mA
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 1.65$ to $2.3V$)	± 4	mA
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2V at $V_{CC} = 3.0V$

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value				Unit
		V _{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	1.65 to 1.95		0.65V _{CC}		0.65V _{CC}		V
		2.3 to 2.7		1.7		1.7		
		2.7 to 3.6		2		2		
V _{IL}	Low Level Input Voltage	1.65 to 1.95			0.35V _{CC}		0.35V _{CC}	V
		2.3 to 2.7			0.7		0.7	
		2.7 to 3.6			0.8		0.8	
V _{OH}	High Level Output Voltage	1.65 to 3.6	I _O =-100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		1.65	I _O =-4 mA	1.2		1.2		
		2.3	I _O =-8 mA	1.7		1.7		
		2.7	I _O =-12 mA	2.2		2.2		
		3.0	I _O =-18 mA	2.4		2.4		
		3.0	I _O =-24 mA	2.2		2.2		
V _{OL}	Low Level Output Voltage	1.65 to 3.6	I _O =100 μA		0.2		0.2	V
		1.65	I _O =4 mA		0.45		0.45	
		2.3	I _O =8 mA		0.7		0.7	
		2.7	I _O =12 mA		0.4		0.4	
		3.0	I _O =24 mA		0.55		0.55	
I _I	Input Leakage Current	3.6	V _I = 0 to 5.5V		± 5		± 5	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 5.5V		10		10	μA
I _{OZ}	High Impedance Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = 0 to 5.5V		± 5		± 5	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND		10		10	μA
			V _I or V _O = 3.6 to 5.5V		± 10		± 10	
ΔI _{CC}	I _{CC} incr. per Input	2.7 to 3.6	V _{IH} = V _{CC} -0.6V		500		500	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
V _{OLP}	Dynamic Low Level Quiet Output (note 1)	3.3	C _L = 50pF V _{IL} = 0V, V _{IH} = 3.3V		0.8		V
V _{OLV}					-0.8		

1) Number of output defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition				Value				Unit
		V _{CC} (V)	C _L (pF)	R _L (Ω)	t _s = t _r (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time D to Q	1.65 to 1.95	30	1000	2.0		TBD		TBD	ns
		2.3 to 2.7	30	500	2.0		TBD		TBD	
		2.7	50	500	2.5	1.5	7.8	1.5	9.4	
		3.0 to 3.6	50	500	2.5	1	6.8	1	8.2	
t _{PLH} t _{PHL}	Propagation Delay Time LE to Q	1.65 to 1.95	30	1000	2.0		TBD		TBD	ns
		2.3 to 2.7	30	500	2.0		TBD		TBD	
		2.7	50	500	2.5	1.5	7.8	1.5	9.4	
		3.0 to 3.6	50	500	2.5	1	6.8	1	8.2	
t _{PZL} t _{PZH}	Output Enable Time	1.65 to 1.95	30	1000	2.0		TBD		TBD	ns
		2.3 to 2.7	30	500	2.0		TBD		TBD	
		2.7	50	500	2.5	1	8.7	1	10.4	
		3.0 to 3.6	50	500	2.5	1	7.7	1	9.2	
t _{PLZ} t _{PHZ}	Output Disable Time	1.65 to 1.95	30	1000	2.0		TBD		TBD	ns
		2.3 to 2.7	30	500	2.0		TBD		TBD	
		2.7	50	500	2.5	2	7.6	2	9.1	
		3.0 to 3.6	50	500	2.5	2	7.0	2	8.4	
t _w	LE Pulse Width HIGH	1.65 to 1.95	30	1000	2.0	TBD		TBD		ns
		2.3 to 2.7	30	500	2.0	TBD		TBD		
		2.7	50	500	2.5	3.3		3.3		
		3.0 to 3.6	50	500	2.5	3.3		3.3		
t _s	Setup Time D to LE, (HIGH to LOW)	1.65 to 1.95	30	1000	2.0	TBD		TDB		ns
		2.3 to 2.7	30	500	2.0	TBD		TBD		
		2.7	50	500	2.5	2		2		
		3.0 to 3.6	50	500	2.5	2		2		
t _h	Hold Time LE (HIGH to LOW) to D	1.65 to 1.95	30	1000	2.0	TBD		TBD		ns
		2.3 to 2.7	30	500	2.0	TBD		TBD		
		2.7	50	500	2.5	1.5		1.5		
		3.0 to 3.6	50	500	2.5	1.5		1.5		
t _{OSLH} t _{OSHL}	Output To Output Skew Time (note1, 2)	2.7 to 3.6					1		1	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|)

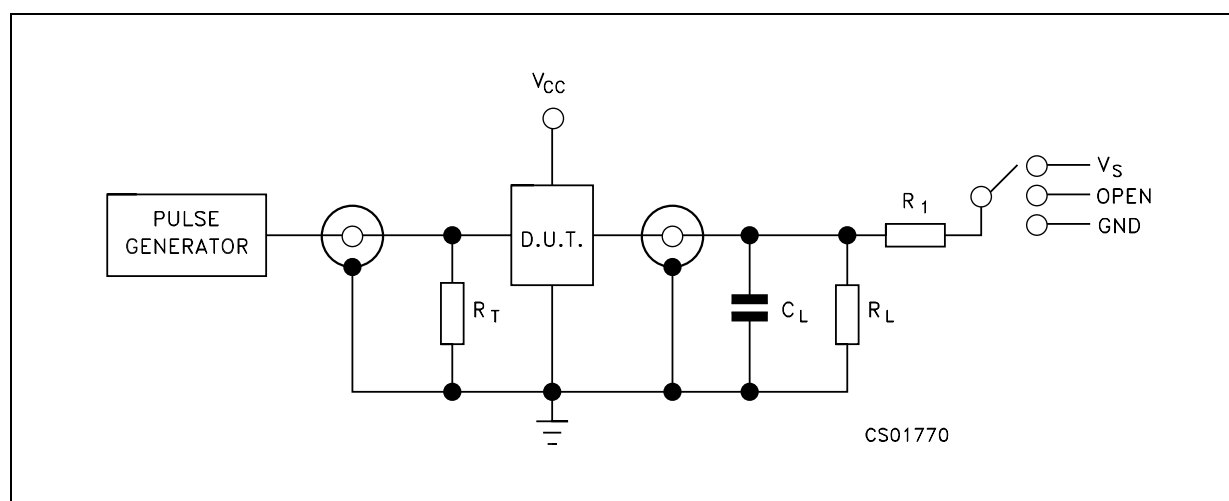
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance				4		pF
C _{PD}	Power Dissipation Capacitance (note 1)	1.8	f _{IN} = 10MHz		28		pF
		2.5			30		
		3.3			34		

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/n (per circuit)

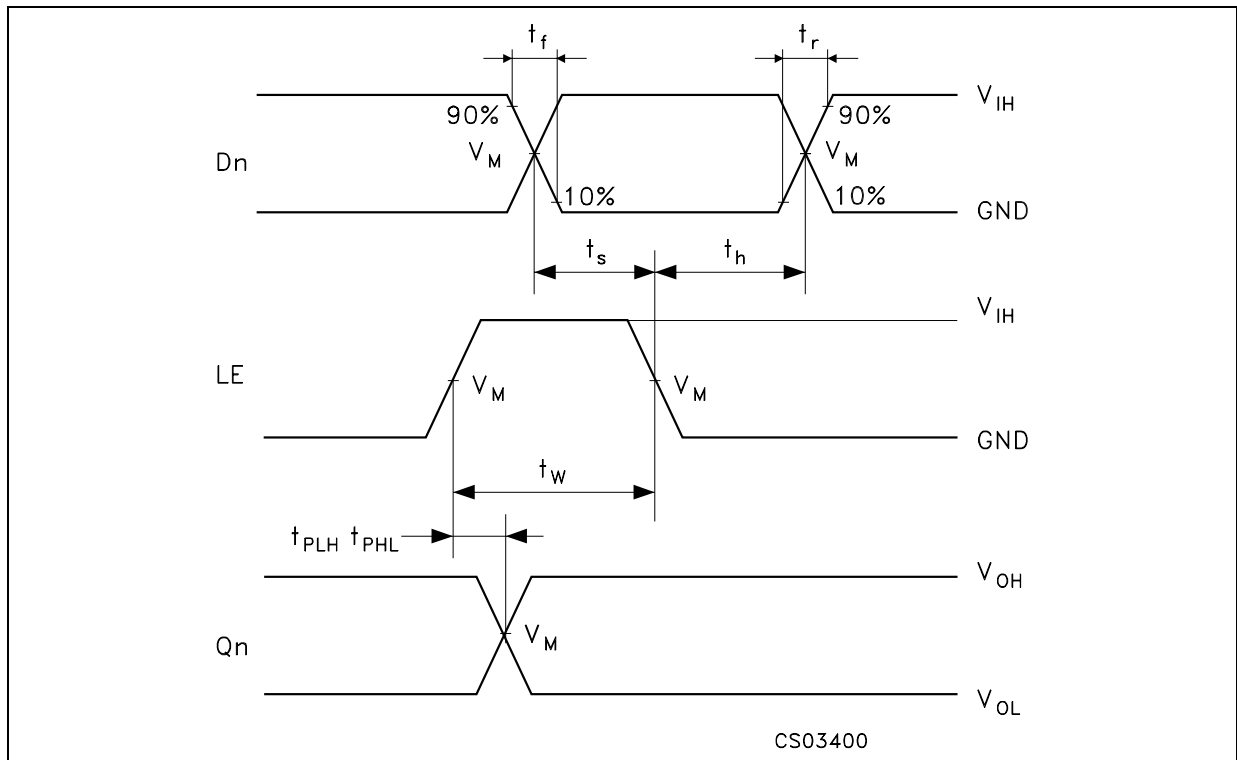
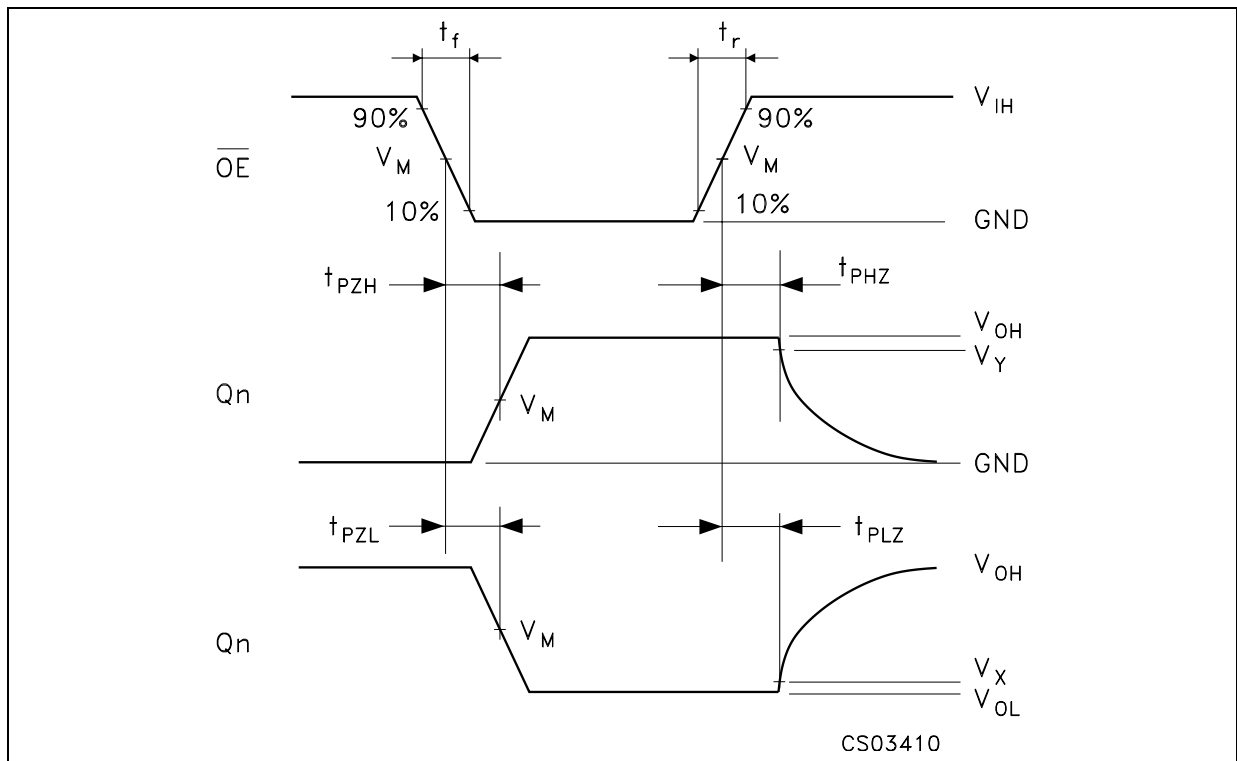
TEST CIRCUIT

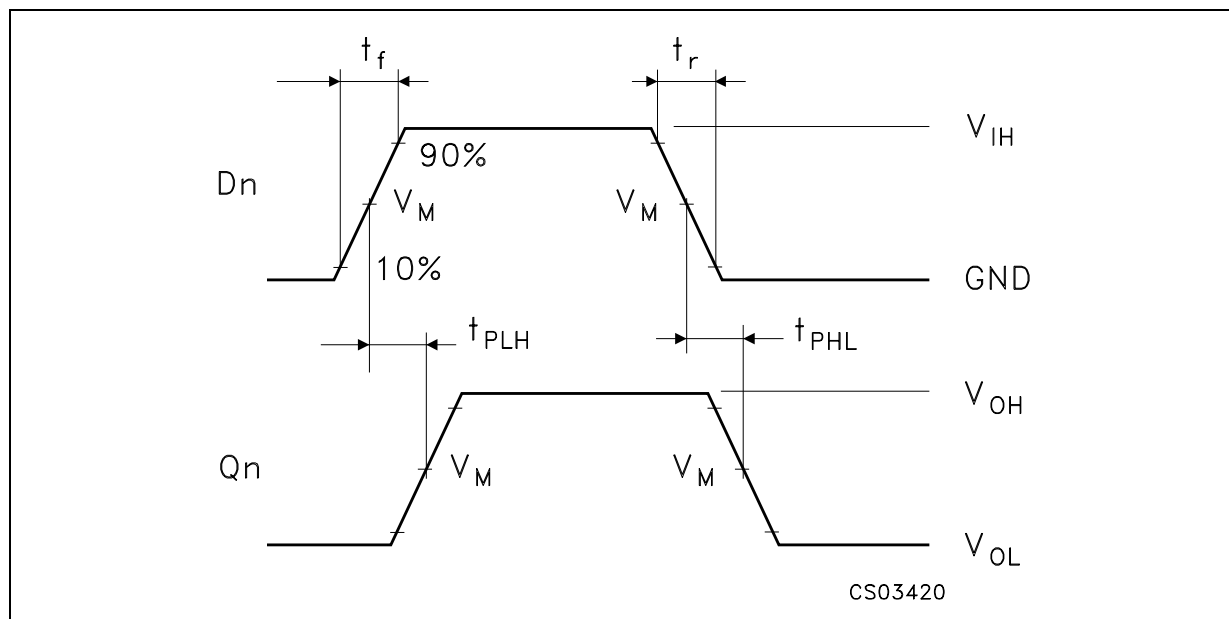


R_T = Z_{OUT} of pulse generator (typically 50Ω)

TEST CIRCUIT AND WAVEFORM SYMBOL VALUE

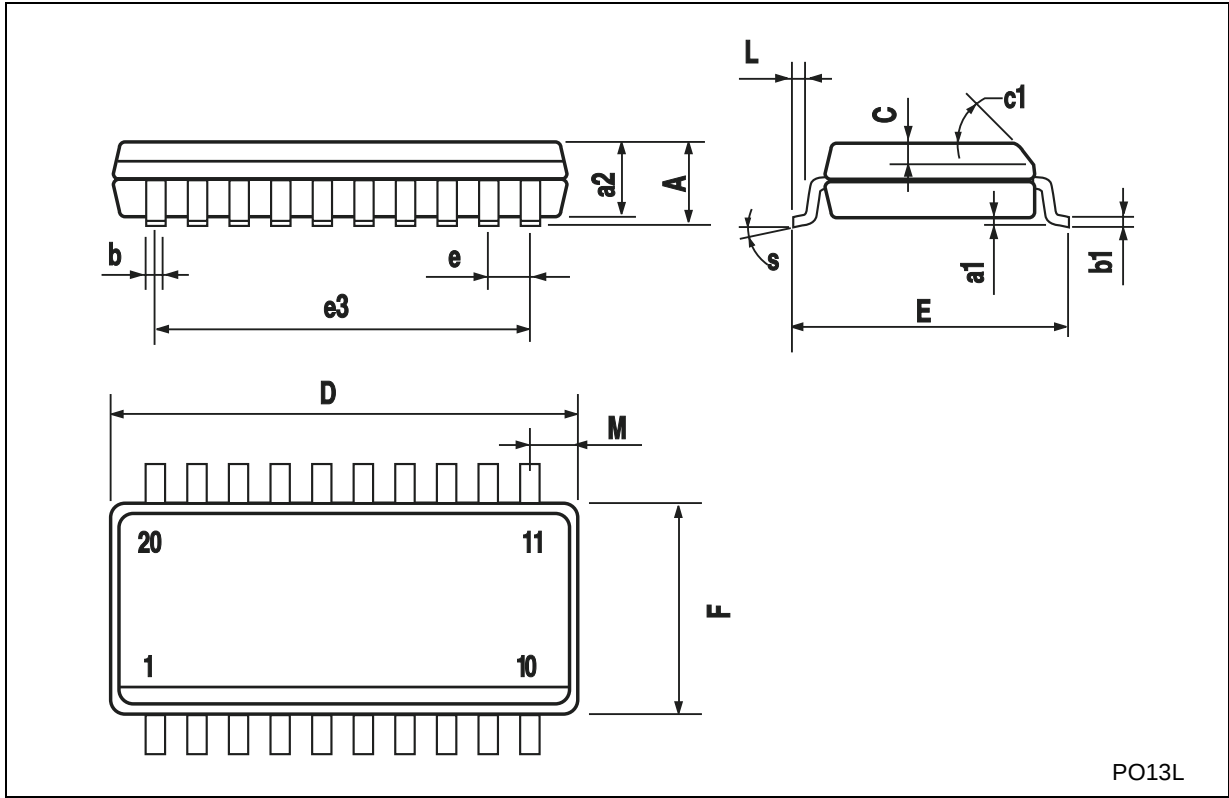
Symbol	V _{CC}			
	1.65 to 1.95V	2.3 to 2.7V	2.7V	3.0 to 3.6V
C _L	30pF	30pF	50pF	50pF
R _L = R ₁	1000Ω	500Ω	500Ω	500Ω
V _S	2 × V _{CC}	2 × V _{CC}	6V	7V
V _{IH}	V _{CC}	V _{CC}	2.7V	3.0V
V _M	V _{CC} /2	V _{CC} /2	1.5V	1.5V
V _{OH}	V _{CC}	V _{CC}	3.0V	3.5V
V _X	V _{OL} + 0.15V	V _{OL} + 0.15V	V _{OL} + 0.3V	V _{OL} + 0.3V
V _Y	V _{OH} - 0.15V	V _{OH} - 0.15V	V _{OH} - 0.3V	V _{OH} - 0.3V
t _r = t _f	<2.0ns	<2.0ns	<2.5ns	<2.5ns

WAVEFORM 1: PROPAGATION DELAY, SETUP AND HOLD TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES** ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 3: PROPAGATION DELAY TIME ($f=1\text{MHz}$; 50% duty cycle)

SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

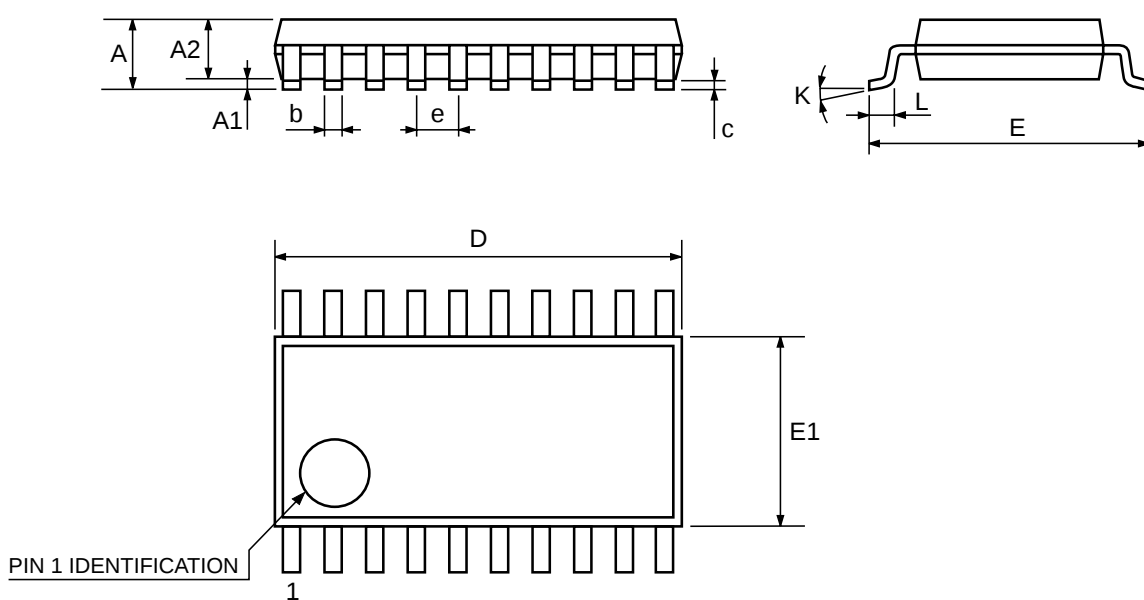


PO13L



TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0087225C

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>