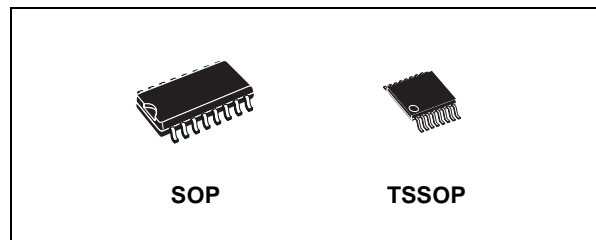




# 74VHCT174A

## HEX D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:  
 $f_{MAX} = 150 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:  
 $V_{IH} = 2\text{V (MIN.)}, V_{IL} = 0.8\text{V (MAX)}$
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC(OPR)} = 4.5\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 174
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE:  $V_{OLP} = 0.8\text{V (MAX.)}$



### ORDER CODES

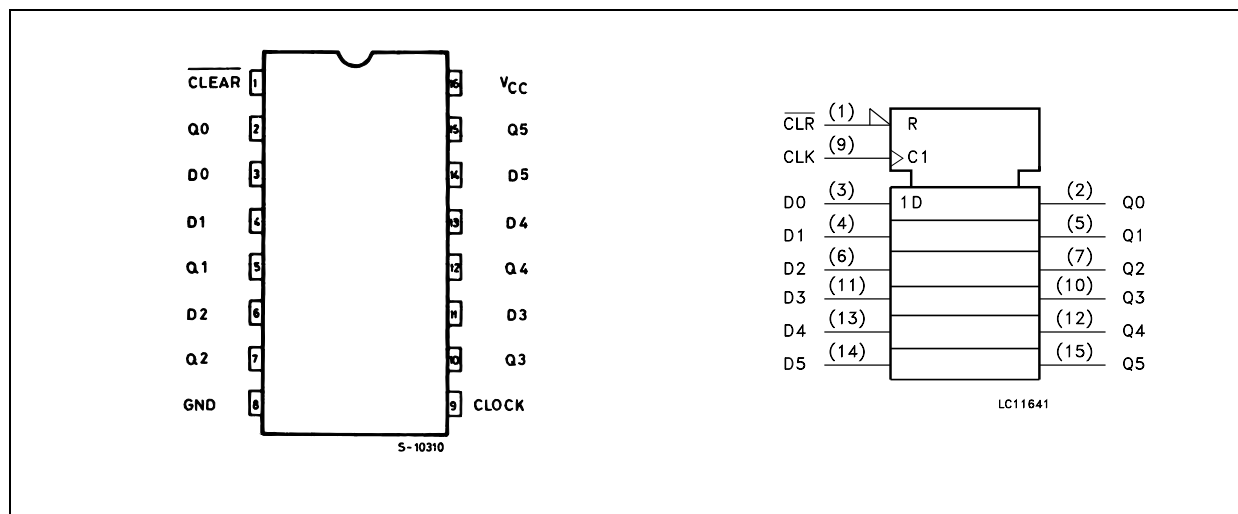
PACKAGE	TUBE	T & R
SOP	74VHCT174AM	74VHCT174AMTR
TSSOP		74VHCT174ATTR

When the  $\overline{\text{CLEAR}}$  input is held low, the Q outputs are held low independently of the other inputs. Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V since all inputs are equipped with TTL threshold. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

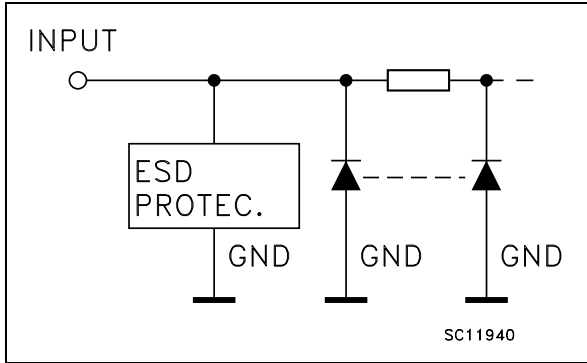
### DESCRIPTION

The 74VHCT174A is an advanced high-speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

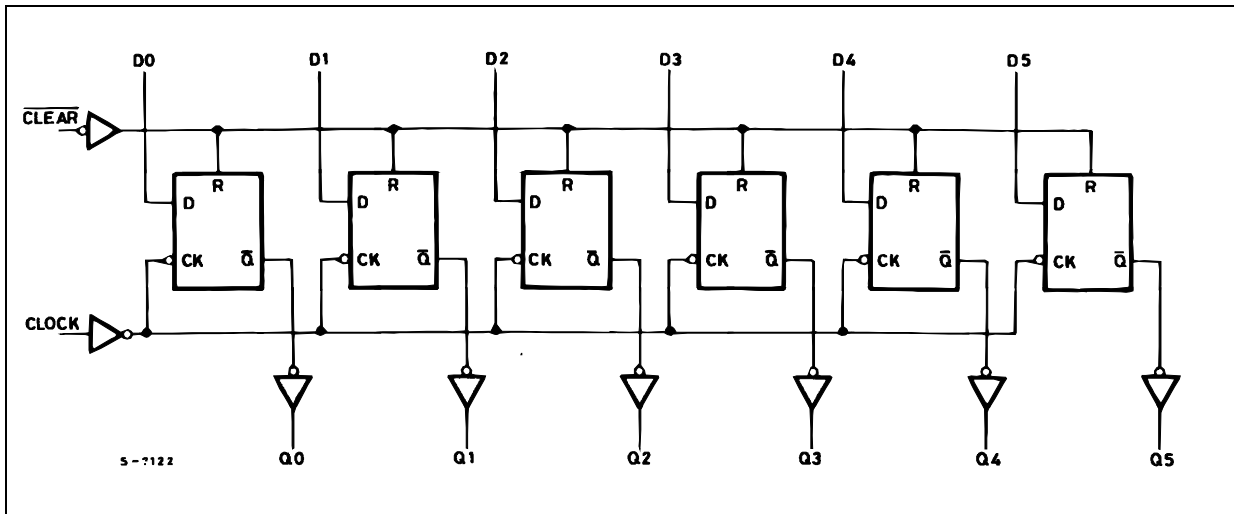
PIN No	SYMBOL	NAME AND FUNCTION
1	CLEAR	Asynchronous Master Reset (Active LOW)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-Flop Outputs
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW-to-HIGH, Edge Triggered)
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
CLEAR	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q <sub>n</sub>	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage (see note 1)	-0.5 to +7.0	V
$V_O$	DC Output Voltage (see note 2)	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

1)  $V_{CC} = 0V$

2) High or Low State

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage (see note 1)	0 to 5.5	V
$V_O$	Output Voltage (see note 2)	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) ( $V_{CC} = 5.0 \pm 0.5V$ )	0 to 20	ns/V

1)  $V_{CC} = 0V$

2) High or Low State

3)  $V_{IN}$  from 0.8V to 2V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> =-50 μA	4.4	4.5		4.4		4.4		V
		4.5	I <sub>O</sub> =-8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =8 mA			0.36		0.44		0.55	
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1.0		± 1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		40	μA
Δ I <sub>CC</sub>	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V <sub>CC</sub> or GND			1.35		1.5		1.5	mA
I <sub>OPD</sub>	Output Leakage Current	0	V <sub>OUT</sub> = 5.5V			0.5		5.0		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CLOCK to Q	5.0(*)	15		5.8	7.8	1.0	9.0	1.0	9.0	ns
		5.0(*)	50		6.3	8.8	1.0	10.0	1.0	10.0	
t <sub>PHL</sub>	Propagation Delay Time CLEAR to Q	5.0(*)	15		7.6	10.4	1.0	13.0	1.0	13.0	ns
		5.0(*)	50		8.1	11.4	1.0	13.0	1.0	13.0	
t <sub>w</sub>	CLEAR Pulse Width LOW	5.0(*)				5.0		5.0		5.0	ns
t <sub>w</sub>	CLEAR Pulse Width HIGH or LOW	5.0(*)				5.0		5.0		5.0	ns
t <sub>s</sub>	Setup Time D to CLOCK, HIGH or LOW	5.0(*)				5.0		6.0		6.0	ns
t <sub>h</sub>	Hold Time D to CLOCK, HIGH or LOW	5.0(*)				0.0		0.0		0.0	ns
t <sub>REM</sub>	Recovery Time CLEAR to CLOCK	5.0(*)				3.0		3.0		3.0	ns
f <sub>MAX</sub>	Maximum Clock Frequency	5.0(*)	15		95	150		80		80	MHz
		5.0(*)	50		55	85		50		50	

(\*) Voltage range is 5.0V ± 0.5V

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Value						Unit	
			T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
			Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance			6	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)			28						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$  (per flip-flop)

## DYNAMIC SWITCHING CHARACTERISTICS

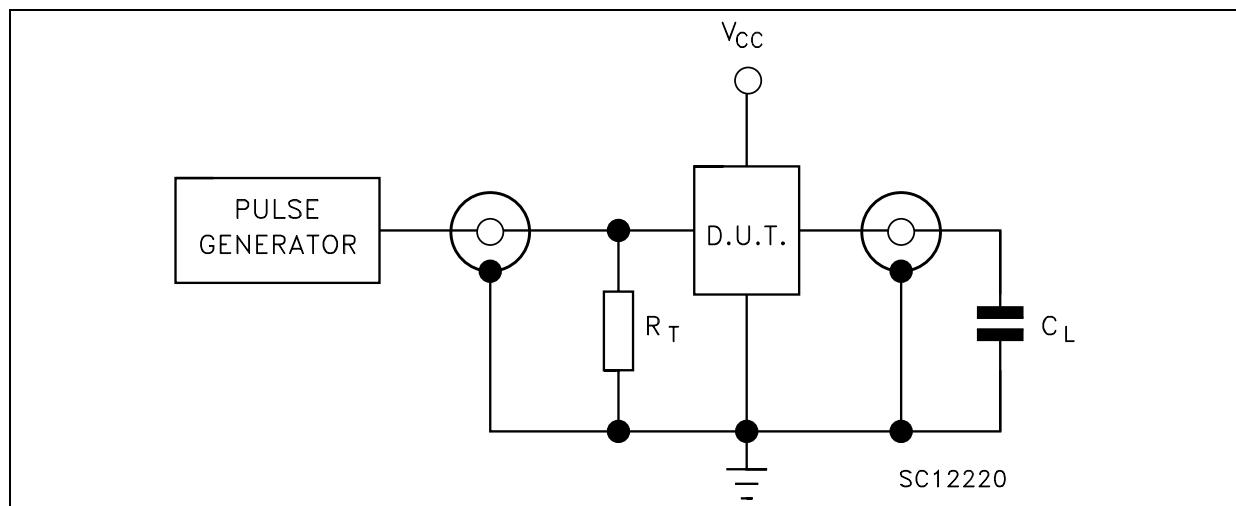
Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C <sub>L</sub> = 50 pF		0.3	0.8					V
V <sub>OLV</sub>				-0.8	-0.3						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	5.0		2.0							
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	5.0				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.0V. Inputs under test switching: 3.0V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

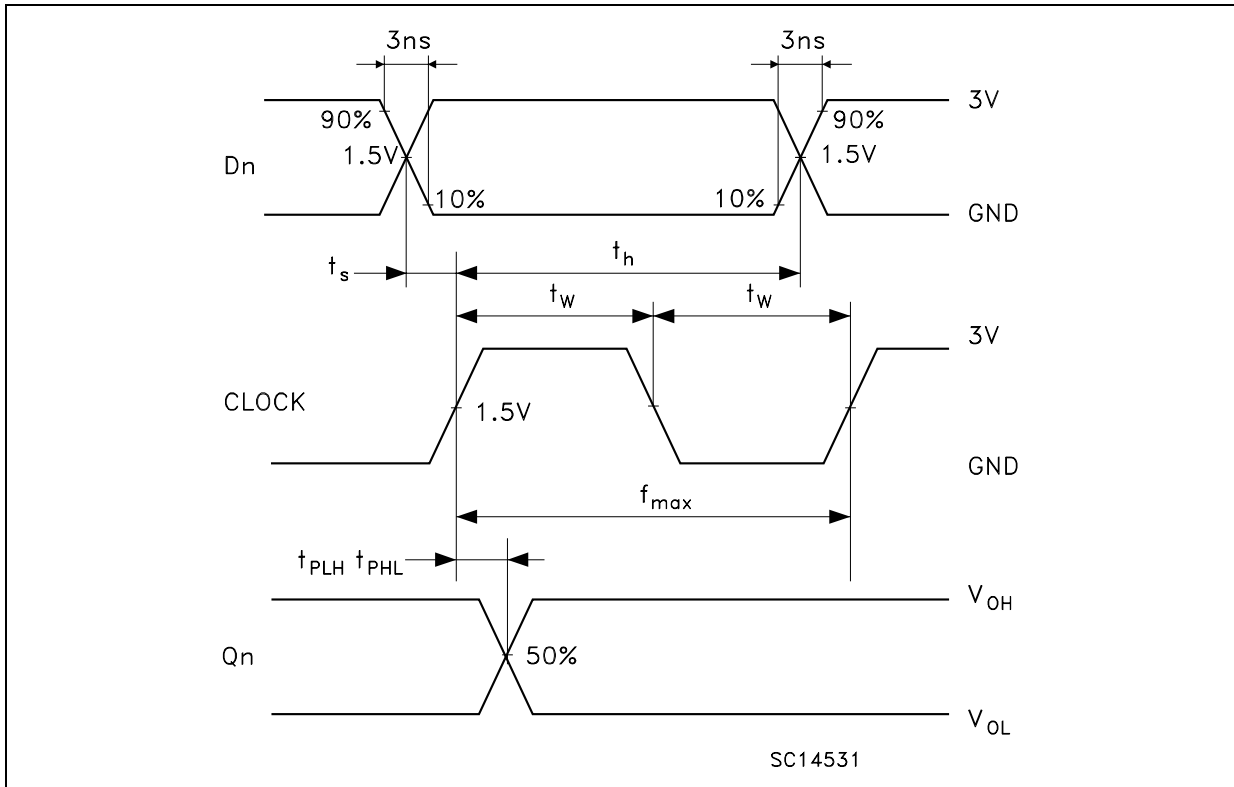
## TEST CIRCUIT



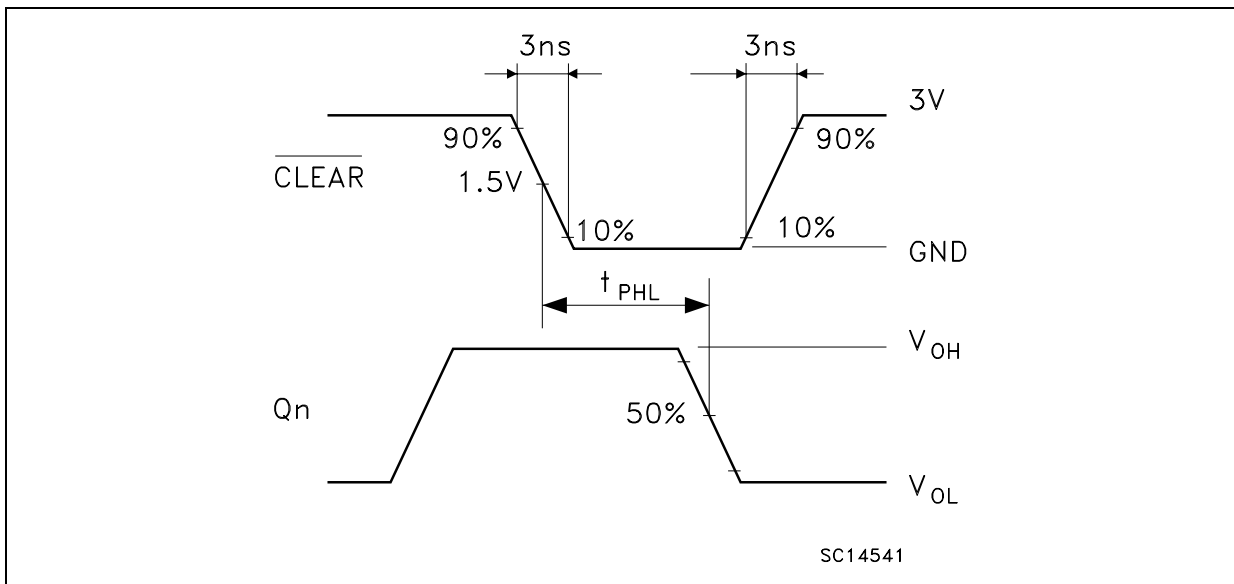
C<sub>L</sub> = 15/50pF or equivalent (includes jig and probe capacitance)

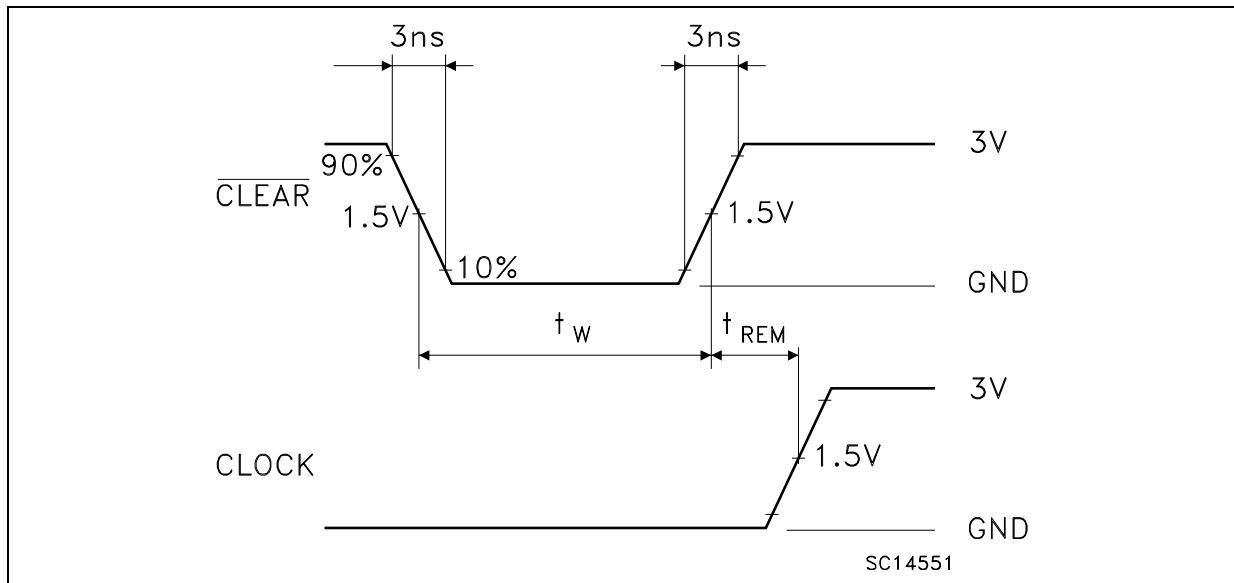
R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



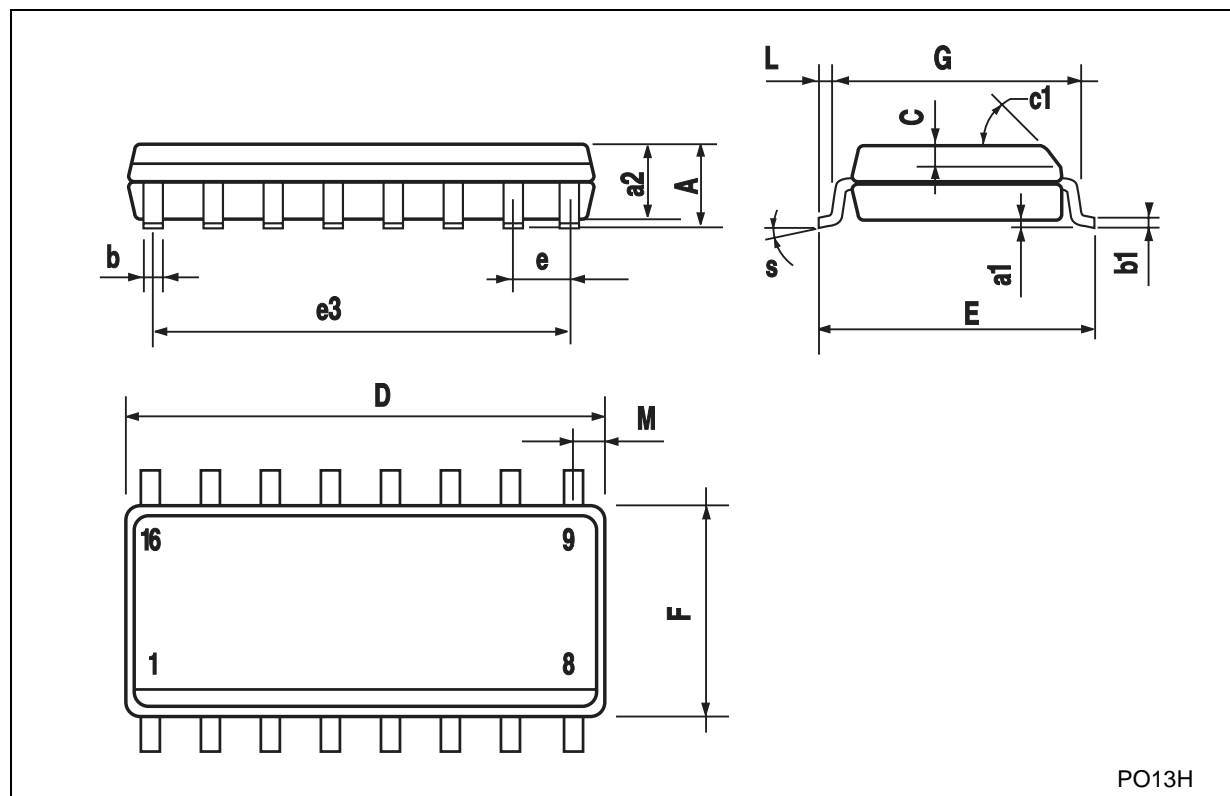
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



**WAVEFORM 3: REMOVAL TIME** ( $f=1\text{MHz}$ ; 50% duty cycle)

## SO-16 MECHANICAL DATA

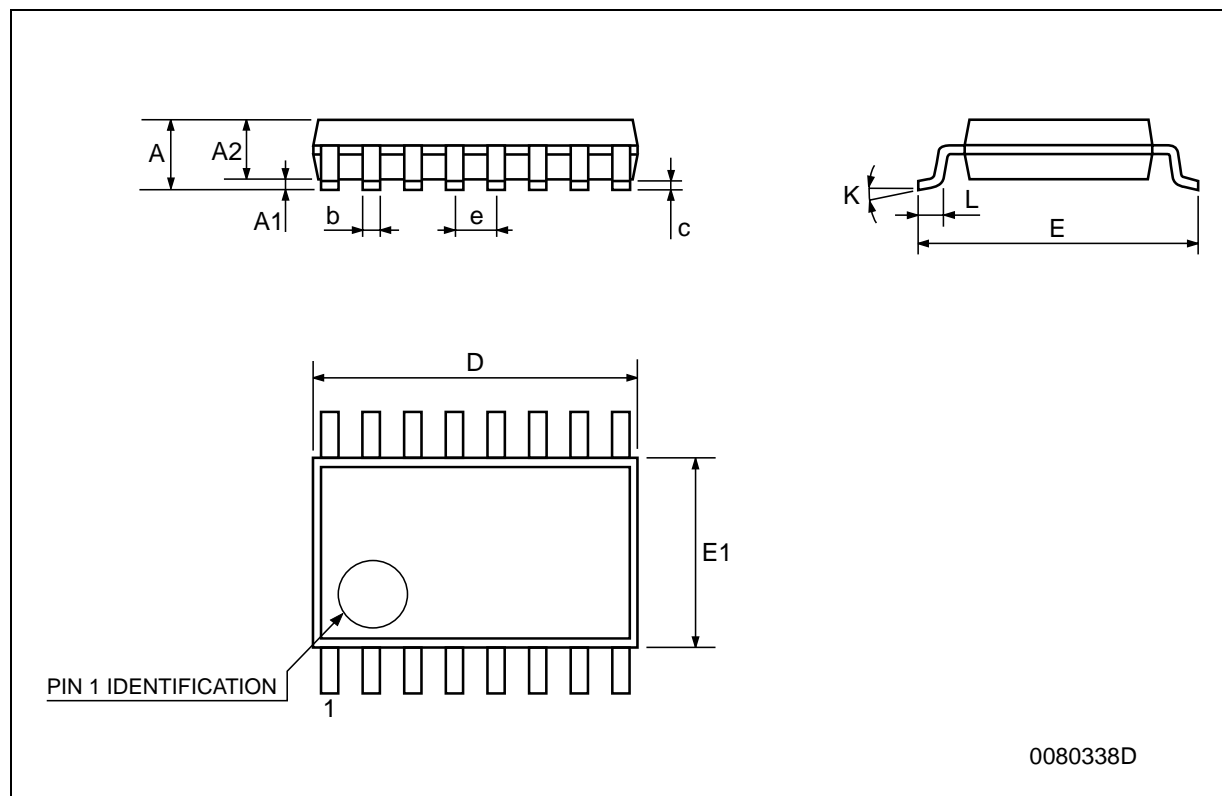
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

## TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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