



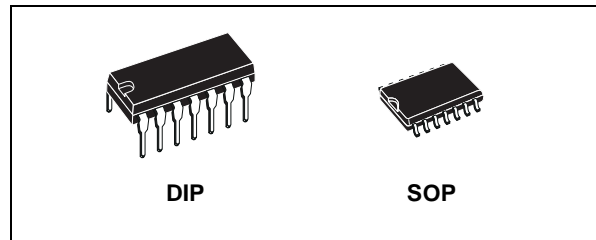
# HCF4013B

## DUAL D-TYPE FLIP FLOP

- SET - RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM SPEED OPERATION 16MHz (TYP.) CLOCK TOGGLE RATE AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

The HCF4013B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The HCF4013B consists of two identical, independent data type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and

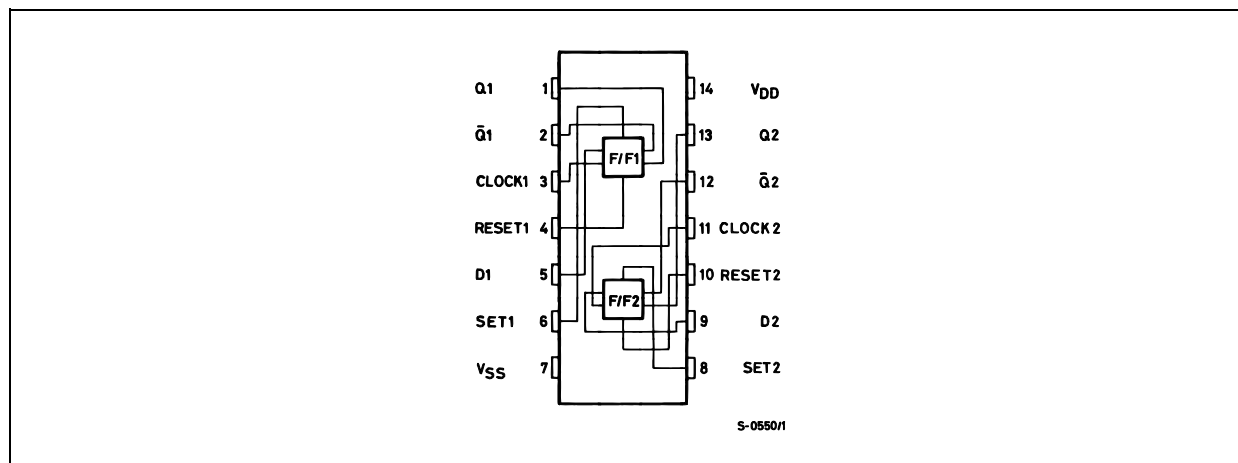


### ORDER CODES

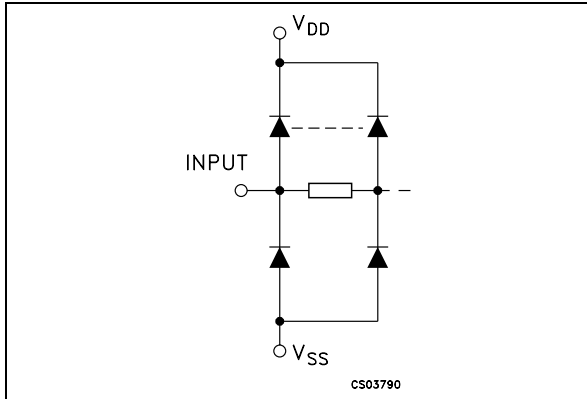
PACKAGE	TUBE	T & R
DIP	HCF4013BEY	
SOP	HCF4013BM1	HCF4013M013TR

Q and  $\bar{Q}$  outputs. This device can be used for shift register applications, and, by connecting  $\bar{Q}$  output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the  $\bar{Q}$  output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively

### PIN CONNECTION



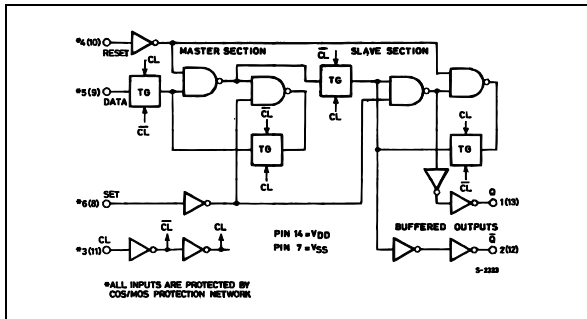
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 11	CLOCK1 CLOCK2	Clock Inputs
4, 10	RESET1 RESET2	Reset Inputs
6, 8	SET1, SET2	Set Inputs
5, 9	D1, D2	Data Inputs
1, 13	Q1, Q2	Data Outputs
2, 12	$\overline{Q1}$ , $\overline{Q2}$	Data Outputs
7	$V_{SS}$	Negative Supply Voltage
14	$V_{DD}$	Positive Supply Voltage

LOGIC DIAGRAM



TRUTH TABLE

CLOCK $\Delta$	D	RESET	SET	Q	$\overline{Q}$
	L	L	L	L	H
	H	L	L	H	L
	X	L	L	Q	$\overline{Q}$
X	X	H	L	L	H
X	X	L	H	H	L
X	X	H	H	H	H

X : Don't Care  
 $\Delta$  : Low Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to  $V_{SS}$  pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.02	1		30		30	$\mu$ A
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

## HCF4013B

### DYNAMIC ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^{\circ}\text{C}$ , $C_L = 50\text{pF}$ , $R_L = 200\text{K}\Omega$ , $t_r = t_f = 20\text{ ns}$ )

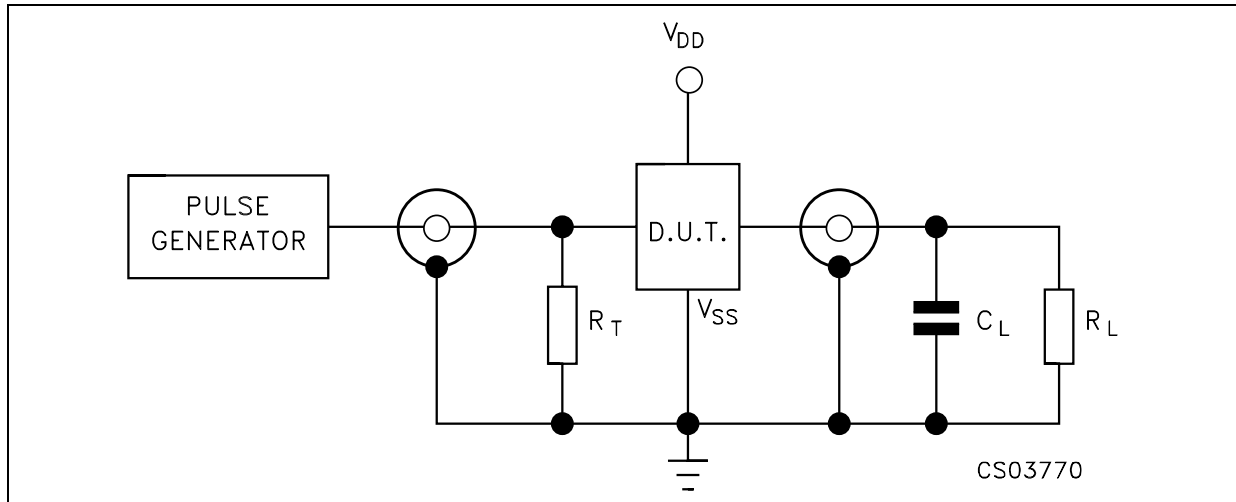
Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{TLH}$ $t_{THL}$	Propagation Delay Time (CLOCK to Q or $\bar{Q}$ outputs)	5			150	300	ns
		10			65	130	
		15			45	90	
$t_{PLH}$	Propagation Delay Time (SET to Q or RESET to Q)	5			150	300	ns
		10			65	130	
		15			45	90	
$t_{PHL}$	Propagation Delay Time (SET to Q or RESET to Q)	5			200	400	ns
		10			85	170	
		15			60	120	
$t_{THL}$ $t_{TLH}$	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
$f_{CL}^{(1)}$	Maximum Clock Input Frequency	5		3.5	7		MHz
		10		8	16		
		15		12	24		
$t_W$	Clock Pulse Width	5		140	70		ns
		10		60	30		
		15		40	20		
$t_r, t_f^{(2)}$	Clock Input Rise or Fall Time	5				15	$\mu\text{s}$
		10				4	
		15				1	
$t_W$	Set or Reset Pulse Width	5		180	90		ns
		10		80	40		
		15		50	25		
$t_{setup}$	Data Setup Time	5		40	20		ns
		10		20	10		
		15		15	7		

(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.

(1) Input  $t_r, t_f = 5\text{ ns}$

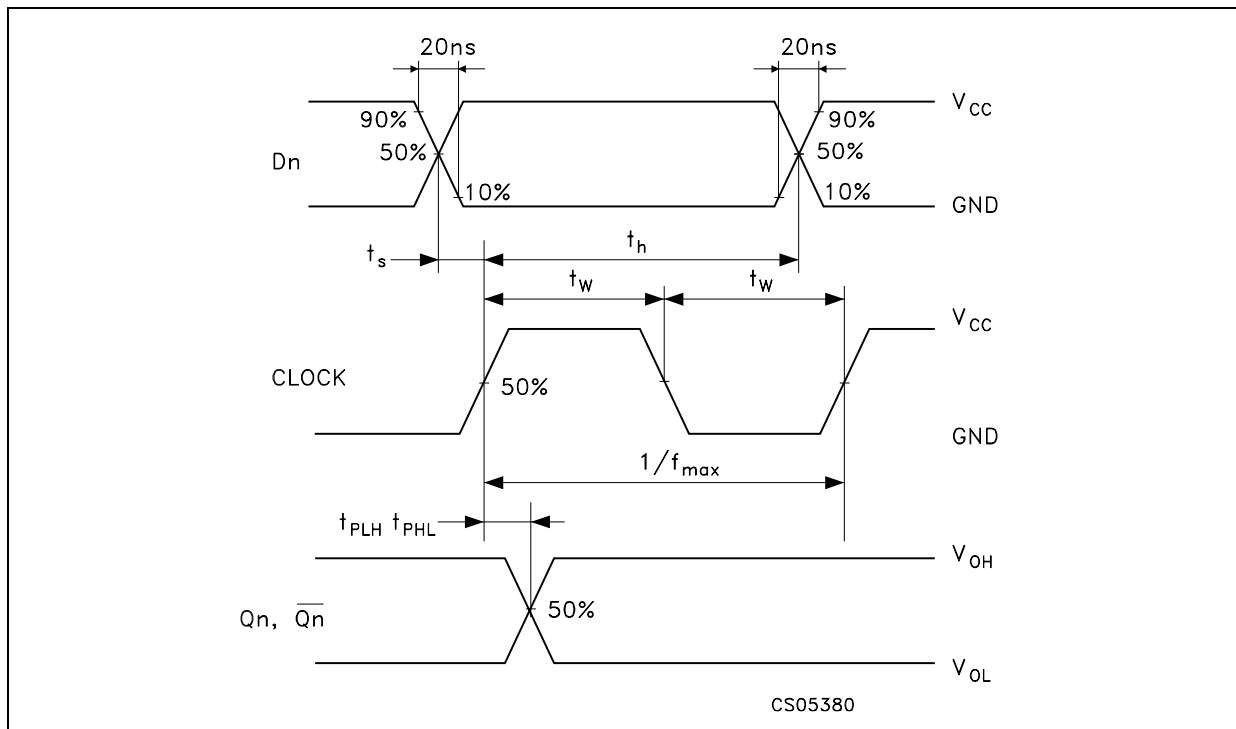
(2) If more than unit is cascaded in a parallel clocked application,  $t_r$  should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the carry output driving stage for the estimated capacitive load.

TEST CIRCUIT

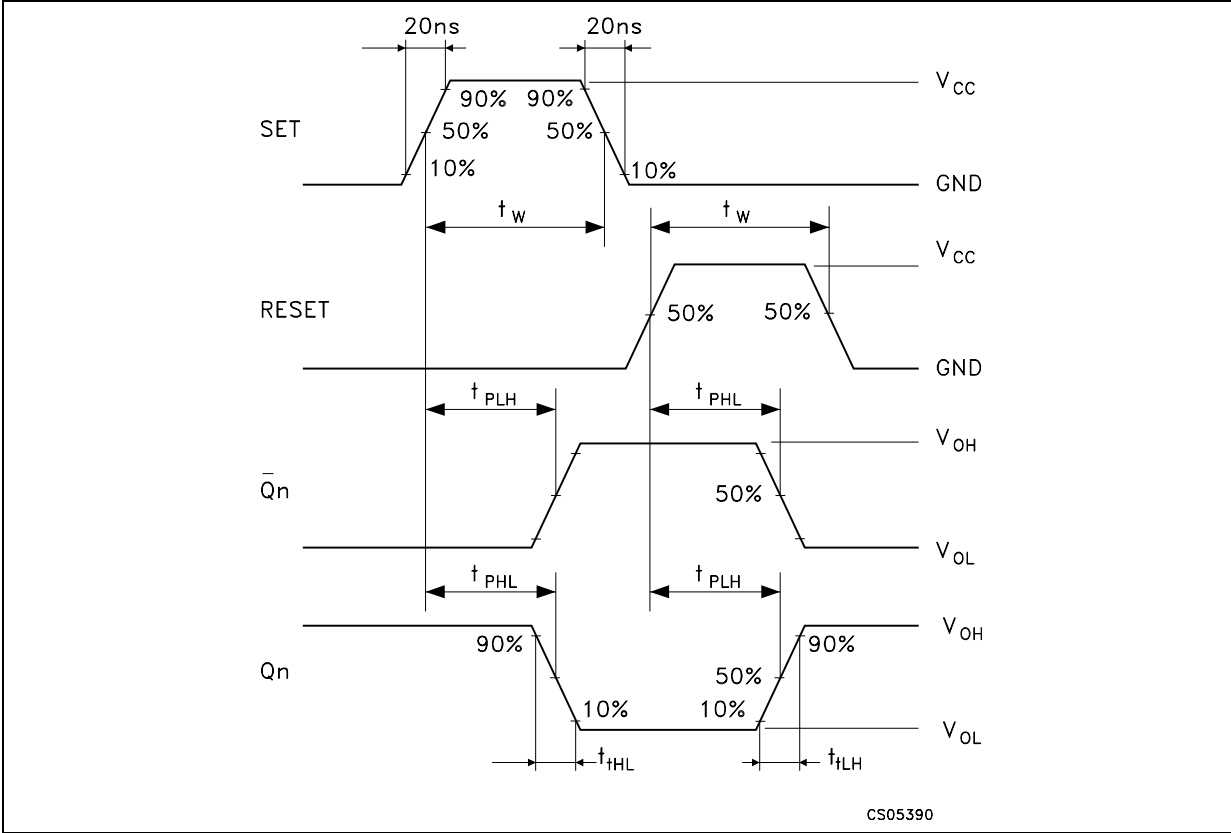


$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = 200\text{K}\Omega$   
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**WAVEFORM 1 : CLOCK TO  $Q_n$ ,  $\bar{Q}_n$  PROPAGATION DELAY TIMES,  $D_n$  TO CLOCK SETUP AND HOLD TIMES, CLOCK MINIMUM PULSE WIDTH, MAXIMUM CLOCK FREQUENCY**  
 ( $f=1\text{MHz}$ ; 50% duty cycle)

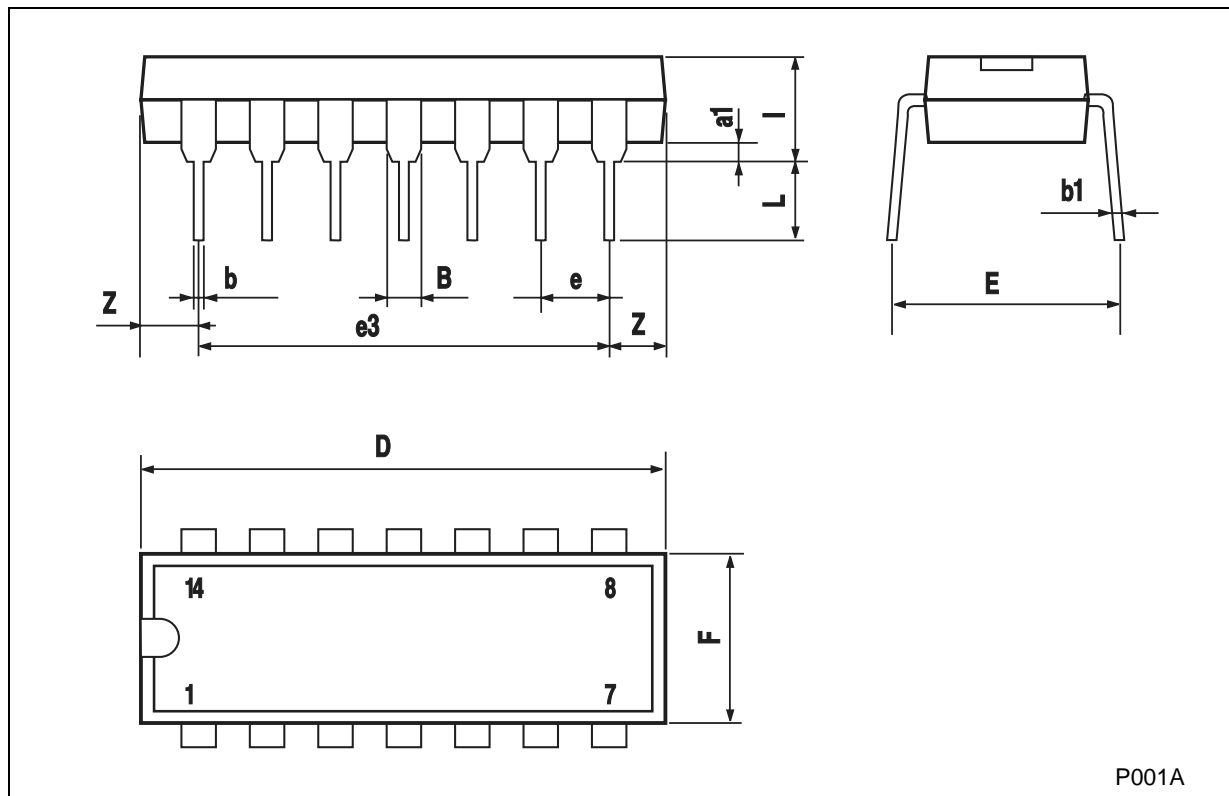


WAVEFORM 2 : PROPAGATION DELAY TIMES ( $Q_n$ ,  $\bar{Q}_n$  TO SET, RESET), MINIMUM PULSE WIDTH (SET AND RESET) ( $f=1\text{MHz}$ ; 50% duty cycle)



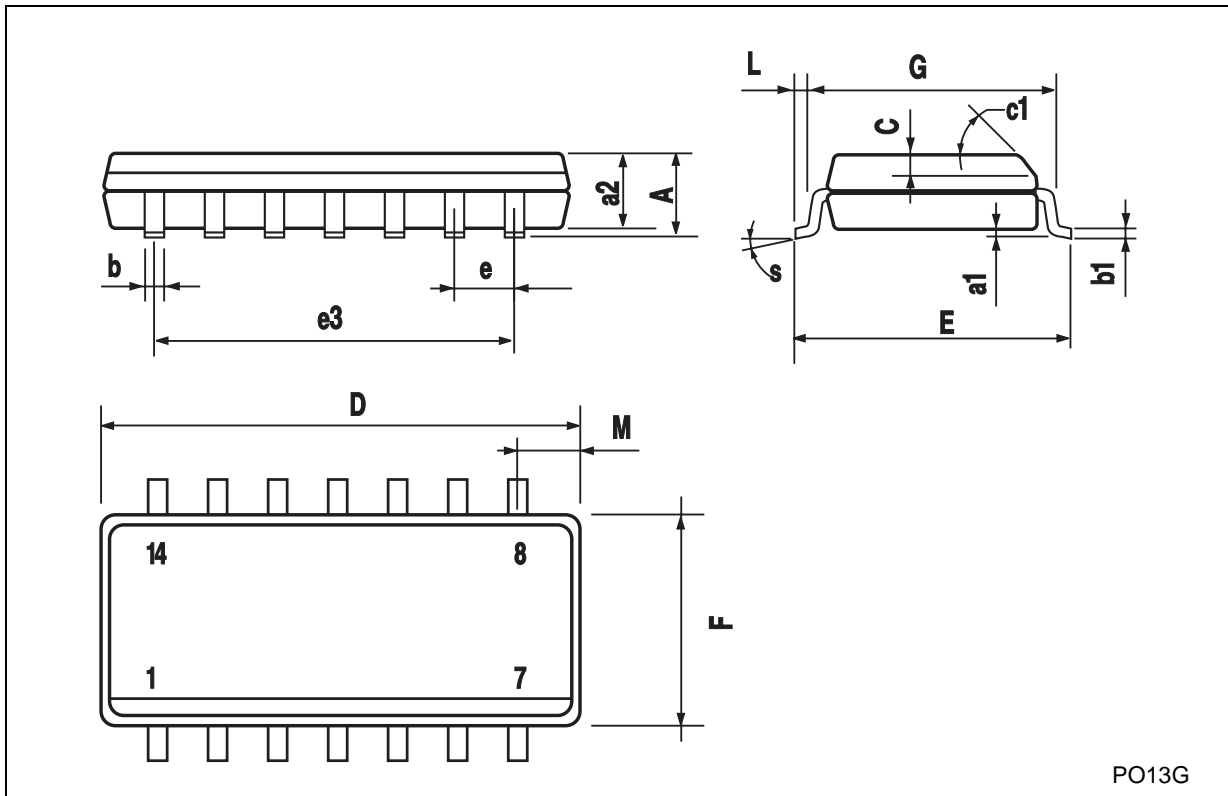
<b>Plastic DIP-14 MECHANICAL DATA</b>						
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DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



**SO-14 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G



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