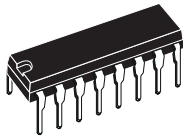
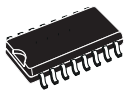
HCF4026B

DECADE COUNTER/DIVIDER WITH DECODED 7-SEGMENT DISPLAY OUTPUT AND DISPLAY ENABLE

- COUNTER AND 7-SEGMENT DECODING IN ONE PACKAGE
- EASILY INTERFACED WITH 7-SEGMENT DISPLAY TYPES
- FULLY STATIC COUNTER OPERATION : DC TO 6MHz (Typ.) AT V_{DD} = 10V
- IDEAL FOR LOW POWER DISPLAYS
- DISPLAY ENABLE OUTPUT
- QUIESCENT CURRENT SPECIF. UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

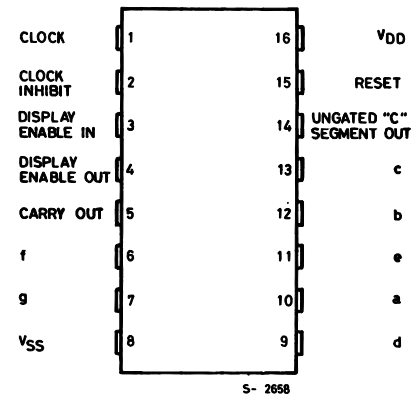
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4026BEY	
SOP	HCF4026BM1	HCF4026M013TR

DESCRIPTION

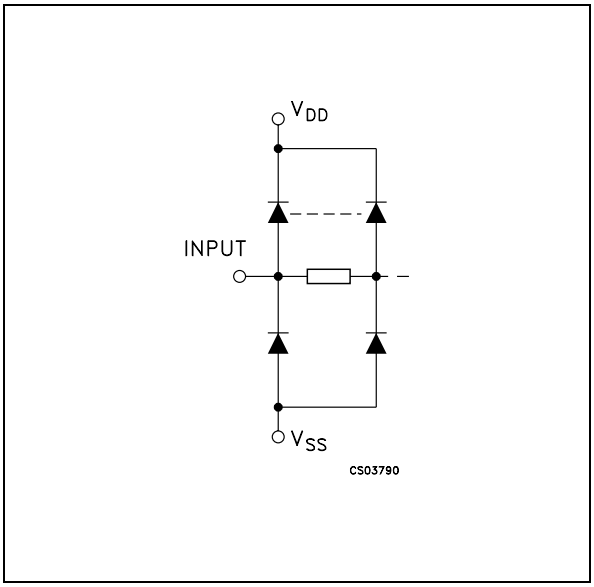
The HCF4026B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4026B consists of a 5-stages Johnson decade counter and an output decoder which converts the Johnson code to a 7 segment decoded output for driving one stage in a numerical display. This device is particularly advantageous in display applications where low power dissipation and/or low package count are important. This device has CLOCK, RESET, CLOCK INHIBIT, DISPLAY ENABLE input and CARRY OUT, DISPLAY ENABLE, UNGATED "C" SEGMENT and 7 DECODED outputs (a to g).
A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C_{OUT}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

PIN CONNECTION



The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high when the DISPLAY ENABLE IN is high. When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display character multiplexing. The CARRY OUT and UNGATED "C" SEGMENT signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider function such a as divide by 60 and divide by 12.

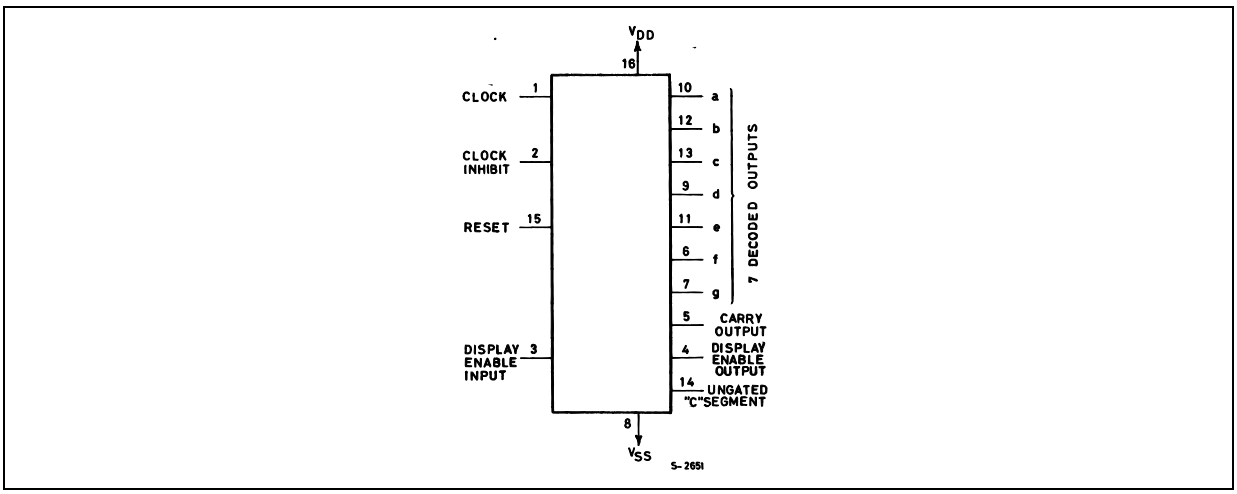
IINPUT EQUIVALENT CIRCUIT



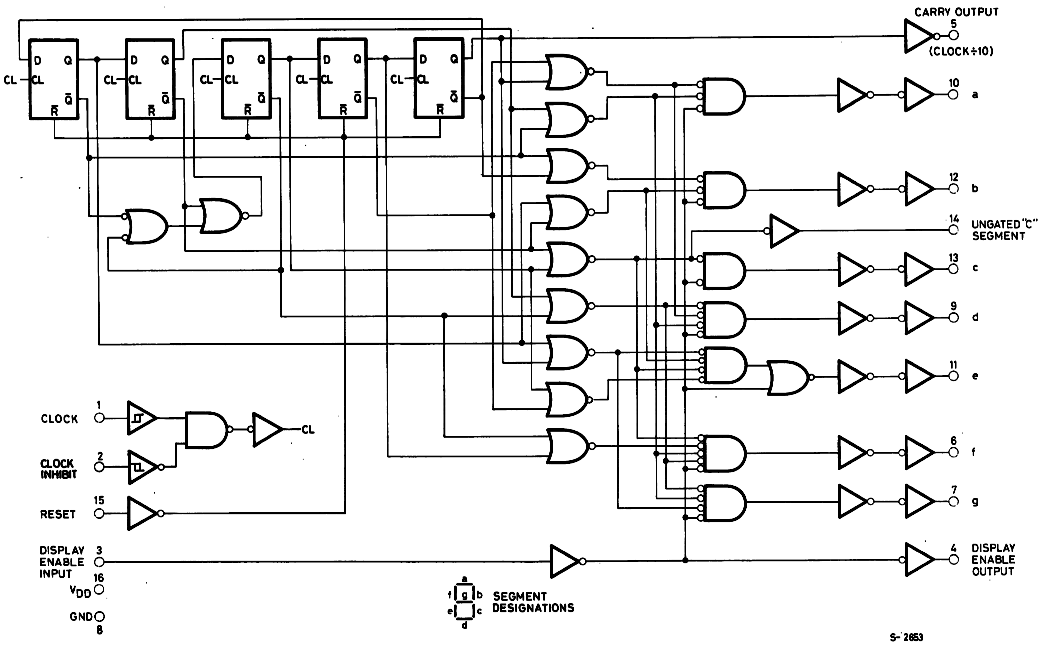
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK	Clock Input
10, 12, 13, 9, 11, 6, 7	a to g	7 - Segments Decoded Outputs
2	CLOCK INHIBIT	Clock Inhibit Input
15	RESET	Reset Input
3	DISPLAY ENABLE IN	Display Enable Input
5	CARRY OUT	Carry Out Output
4	DISPLAY ENABLE OUT	Display Enable Output
14	UNGATED "C" SEG-MENT OUT	Ungated "C" Segment Output
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

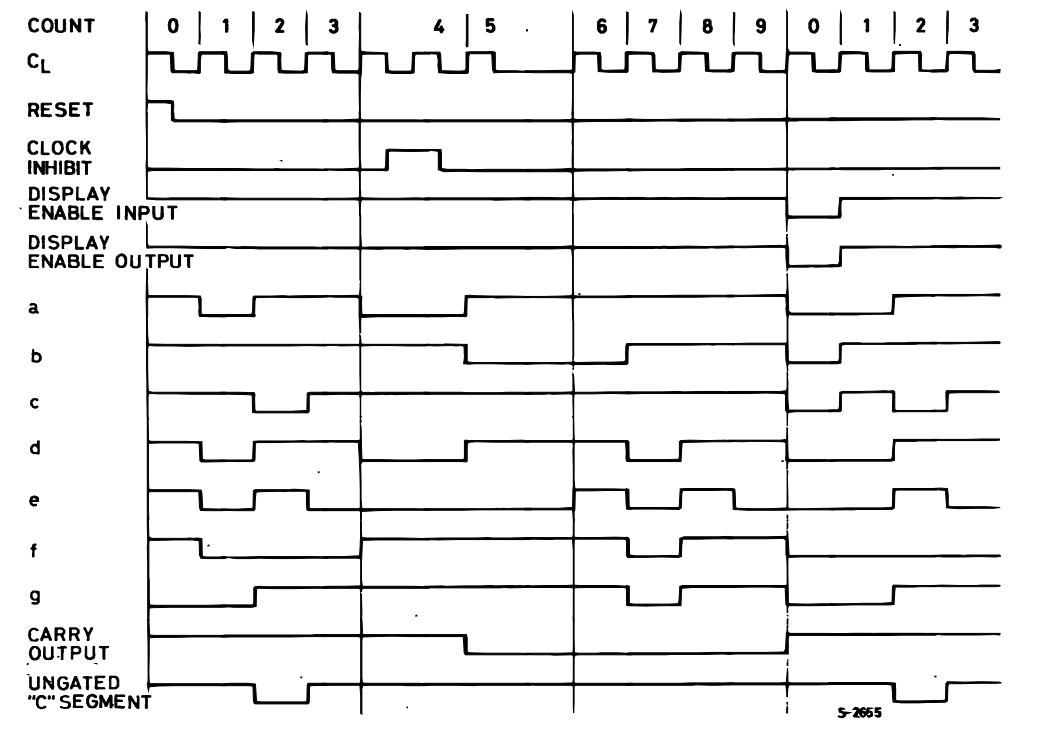
FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/18.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		0.5/4.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			1.5/18.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5		5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6		5	-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4		5	0.44	1		0.36		0.36		mA
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	any input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		any input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

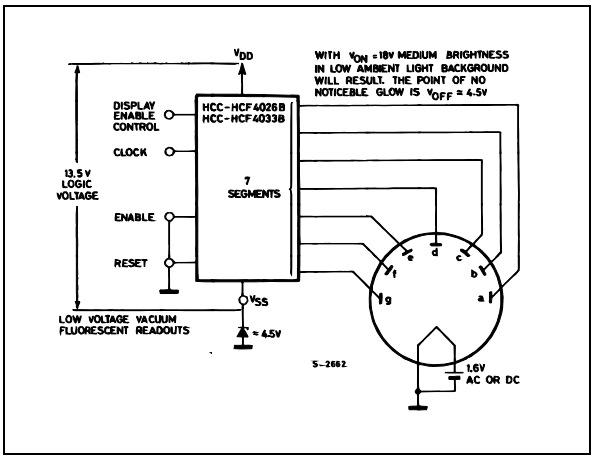
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
CLOCKED OPERATION							
t_{PLH} t_{PHL}	Propagation Delay Time (Carry Out Line)	5			250	500	ns
		10			100	200	
		15			75	150	
t_{PLH} t_{PHL}	Propagation Delay Time (Decoded Out Lines)	5			350	700	ns
		10			125	250	
		15			90	180	
t_{THL} t_{TLH}	Transition Time (Carry Out Line)	5			100	200	ns
		10			50	100	
		15			25	50	
f_{CL} (1)	Maximum Clock Input Frequency	5		2.5	5		MHz
		10		5.5	11		
		15		8	16		
t_{WC}	Clock Pulse Width	5			110	260	ns
		10			50	100	
		15			40	80	
t_r , t_f	Clock Input Rise or Fall Time	5		Unlimited			µs
		10					
		15					
RESET OPERATION							
t_{PLH} t_{PHL}	Propagation Delay Time (Carry Out Line)	5			275	550	ns
		10			120	240	
		15			80	160	
t_{PLH} t_{PHL}	Propagation Delay Time (Decoded Out Lines)	5			300	600	ns
		10			125	250	
		15			90	180	
t_{WR}	Reset Pulse Widht	5			100	120	ns
		10			50	100	
		15			25	50	
t_{rem}	Reset Removal Time	5			0	30	ns
		10			0	15	
		15			0	10	

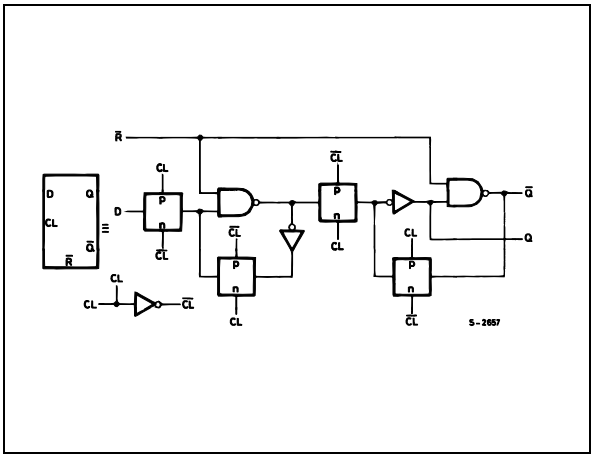
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) Measured with respect to carry output line.

TYPICAL APPLICATIONS

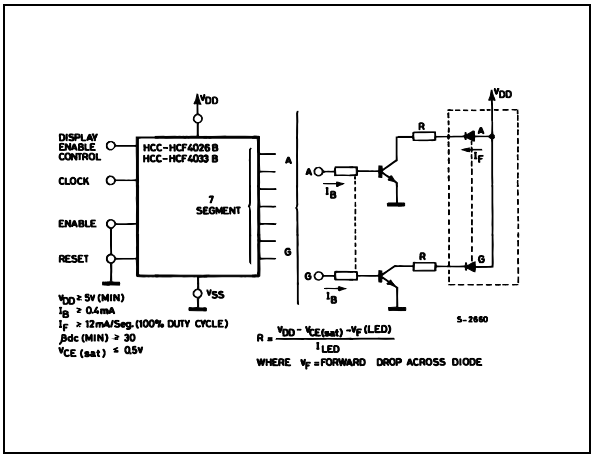
Interfacing with Filament Fluorescent Display



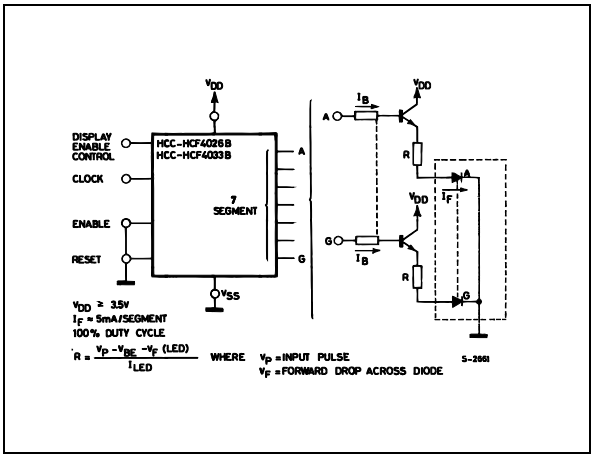
Detail of Typical Flip-flop Stage



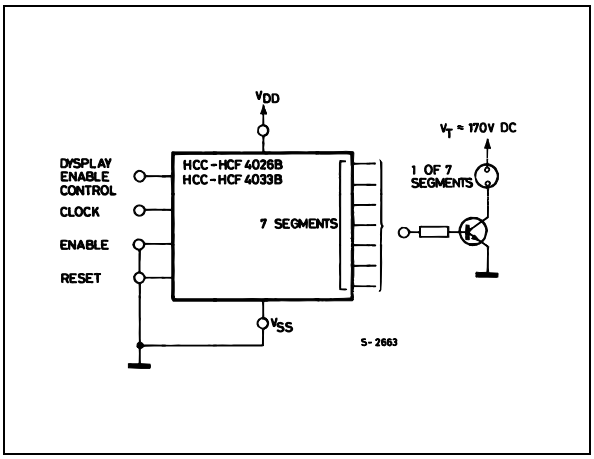
Interfacing with LED Displays (display common anode)



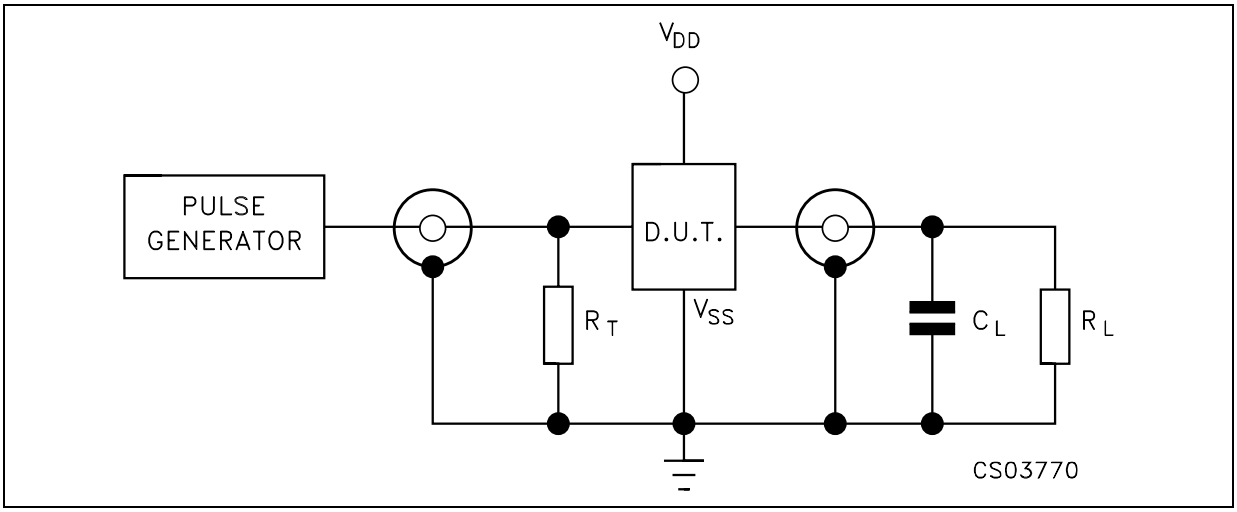
Interfacing with LED Displays (display common cathode)



Interfacing with NIXIE Tube



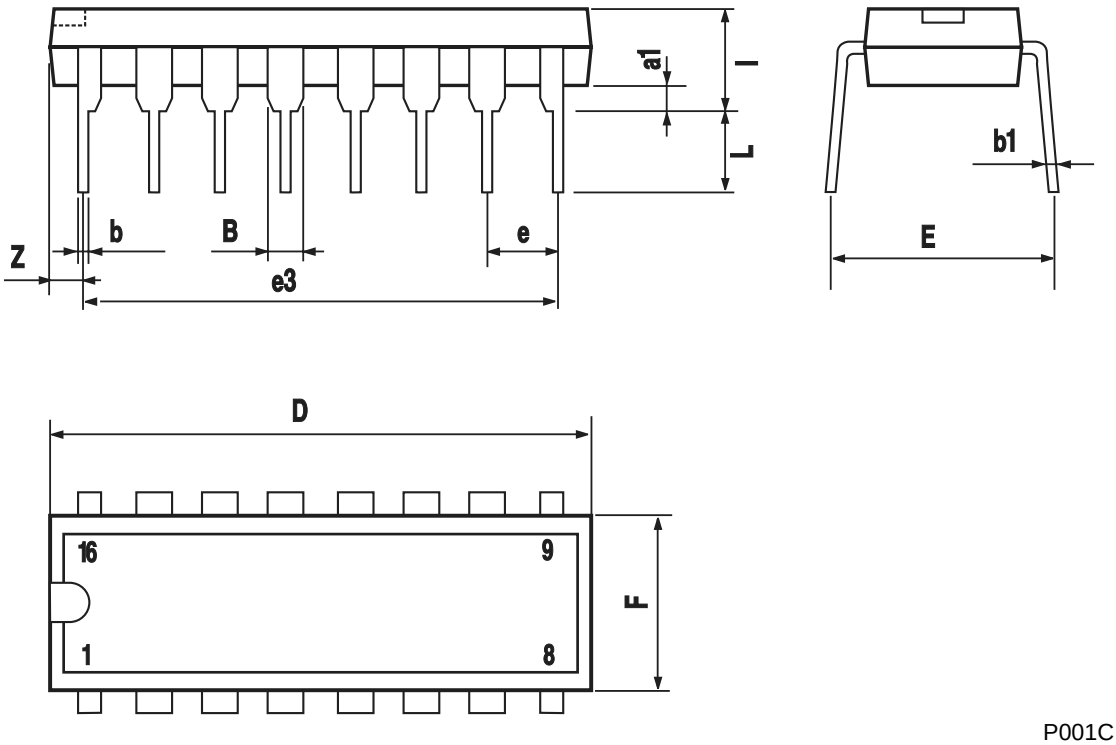
TEST CIRCUIT



C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Plastic DIP-16 (0.25) MECHANICAL DATA

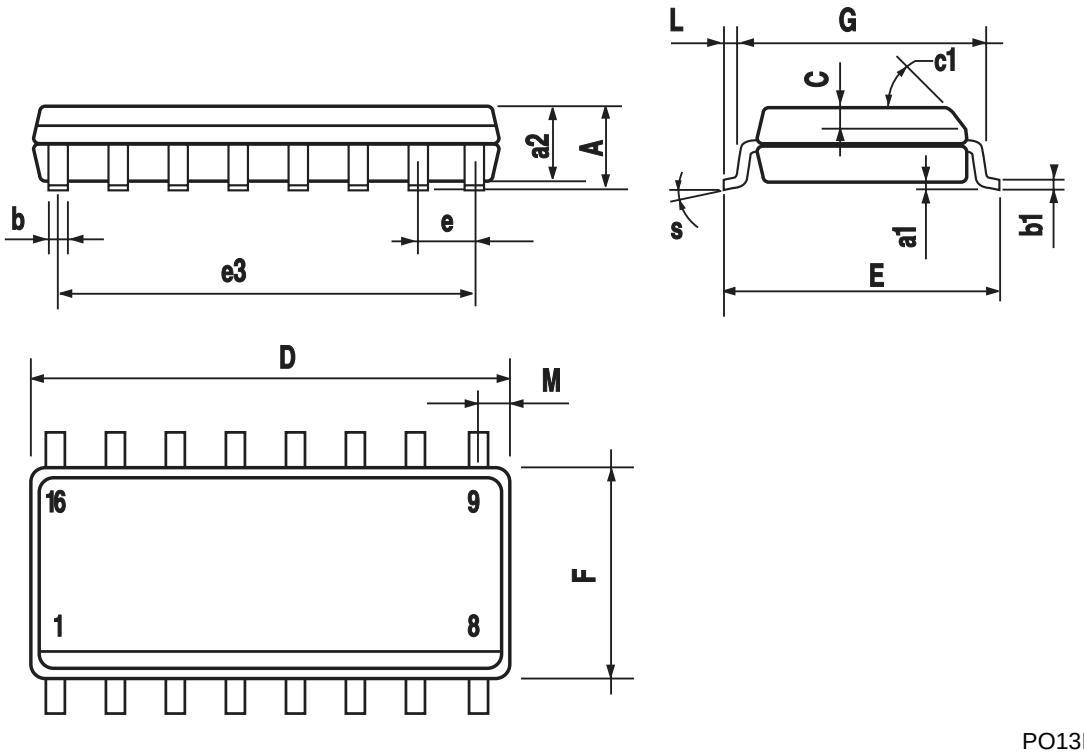
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



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