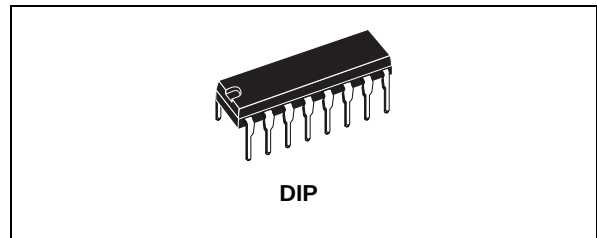


BCD RATE MULTIPLEXER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO 9 INPUT AND 9 DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4527BEY	

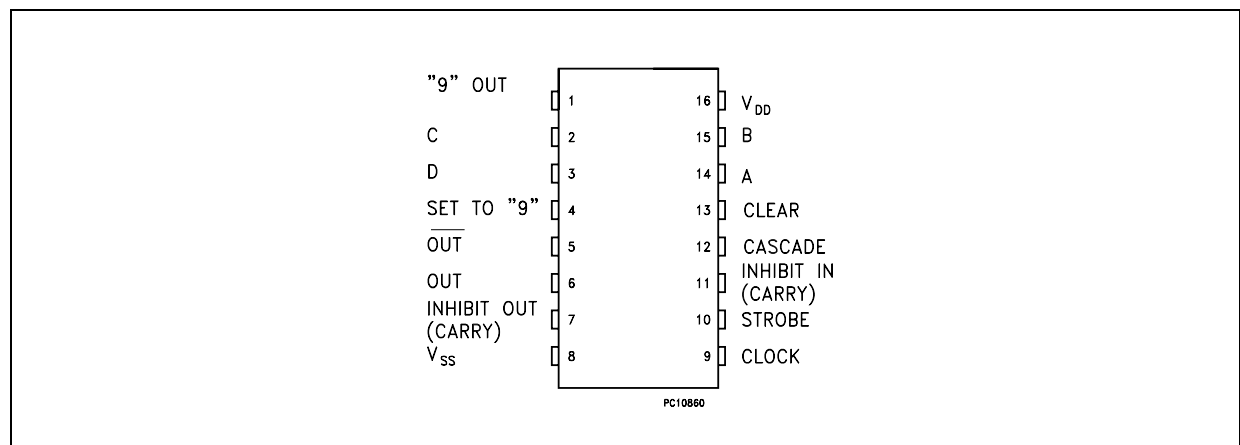
DESCRIPTION

HCF4527B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP package.

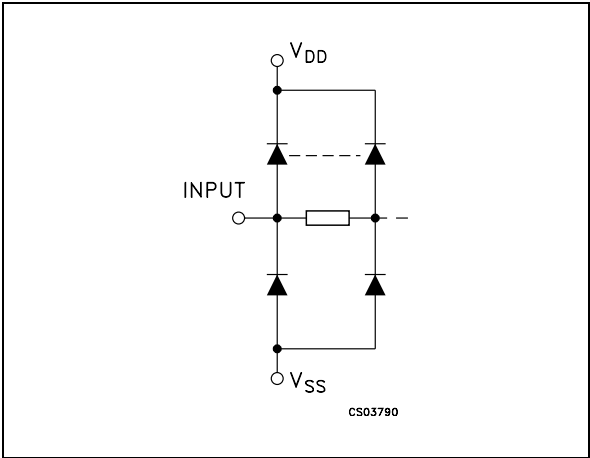
This device is a low power 4-bit digital rate multiplier that provides an output pulse rate which is the clock input pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD

input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

PIN CONNECTION



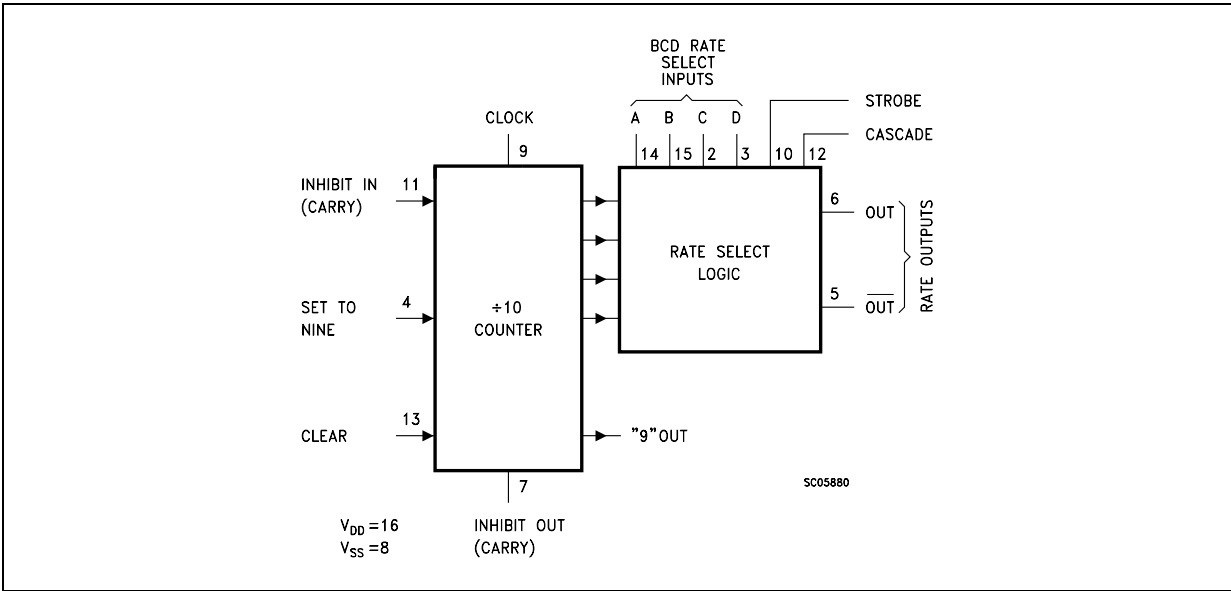
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
14, 15, 2, 3	A, B, C, D	BCD Rate Select Inputs
10	STROBE	Strobe Input
12	CASCADE	Cascade
5, 6	OUT, OUT	Rate Outputs
9	CLOCK	Clock Input
11	INHIBIT IN	Inhibit Input (Carry)
4	SET TO "9"	Set Input
13	CLEAR	Clear Input
7	INHIBIT OUT	Inhibit Out (Carry)
1	"9" OUT	Output
8	V _{SS}	Negative Supply Voltage
16	V _{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



TRUTH TABLE

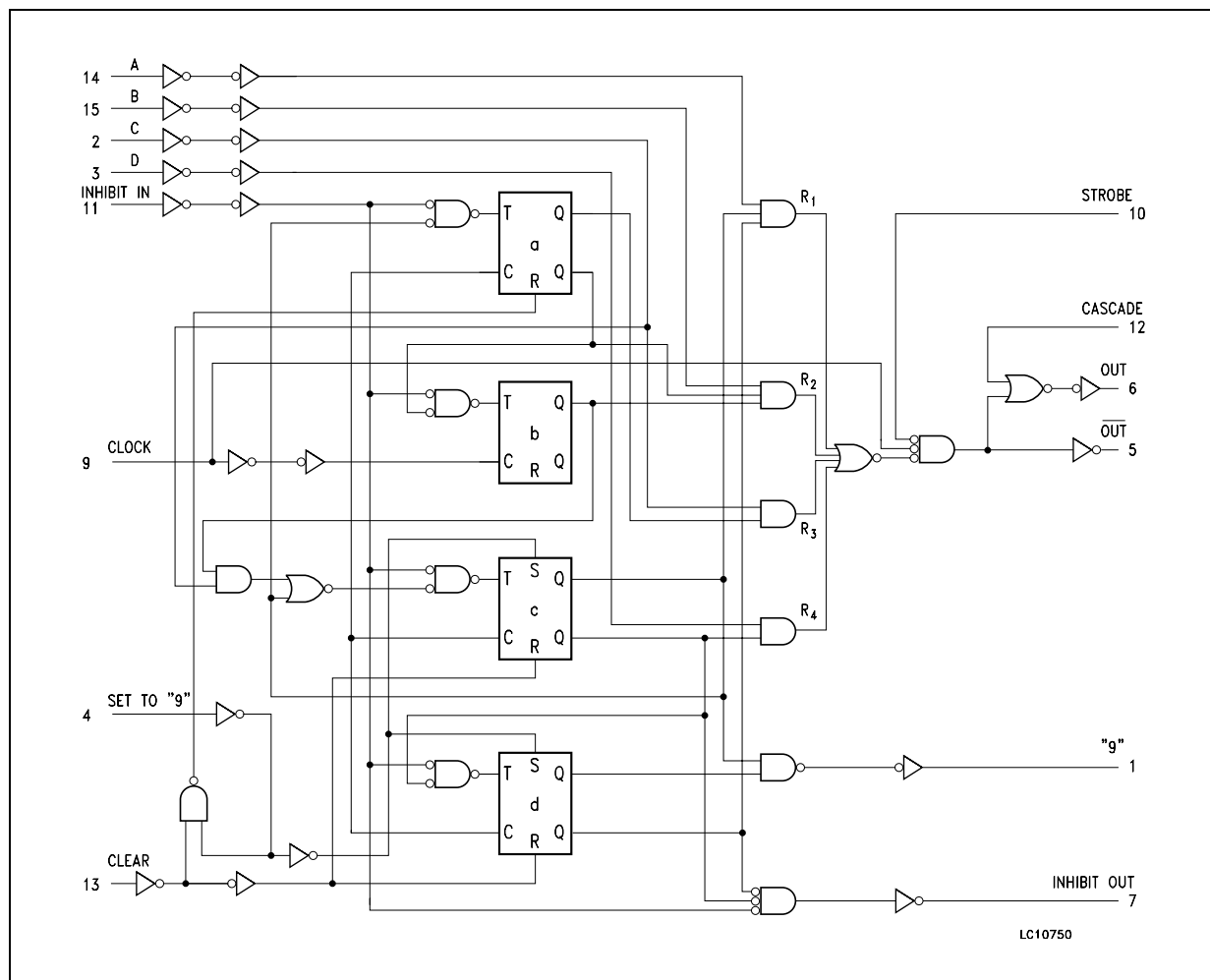
INPUTS										OUTPUTS			
Number of Pulses or Logic Level										Number of Pulses or Output Logic Level			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{\text{OUT}}$	INH OUT	"9" OUT
L	L	L	L	10	L	L	L	L	L	L	H	1	1
L	L	L	H	10	L	L	L	L	L	1	1	1	1
L	L	H	L	10	L	L	L	L	L	2	2	1	1
L	L	H	H	10	L	L	L	L	L	3	3	1	1
L	H	L	L	10	L	L	L	L	L	4	4	1	1
L	H	L	H	10	L	L	L	L	L	5	5	1	1
L	H	H	L	10	L	L	L	L	L	6	6	1	1
L	H	H	H	10	L	L	L	L	L	7	7	1	1
H	L	L	L	10	L	L	L	L	L	8	8	1	1
H	L	L	H	10	L	L	L	L	L	9	9	1	1
H	L	H	L	10	L	L	L	L	L	8	8	1	1
H	L	H	H	10	L	L	L	L	L	9	9	1	1
H	H	L	L	10	L	L	L	L	L	8	8	1	1
H	H	L	H	10	L	L	L	L	L	9	9	1	1
H	H	H	L	10	L	L	L	L	L	8	8	1	1
H	H	H	H	10	H	L	L	L	L	9	9	1	1
X	X	X	X	10	L	H	L	L	L	**	**	H	**
X	X	X	X	10	L	L	L	L	L	L	H	1	1
X	X	X	X	10	L	L	H	L	L	H	*	1	1
H	X	X	X	10	L	L	L	H	L	10	10	H	L
L	X	X	X	10	L	L	L	H	L	L	H	H	L
X	X	X	X	10	L	L	L	L	H	L	H	L	H

X : Don't Care

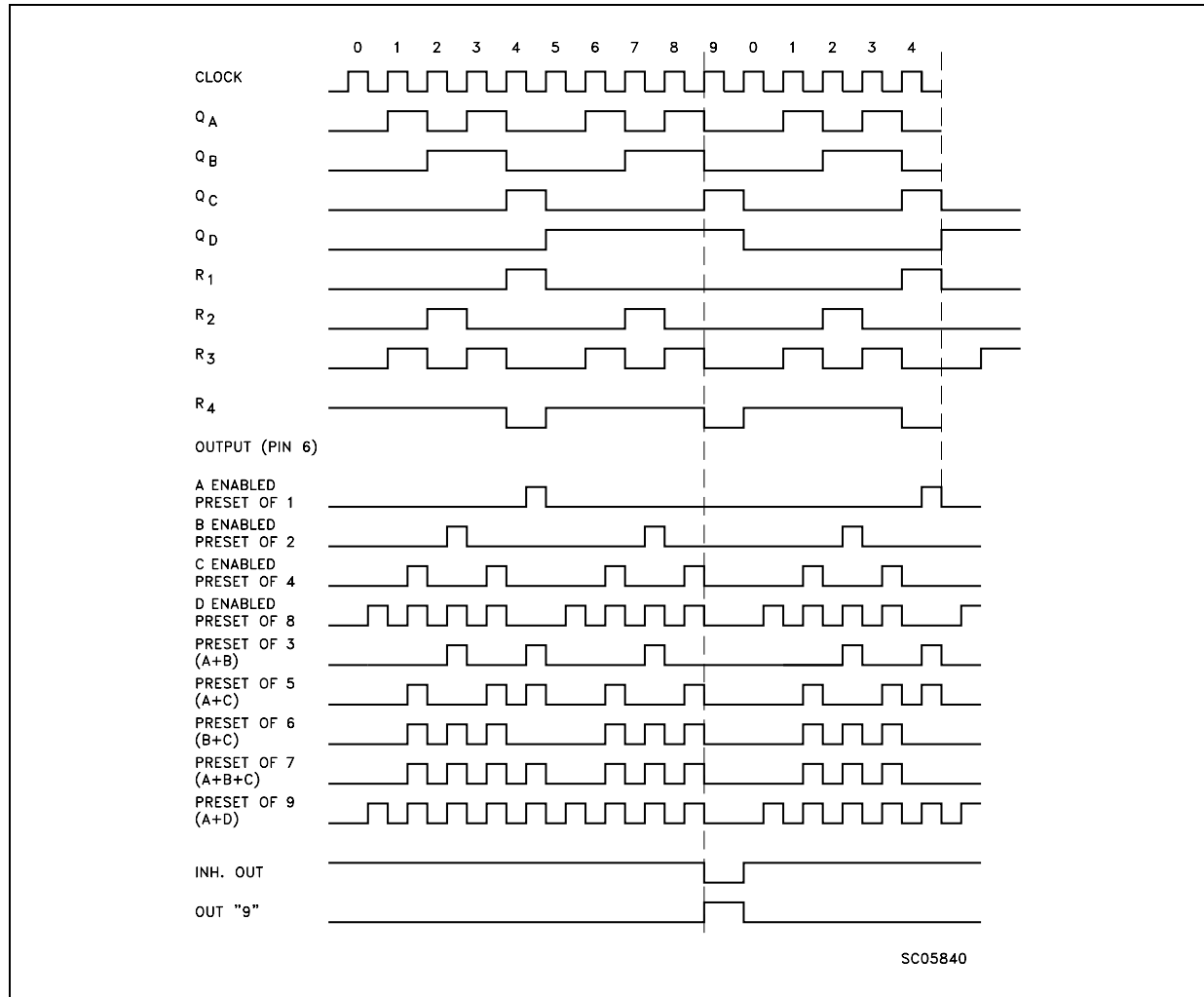
** : Depends on internal state of counter.

* : Output same as the first 16 lines of this truth table (depending on value of A, B, C, D)

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V _I (V)	V _O (V)	I _{OL} (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current (Source) Q, Q', Q' CL _D	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current Q	0/5	0.4	<1	5	1.74	4		1.43		1.43		mA
		0/10	0.5	<1	10	4.42	10.4		3.74		3.74		
		0/15	1.5	<1	15	11.56	27.2		9.52		9.52		
I _{OL}	Output Sink Current Q, Q', CL _D	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA
C _I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}=5V$, 2V min. with $V_{DD}=10V$, 2.5V min. with $V_{DD}=15V$

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time : Clock to Output	5			110	220	ns
		10			55	110	
		15			45	90	
t_{PLH}, t_{PHL}	Propagation Delay Time : Clock or Strobe to Output	5			150	300	ns
		10			75	150	
		15			60	120	
t_{PLH}	Propagation Delay Time : Clock to Inhibit Output	5			320	640	ns
		10			145	290	
		15			100	200	
t_{PHL}	Propagation Delay Time : Clock to Inhibit Output	5			250	500	ns
		10			100	200	
		15			75	150	
t_{PLH}, t_{PHL}	Propagation Delay Time : Clear to Output	5			380	760	ns
		10			175	550	
		15			130	260	
t_{PLH}, t_{PHL}	Propagation Delay Time : Clock to "9" or "1" Q Output	5			300	600	ns
		10			125	250	
		15			90	180	
t_{PLH}, t_{PHL}	Propagation Delay Time : Cascade to Output	5			90	180	ns
		10			45	90	
		15			35	70	
t_{PLH}, t_{PHL}	Propagation Delay Time : Inhibit Input to Inhibit Output	5			130	260	ns
		10			60	120	
		15			45	90	
t_{PLH}, t_{PHL}	Propagation Delay Time : Set to Output	5			330	660	ns
		10			150	300	
		15			110	220	
t_{THL}, t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f_{CL}	Maximum Clock Frequency	5		1.2	2.4		MHz
		10		2.5	5		
		15		3.5	7		
t_W	Clock Pulse Width	5		330	165		ns
		10		170	85		
		15		100	50		
t_r, t_f	Clock Rise or Fall Time	5				15	μs
		10				15	
		15				15	
t_W	Set or Clear Pulse Width	5		160	80		ns
		10		90	45		
		15		60	30		
t_{setup}	Inhibit Input Setup Time	5		100	50		ns
		10		40	20		
		15		20	10		

Symbol	Parameter	Test Condition		Value (*)			Unit
		V _{DD} (V)		Min.	Typ.	Max.	
t _R	Inhibit Input Removal Time	5		240	120		ns
		10		130	65		
		15		110	55		
t _R	Set Removal Time	5		150	75		ns
		10		80	40		
		15		50	25		
t _R	Clear Removal Time	5		60	30		ns
		10		40	20		
		15		30	15		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

APPLICATION NOTE :

For fractional multipliers with more than one digit, HCF4527B may be cascaded in two different modes: The ADD mode and the MULTIPLY mode (see figure 1 and 2).

When two units are cascaded in ADD mode and programmed to 9 and 4 respectively, the more significant unit will have 9 output pulses for every 10 input pulses and the other will have 4 output pulses for every 100 input pulses for a total of :

$$\frac{9}{10} + \frac{4}{100} = \frac{94}{100}$$

In the multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one :

If N₁ = 9 and N₂ = 4

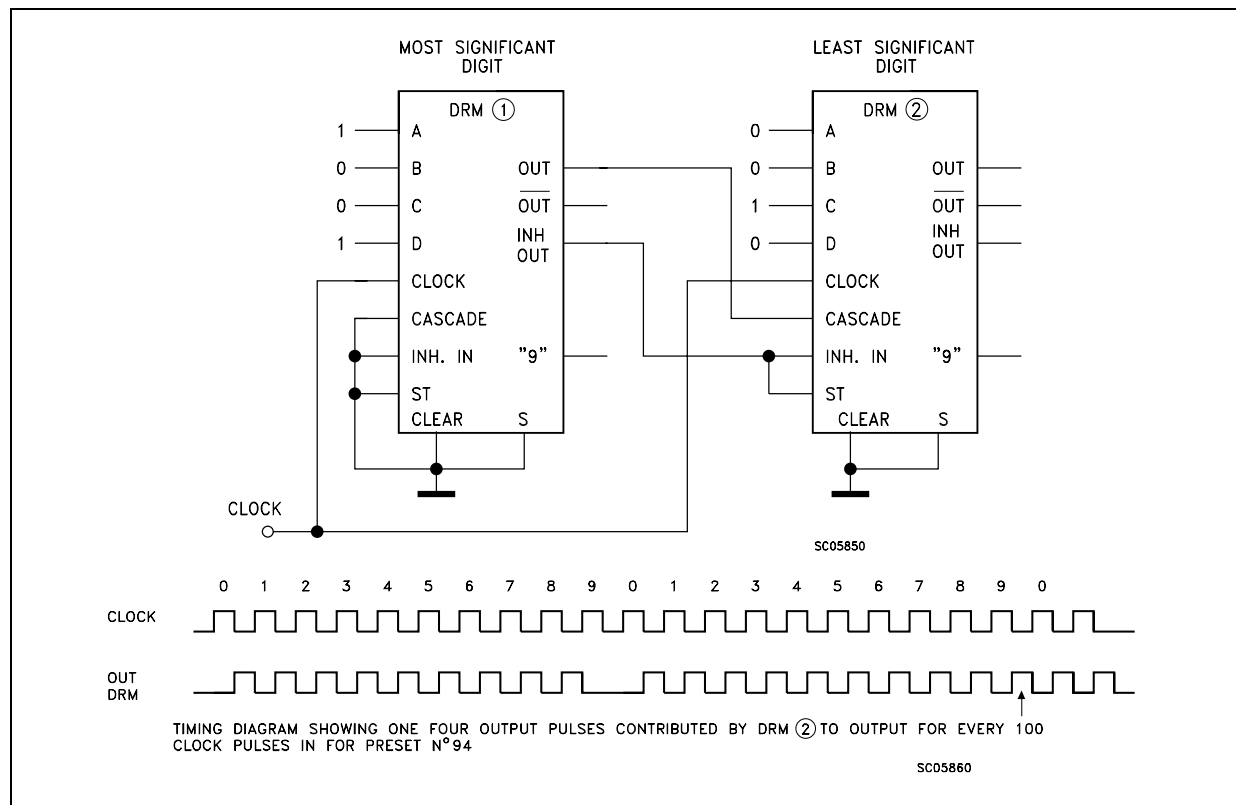
$$f_{OUT2} = \frac{4}{10} f_{OUT1}$$

$$f_{OUT1} = \frac{9}{10} f_{CLOCK}$$

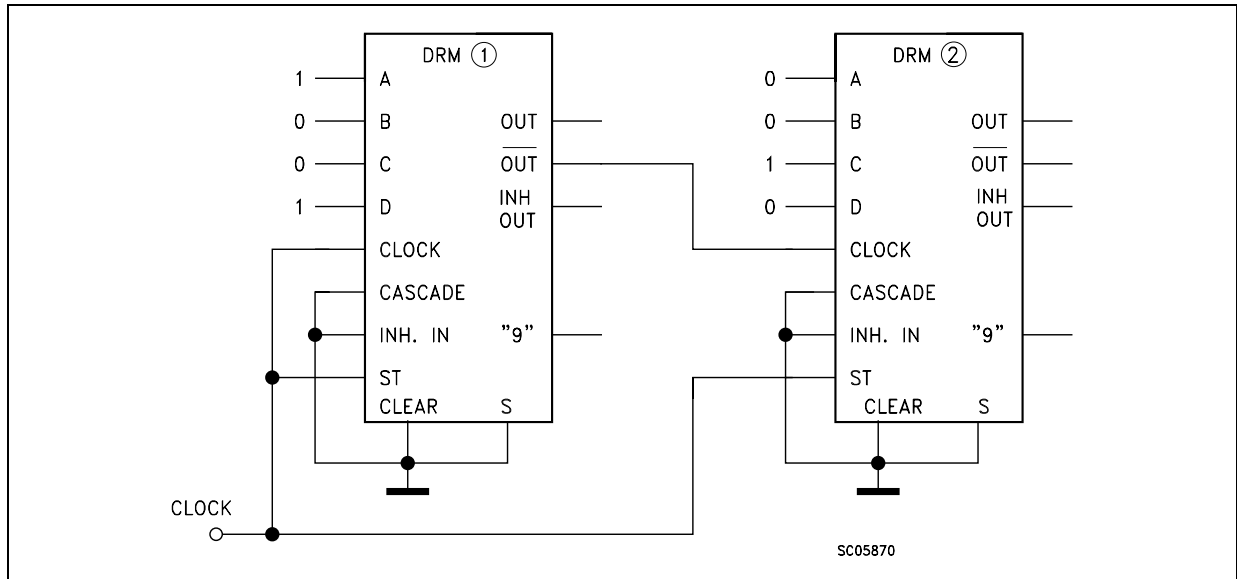
$$f_{OUT2} = \frac{4}{10} \times \left(\frac{9}{10} f_{CLOCK} \right) = \frac{36}{100} f_{CLOCK}$$

Therefore 36 output pulses for every 100 clock input pulses

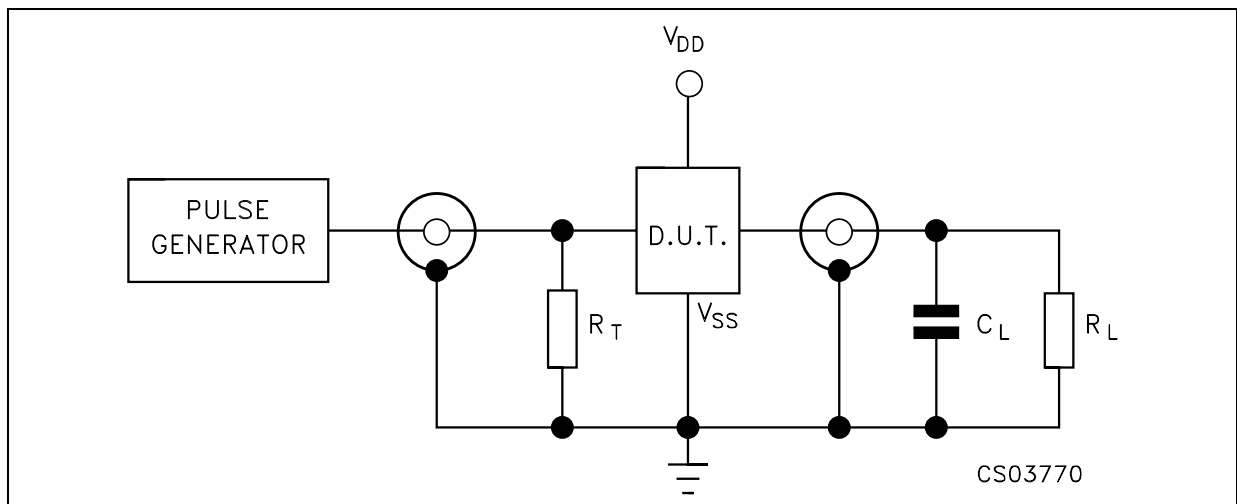
Two HCF4527B Cascaded in the ADD mode with a Preset Number



Two HCF4527B Cascaded in the MULTIPLY Mode with a Preset Number

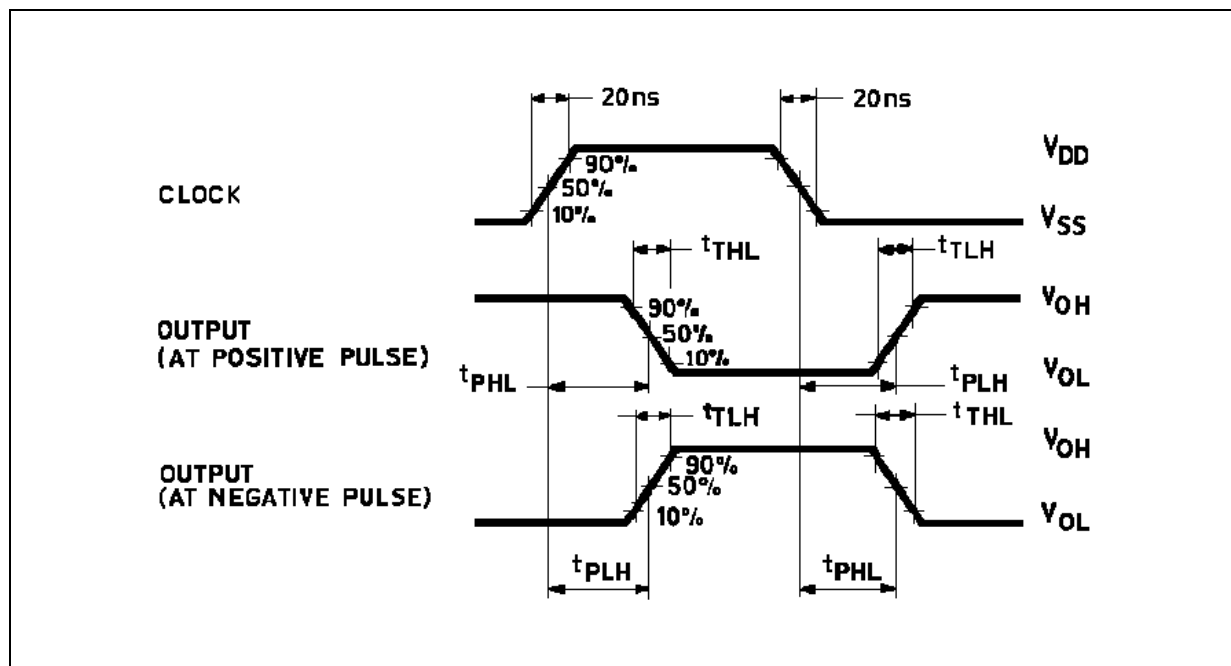


TEST CIRCUIT



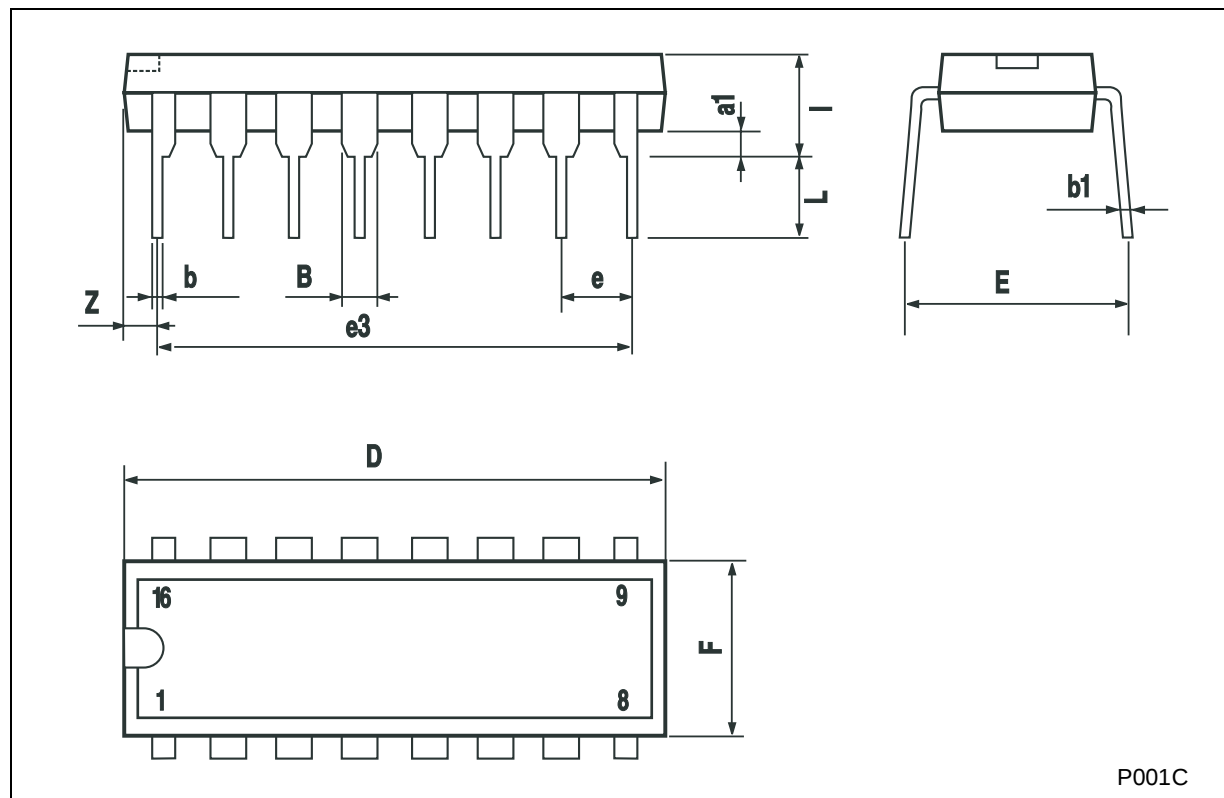
$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{K}\Omega$
 $R_T = Z_{\text{OUT}}$ of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>