



S G S-THOMSON

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

IRF 530/FI-531/FI
IRF 532/FI-533/FI

PRELIMINARY DATA

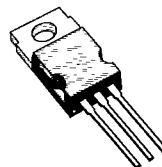
TYPE	V _{DSS}	R _{DS(on)}	I _D ■
IRF530	100 V	0.16 Ω	14 A
IRF530FI	100 V	0.16 Ω	9 A
IRF531	80 V	0.16 Ω	14 A
IRF531FI	80 V	0.16 Ω	9 A
IRF532	100 V	0.23 Ω	12 A
IRF532FI	100 V	0.23 Ω	8 A
IRF533	80 V	0.23 Ω	12 A
IRF533FI	80 V	0.23 Ω	8 A

- 80-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- ULTRA FAST SWITCHING
- EASY DRIVE- FOR REDUCED COST AND SIZE

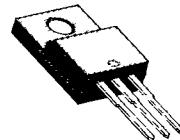
INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

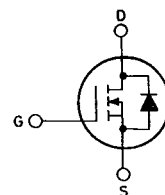
N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power-audio amplifiers and robotics.



TO-220



ISOWATT220

**INTERNAL SCHEMATIC
DIAGRAM****ABSOLUTE MAXIMUM RATINGS**

		TO-220 ISOWATT220		IRF			
				530 530FI	531 531FI	532 532FI	533 533FI
V _{DS} *	Drain-source voltage (V _{GS} = 0)			100	80	100	80
V _{DGR} *	Drain-gate voltage (R _{GS} = 20 KΩ)			100	80	100	80
V _{GS}	Gate-source voltage			±20			
I _{DM} (●)	Drain current (pulsed)			56	56	48	48
I _{DLM}	Drain inductive current, clamped (L = 100 μH)			56	56	48	48
I _D	Drain current (cont.) at T _c = 25°C			530	531	532	533
I _D	Drain current (cont.) at T _c = 100°C			14	14	12	12
I _D ■	Drain current (cont.) at T _c = 25°C			9	9	8	8
I _D ■	Drain current (cont.) at T _c = 100°C			530FI	531FI	532FI	533FI
P _{tot} ■	Total dissipation at T _c < 25°C			9	9	8	8
■	Derating factor			5.5	5.5	5	5
T _{stg}	Storage temperature			TO-220		ISOWATT220	
T _j	Max. operating junction temperature			79	35		
				0.63	0.28		
				-55 to 150			
				150			

* T_j = 25°C to 125°C

(●) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

$R_{thj-case}$	Thermal resistance junction-case	max	1.58	3.57	°C/W
R_{thc-s}	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ for IRF530/532/530FI/532FI for IRF531/533/531FI/533FI	$V_{GS} = 0$	100 80	V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^\circ\text{C}$	250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$		± 100	nA

ON **

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$I_{D(on)}$	On-state drain current	$V_{DS} > I_{D(on)} \times R_{DS(on) max}$ for IRF530/531/530FI/531FI for IRF532/533/532FI/533FI	$V_{GS} = 10 \text{ V}$	14 12			A A
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ for IRF530/531/530FI/531FI for IRF532/533/532FI/533FI	$I_D = 8.3 \text{ A}$			0.16 0.23	Ω Ω

DYNAMIC

$g_{fs} **$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on) max}$ $I_D = 8.3 \text{ A}$	5.1				mho
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$			850		pF
C_{oss}	Output capacitance	$f = 1 \text{ MHz}$			260		pF
C_{rss}	Reverse transfer capacitance	$V_{GS} = 0$			50		pF

SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 36 \text{ V}$	$I_D = 8.0 \text{ A}$			30	ns
t_r	Rise time	$R_l = 15 \Omega$	(see test circuit)			75	ns
$t_{d(off)}$	Turn-off delay time					40	ns
t_f	Fall time					45	ns
Q_g	Total Gate Charge	$V_{GS} = 10 \text{ V}$ $V_{DS} = \text{Max Rating} \times 0.8$ (see test circuit)	$I_D = 14 \text{ A}$			30	nC

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T-39-11

ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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SOURCE DRAIN DIODE

I_{SD}	Source-drain current			14	A
$I_{SDM}^{(*)}$	Source-drain current (pulsed)			56	A
V_{SD}^{**}	Forward on voltage	$I_{SD} = 14\text{ A}$	$V_{GS} = 0$	2.5	V
t_{rr}	Reverse recovery time	$T_J = 150^\circ\text{C}$		360	ns
Q_{rr}	Reverse recovered charge	$I_{SD} = 14\text{ A}$	$di/dt = 100\text{ A}/\mu\text{s}$	21	μC

** Pulsed: Pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

(*) Repetitive Rating: Pulse width limited by max junction temperature

■ See note on ISOWATT220 in this datasheet

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.

ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_J - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)} \text{ (at } 150^\circ\text{C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.

The total thermal resistance $R_{th \text{ (tot)}}$ is the sum of each of these elements.

The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

It is often possible to discern these areas on transient thermal impedance curves.

Fig. 1

