



L4979D L4979MD

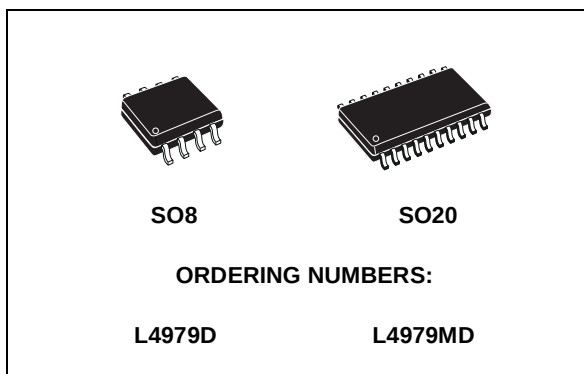
LOW DROP VOLTAGE REGULATOR

PRODUCT PREVIEW

- OPERATING DC SUPPLY VOLTAGE RANGE
6V TO 31V
- TRANSIENT SUPPLY VOLTAGE UP TO 40V
- LOW QUIESCENT CURRENT CONSUMPTION
LESS THAN 20 μ A WITH ENABLE LOW
- HIGH PRECISION OUTPUT VOLTAGE (2%)
- LOW DROPOUT VOLTAGE LESS THAN 0.5V
- RESET CIRCUIT SENSING THE OUTPUT
VOLTAGE DOWN TO 1V
- PROGRAMMABLE RESET PULSE DELAY
WITH EXTERNAL CAPACITOR
- WATCHDOG
- PROGRAMMABLE WATCHDOG TIMER WITH
EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT
CIRCUIT PROTECTION
- WIDE TEMPERATURE RANGE ($T_J = -40^{\circ}\text{C}$ TO
150 $^{\circ}\text{C}$)

DESCRIPTION

L4979 is a family of low dropout linear regulators with microprocessor control functions such as power on reset, low voltage reset, watchdog timer, on-off control or Enable. In addition, only low value ceramic capacitor is



required for stability (above or equal to 100nF).

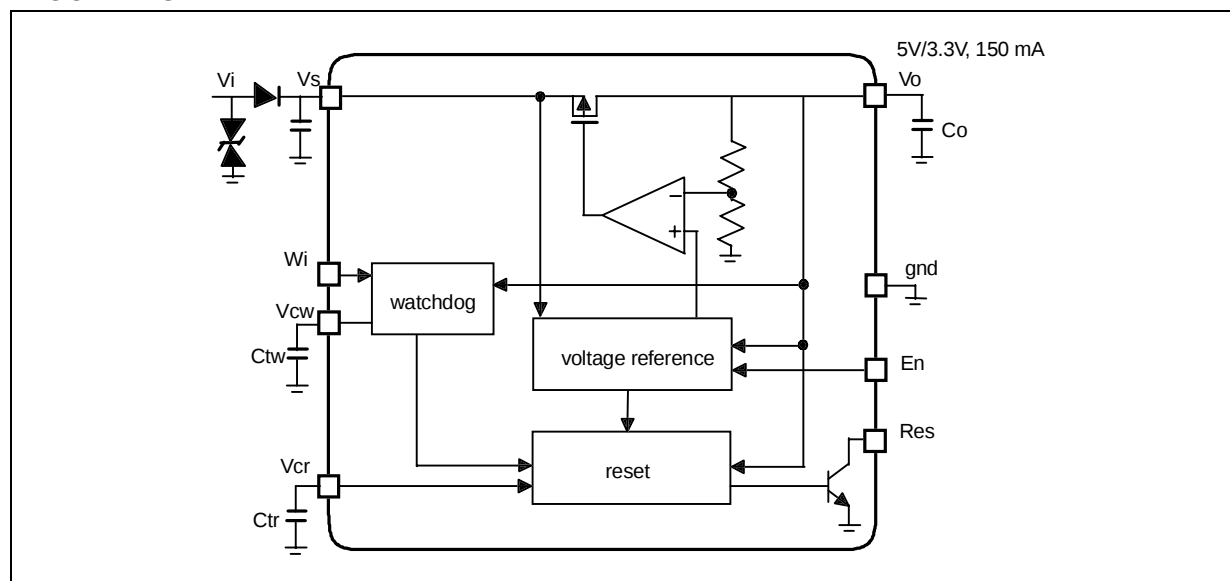
Maximum quiescent current is 20 μ A at all output current equal 0 and enable low.

Typical quiescent current is 1.5mA at output current equal to 5mA, 3mA at output current equal to 150mA, and drops to 10mA in "not enabled" mode.

On chip trimming results in high output voltage accuracy (2%). Accuracy is kept over wide temperature range, line variation, load variation.

The maximum input voltage is 40V. The maximum output current is 200mA. Output current is internally limited. Internal temperature protection disables voltage regulator at overtemperature.

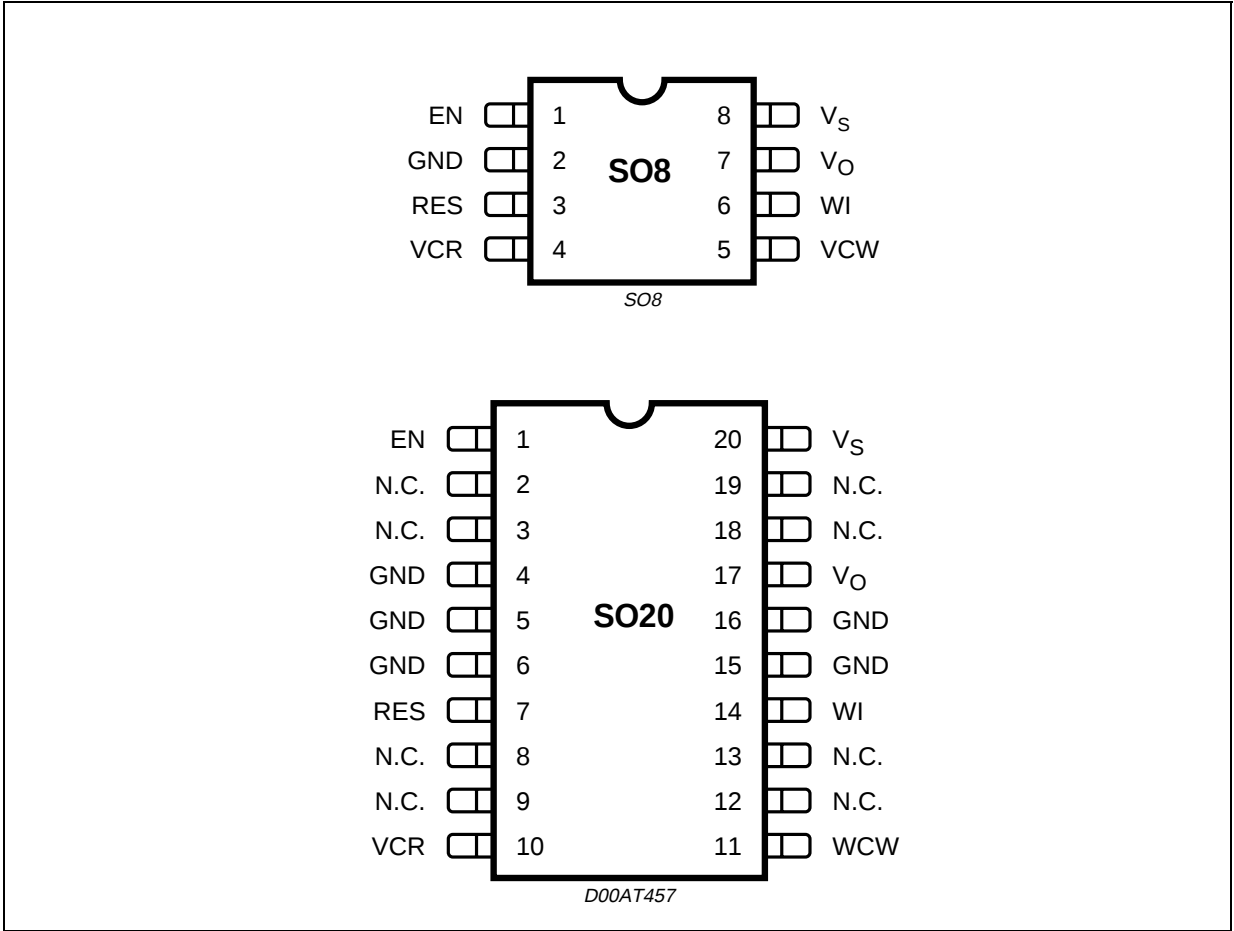
BLOCK DIAGRAM



PIN FUNCTION

SO8 N°	SO20 N°	Pin Name	Function
1	1	En	Voltage regulator enable
2	4, 5, 6, 15, 16	gnd	ground
3	7	Res	Reset output
4	10	Vcr	Reset timing adjust
5	11	Vcw	Watchdog timer adjust
6	14	Wi	Watchdog input
7	17	Vo	Voltage regulator output
8	20	Vs	Supply voltage
	2, 3, 8, 9, 12, 13, 18, 19	N. C.	not connected

PINS CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{vsdc}	DC operating supply voltage	31	V
V _{vstr}	Transient operating supply voltage (t<400ms)	-0.3 to 40	V
I _{vsdc}	Input current	internally limited	
V _{vo}	DC output voltage	-0.3 to 5.5	V
I _{vo}	DC output current	internally limited	
V _{wi}	Watchdog input voltage	-0.3 to 7	V
V _{od}	Open drain output voltage (RES)	-0.3 to 7	V
I _{od}	Open drain output current (RES)	internally limited	
V _{cr}	Reset delay voltage	-0.3 to 7	V
V _{cw}	Watchdog delay voltage	-0.3 to 7	V
V _{en}	Enable input voltage	-0.3 to 40	V
T _j	Junction temperature	-40 to 150	°C
VESD	ESD voltage level (HBM-MIL STD 883C)	+/- 2	kV

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-amb}	Thermal resistance Junction to Ambient (SO8)	130-180	°C/W
R _{th j-amb}	Thermal resistance Junction to Ambient (SO12+4+4)	50 (*)	°C/W

(*) with 6 sq. cm on board heat sink

ELECTRICAL CHARACTERISTICS

(V_S = 5.6V to 31V, T_j = -40°C to +150°C unless otherwise specified)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL							
V _S , V _O	I _q	Quiescent current	V _S = 13.5V, I _O =150mA, enable high all I/O currents=0		3	6	mA
V _S , V _O	I _q	Quiescent current	V _S = 13.5V, I _O = 0mA, enable high all I/O currents = 0		1.5	3	mA
V _S , V _O	I _q	Quiescent current	V _S = 13.5V, I _O = 0mA, enable low all I/O currents = 0			20	μA
	T _w	Thermal protection temperature		150		190	°C
	T _{w_hy}	Thermal protection temperature hysteresis			10		°C

ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
5V VOLTAGE REGULATOR							
V _O	V _{O_ref}	Output voltage	V _S = 5.6 to 31V I _O = 1 to 150mA	4.90	5.00	5.10	V
V _O	I _{lim}	Output current limitation	V _S = 13.5V	200	300	400	mA
V _S , V _O	V _{line}	Line regulation voltage	V _S = 5.6 to 31V I _O = 1 to 150mA			25	mV
V _O	V _{load}	Load regulation voltage	I _O = 1 to 150mA			25	mV
V _S , V _O	V _{dp}	Drop voltage	I _O = 150mA		300	500	mV
V _S , V _O	SVR	Ripple rejection	f _r = 100 Hz	55			dB
3.3V VOLTAGE REGULATOR							
V _O	V _{O_ref}	Output voltage	V _S = 5.6 to 31V I _O = 1 to 150mA	3.23	3.30	3.37	V
V _O	I _{lim}	Output current limitation	V _S = 13.5V	200	300	400	mA
V _S , V _O	V _{line}	Line regulation voltage	V _S = 5.6 to 31V I _O = 1 to 150mA			25	mV
V _S , V _O	V _{dp}	Drop voltage	I _O = 150mA		500	1000	mV
V _O	V _{load}	Load regulation voltage	I _O = 1 to 150mA			25	mV
V _S , V _O	SVR	Ripple rejection	f _r = 100 Hz	55			dB
RESET (5V)							
R _{es}	V _{res_l}	Reset output low voltage	R _{ext} = 5kΩ to V _O , V _O > 1V			0.4	V
R _{es}	I _{res_h}	Reset output high leakage current	V _{res} = 5V			1	μA
R _{es}	R _{p_u}	Pull up internal resistance	with respect to V _O	15	30	50	kΩ
R _{es}	V _{O_th}	V _O out of regulation threshold	V _S = 5.6 to 31V I _O = 1 to 150mA	6% below V _{O_ref}	8% below V _{O_ref}	10% below V _{O_ref}	
V _{cr}	V _{rhth}	Reset timing high threshold	V _S = 13.5V	10% V _{O_ref}	13% V _{O_ref}	16% V _{O_ref}	
V _{cr}	V _{rlth}	Reset timing low threshold	V _S = 13.5V	44% V _{O_ref}	47% V _{O_ref}	50% V _{O_ref}	
V _{cr}	I _{cr}	Charge current	V _S = 13.5V	8	17.6	30	μA
V _{cr}	I _{dr}	Discharge current	V _S = 13.5V	8	17.6	30	μA
R _{es}	t _{rr}	Reset reaction time	see fig. 2	4	10	30	μs
R _{es}	t _{rd}	Reset pulse delay	V _S = 13.5V, C _{tr} = 1nF	65		150	ms

ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
RESET (3.3V)							
R _{es}	V _{res_l}	Reset output low voltage	R _{ext} = 5kΩ to V _O , V _O > 1V			0.4	V
R _{es}	I _{res_h}	Reset output high leakage current	V _{res} = 5V			1	μA
R _{es}	R _{p_u}	Pull up internal resistance	with respect to V _O	15	30	50	kΩ
R _{es}	V _{O_th}	V _O out of regulation threshold	V _S = 5.6 to 31V I _O = 1 to 150mA	6% below V _{O_ref}	8% below V _{O_ref}	10% below V _{O_ref}	
V _{cr}	V _{rhth}	Reset timing high threshold	V _S = 13.5V	10% V _{O_ref}	13% V _{O_ref}	16% V _{O_ref}	
V _{cr}	V _{rlth}	Reset timing low threshold	V _S = 13.5V	44% V _{O_ref}	47% V _{O_ref}	50% V _{O_ref}	
V _{cr}	I _{cr}	Charge current	V _S = 13.5V	8	17.6	30	μA
V _{cr}	I _{dr}	Discharge current	V _S = 13.5V	8	17.6	30	μA
R _{es}	t _{rr}	Reset reaction time	see fig. 2	3	7.5	20	μs
R _{es}	t _{rd}	Reset pulse delay	V _S = 13.5V, C _{tr} = 1nF	40	65	100	ms
WATCHDOG (5V)							
W _i	V _{ih}	Input high voltage	V _S = 13.5V	3.5			V
W _i	V _{il}	Input low voltage	V _S = 13.5V			1.5	V
W _i	V _{ih}	Input hysteresis	V _S = 13.5V		100		mV
W _i	I _i	Pull down current	V _S = 13.5V		10		μA
V _{cw}	V _{whth}	High threshold	V _S = 13.5V	2.20	2.35	2.50	V
V _{cw}	V _{wlth}	Low threshold	V _S = 13.5V	0.50	0.65	0.80	V
V _{cw}	I _{cwc}	Charge current	V _S = 13.5V, V _{cw} = 0.1V	4	8	14	μA
V _{cw}	I _{cwd}	Discharge current	V _S = 13.5V, V _{cw} = 2.5V	1.0	2.13	4.5	μA
V _{cw}	T _{wop}	Watchdog period	V _S = 13.5V, C _{tw} = 47nF	20	48	80	ms
R _{es}	t _{wol}	Watchdog output low time	V _S = 13.5V, C _{tw} = 47nF	5	10	18	ms
WATCHDOG (3.3V)							
W _i	V _{ih}	Input high voltage	V _S = 13.5V	2.3			V
W _i	V _{il}	Input low voltage	V _S = 13.5V			1	V
W _i	V _{ih}	Input hysteresis	V _S = 13.5V		50		mV
W _i	I _i	Pull down current	V _S = 13.5V		10		μA

ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{cw}	V _{whth}	Watchdog timing high threshold	V _S = 13.5V	1.45	1.55	1.65	V
V _{cw}	V _{wlth}	Watchdog timing low threshold	V _S = 13.5V	0.30	0.45	0.55	V
V _{cw}	I _{cwc}	Charge current	V _S = 13.5V, V _{cw} = 0.1V	4	8	14	μA
V _{cw}	I _{cwd}	Discharge current	V _S = 13.5V, V _{cw} = 2.5V	1.0	2.13	4.5	μA
V _{cw}	T _{wop}	Watchdog period	V _S = 13.5V, C _{tw} = 47nF	13	32	54	ms
R _{es}	t _{wol}	Watchdog output low time	V _S = 13.5V, C _{tw} = 47nF	3.0	6.5	11.0	ms
ENABLE (5V)							
E _n	V _{en_l}	Enable input low voltage		2.1			V
E _n	V _{en_h}	Enable input high voltage				3.4	V
E _n	V _{en_hy}	Enable input hysteresis		0.25			V
E _n	I _{leak}	Pull down current	E _n = 5V	5	20	40	μA
ENABLE (3.3V)							
E _n	V _{en_l}	Enable input low voltage		2.0			V
E _n	V _{en_h}	Enable input high voltage				2.7	V
E _n	V _{en_hy}	Enable input hysteresis		0.2			V
E _n	I _{leak}	Pull down current	E _n = 5V	5	20	40	μA

VOLTAGE REGULATOR

Voltage regulator uses a pchannel transistor as a regulating element. With this structure very low dropout voltage at current up to 150mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. A short circuit protection to GND is provided.

RESET

The reset circuit supervises the output voltage V_O. The V_{O_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{O_th} then Res goes low with a reaction time t_{rr}. If the output voltage becomes lower than 2.0V (typ) then Res goes immediately low. The reset low signal is guaranteed for an output voltage V_O greater than 1V.

When the output voltage becomes higher than V_{O_th} then Res goes high with a delay t_{rd}. This delay is obtained by an internal oscillator. Oscillator period is given by

$$T_{osc} = \frac{[(V_{rhth} - V_{rlth}) \cdot C_{tr}]}{I_{cr}} + \frac{[(V_{rhth} - V_{rlth}) \cdot C_{tr}]}{I_{cd}}$$

where:

I_{cr} is an internally generated charge current,

I_{cd} is an internally generated discharge current,

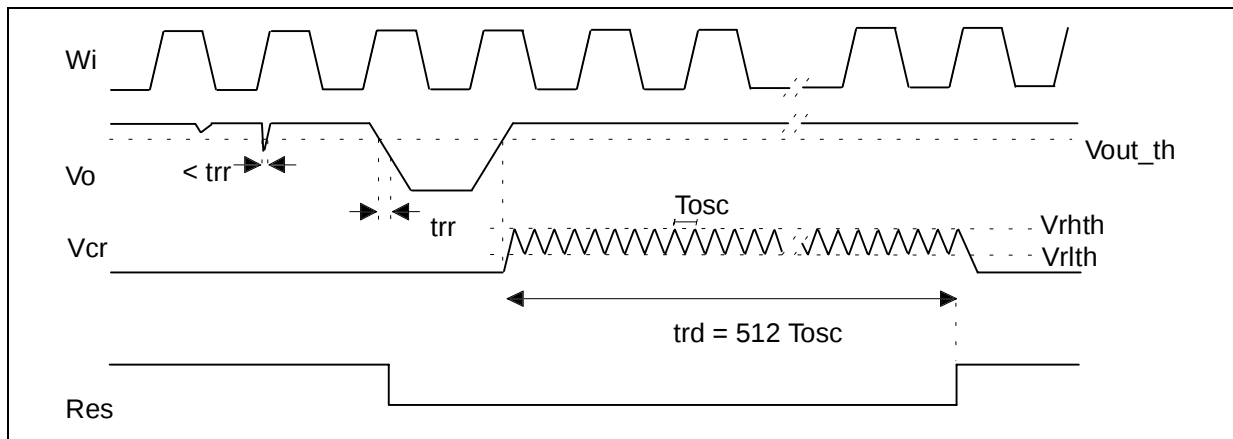
V_{rhth} and V_{rlth} are two voltages defined with the output voltage and a resistor output divider,

C_{tr} is an external capacitance,

t_{rd} is given by

$$t_{rd} = 512 \times T_{osc}$$

Figure 1. Reset Time Diagram.



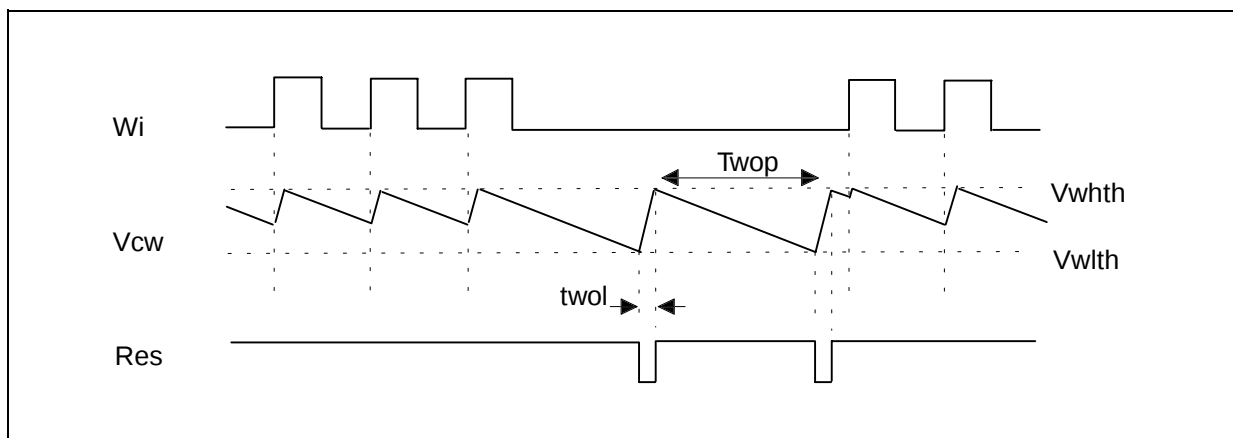
WATCHDOG

A connected microcontroller is monitored by the watchdog input W_i . If pulses are missing, the watchdog output W_o is set to low. The pulse sequence time can be set within a wide range with the external capacitor C_{tw} . The watchdog circuit discharges the capacitor C_{tw} with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t during which the microcontroller must output the positive edge the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every W_i positive edge switches the current source from discharging to charging, the same happens when the lower threshold is reached. When the voltage reaches the upper threshold V_{whth} the current switches from charging to discharging. The result is a sawtooth voltage at the watchdog timer capacitor C_{tw} .

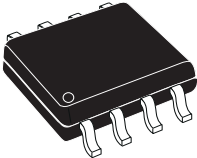
Figure 2. Watchdog time diagram



L4979MD L4979D

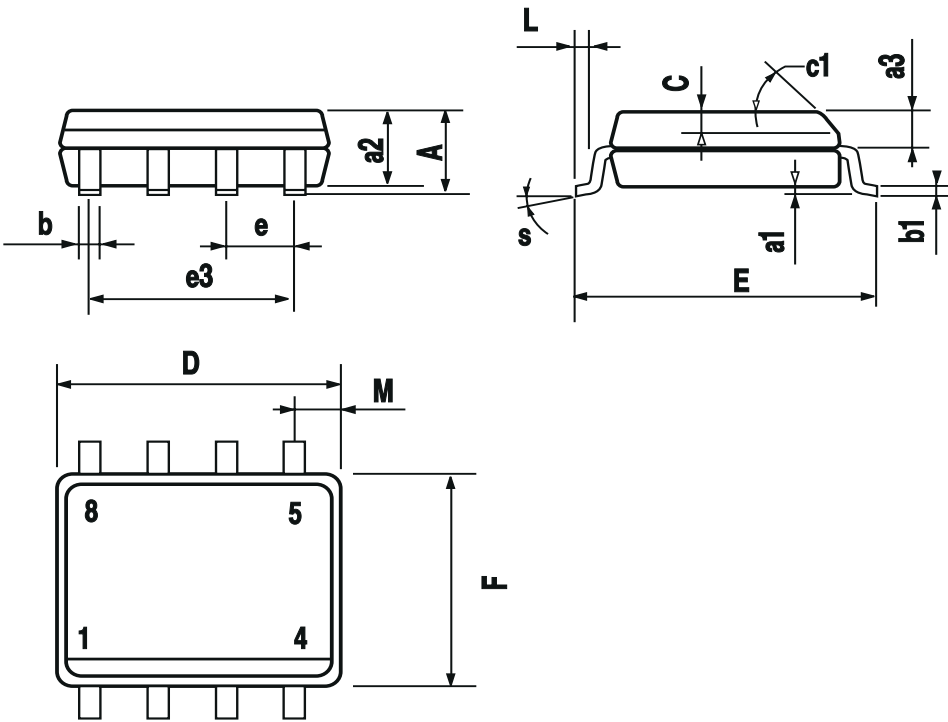
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

**OUTLINE AND
MECHANICAL DATA**



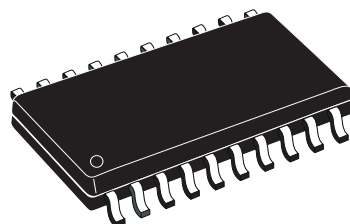
SO8

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).

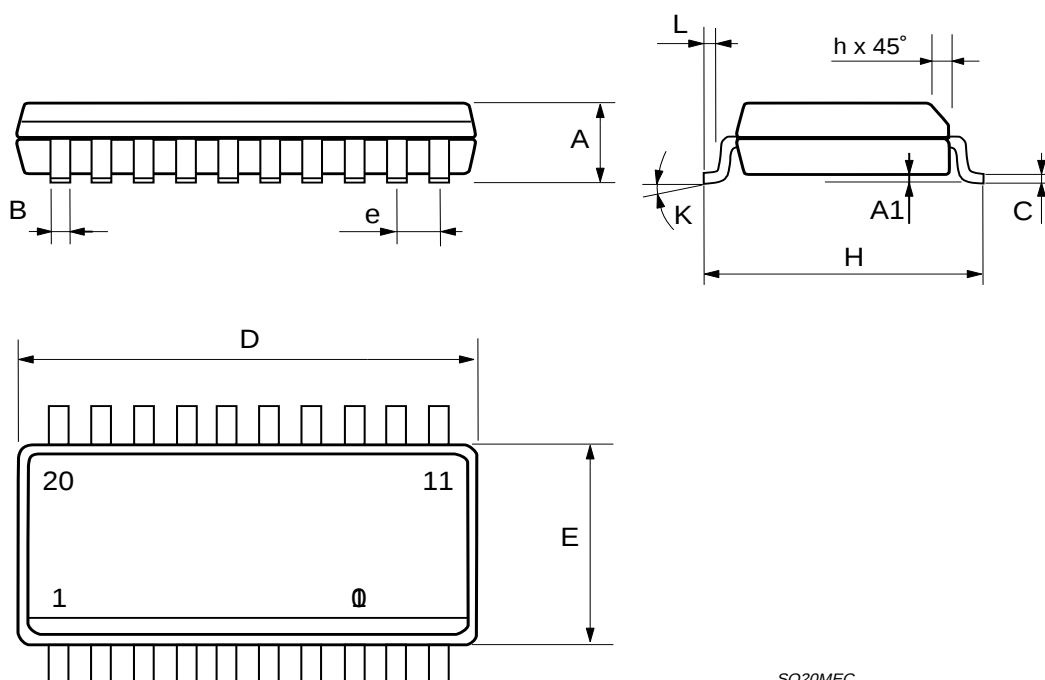


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

OUTLINE AND MECHANICAL DATA



SO20



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