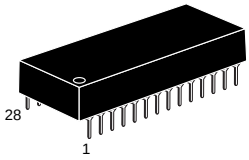
M48Z08
M48Z18

5V, 64 Kbit (8Kb x 8) ZEROPOWER® SRAM

FEATURES SUMMARY

- INTEGRATED, ULTRA LOW POWER SRAM and POWER-FAIL CONTROL CIRCUIT
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
  - M48Z08: V_{CC} = 4.75 to 5.5V
    $4.5V \leq V_{PFD} \leq 4.75V$
  - M48Z18: V_{CC} = 4.5 to 5.5V
    $4.2V \leq V_{PFD} \leq 4.5V$
- SELF-CONTAINED BATTERY IN THE CAPHAT™ DIP PACKAGE
- PIN and FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K x 8 SRAMs

Figure 1. 28-pin CAPHAT, DIP Package



PCDIP28 (PC)
Battery/Crystal
CAPHAT

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SUMMARY DESCRIPTION

The M48Z08/18 ZEROPOWER® RAM is a 8K x 8 non-volatile static RAM which is pin and functional compatible with the DS1225.

The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

The M48Z08/18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28-pin, 600mil DIP CAPHAT™ houses the M48Z08/18 silicon with a long life lithium button cell in a single package.

Figure 2. Logic Diagram

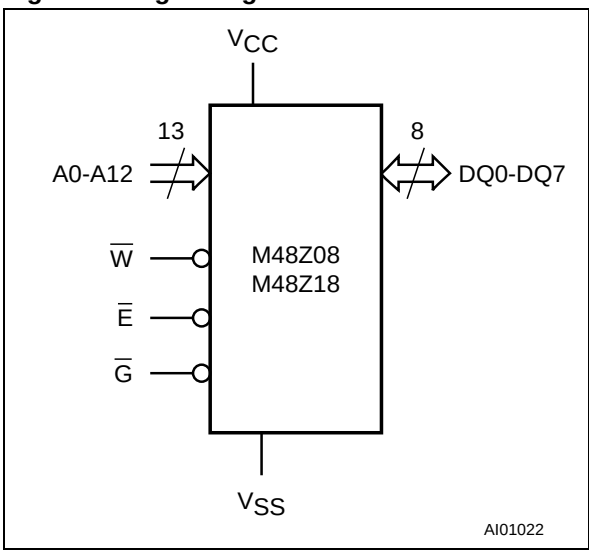


Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	WRITE Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. DIP Connections

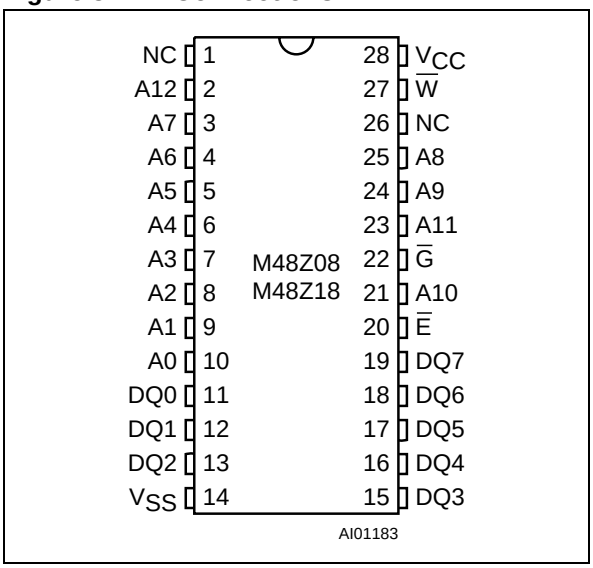
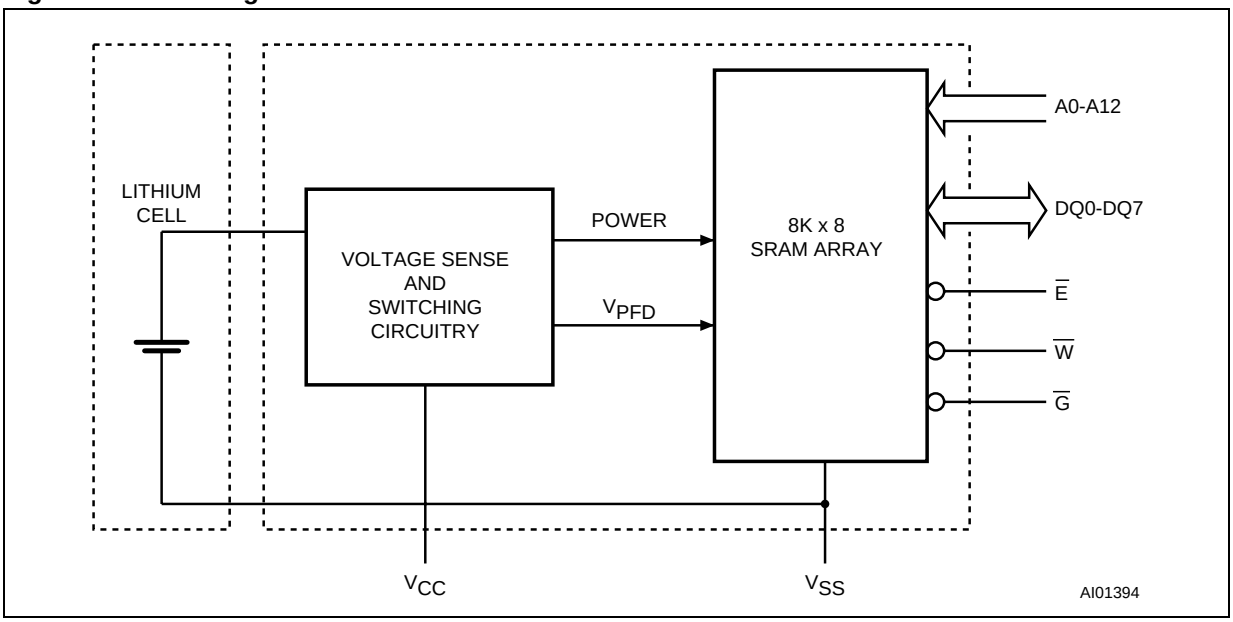


Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
T_{SLD}(1)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: 1. For DIP package: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter	M48Z08	M48Z18	Unit
Supply Voltage (V_{CC})	4.75 to 5.5	4.5 to 5.5	V
Ambient Operating Temperature (T_A)	0 to 70	0 to 70	°C
Load Capacitance (C_L)	100	100	pF
Input Rise and Fall Times	≤ 5	≤ 5	ns
Input Pulse Voltages	0 to 3	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Load Circuit

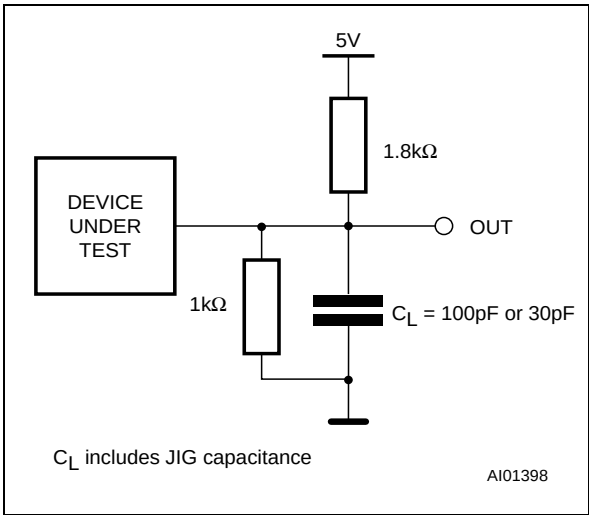


Table 4. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance		10	pF
C_{IO}[3]	Input / Output Capacitance		10	pF

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition(1)	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}(2)	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL}(3)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. Outputs deselected.
3. Negative spikes of –1V allowed for up to 10ns once per Cycle.

OPERATION MODES

The M48Z08/18 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 6. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5V or 4.5 to 5.5V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD}(min)(1)	X	X	X	High Z	CMOS Standby
Deselect	$\le V_{SO}$(1)	X	X	X	High Z	Battery Back-up Mode

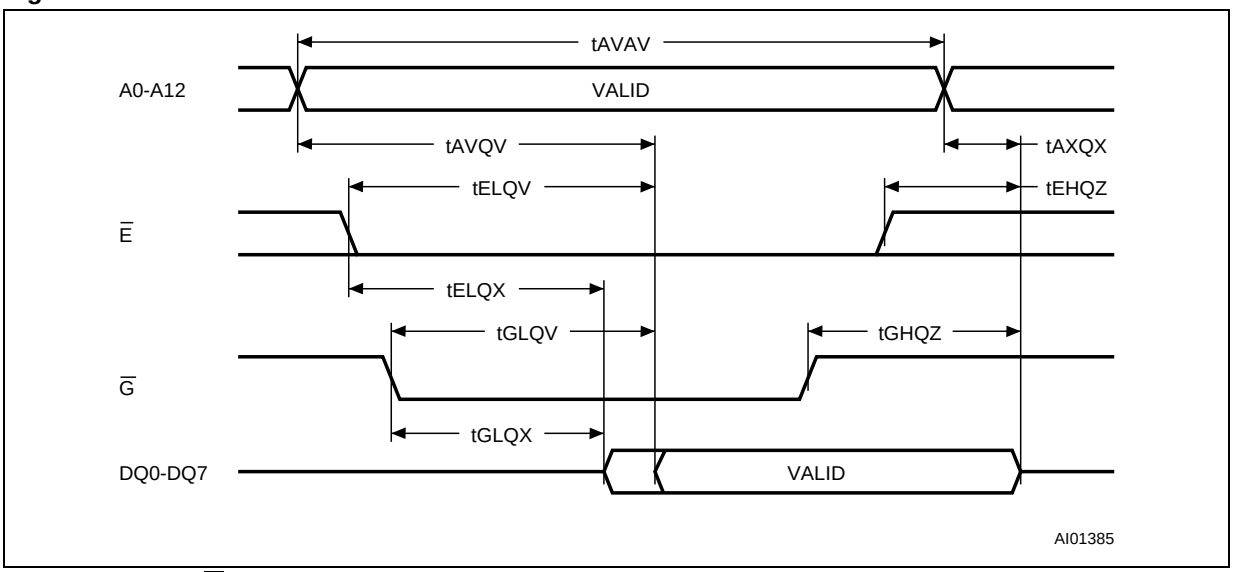
Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.
1. See Table 10, page 11 for details.

READ Mode

The M48Z08/18 is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access time (t_{ELQV}) or Output Enable Access time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 6. READ Mode AC Waveforms



Note: WRITE Enable ($\overline{W}$) = High.

Table 7. READ Mode AC Characteristics

Symbol	Parameter[1]	M48Z08/M48Z18		Unit
		Min	Max	
t_{AVAV}	READ Cycle Time	100		ns
t_{AVQV}	Address Valid to Output Valid		100	ns
t_{ELQV}	Chip Enable Low to Output Valid		100	ns
t_{GLQV}	Output Enable Low to Output Valid		50	ns
t_{ELQX}[2]	Chip Enable Low to Output Transition	10		ns
t_{GLQX}[2]	Output Enable Low to Output Transition	5		ns
t_{EHQZ}[2]	Chip Enable High to Output Hi-Z		50	ns
t_{GHQZ}[2]	Output Enable High to Output Hi-Z		40	ns
t_{AXQX}	Address Transition to Output Transition	5		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. C_L = 30pF.

WRITE Mode

The M48Z08/18 is in the WRITE Mode whenever W and E are active. The start of a WRITE is referenced from the latter occurring falling edge of W or E.

A WRITE is terminated by the earlier rising edge of W or E. The addresses must be held valid throughout the cycle. E or W must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. G should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on E and G, a low on W will disable the outputs t_{WLQZ} after W falls.

Figure 7. WRITE Enable Controlled, WRITE Mode AC Waveform

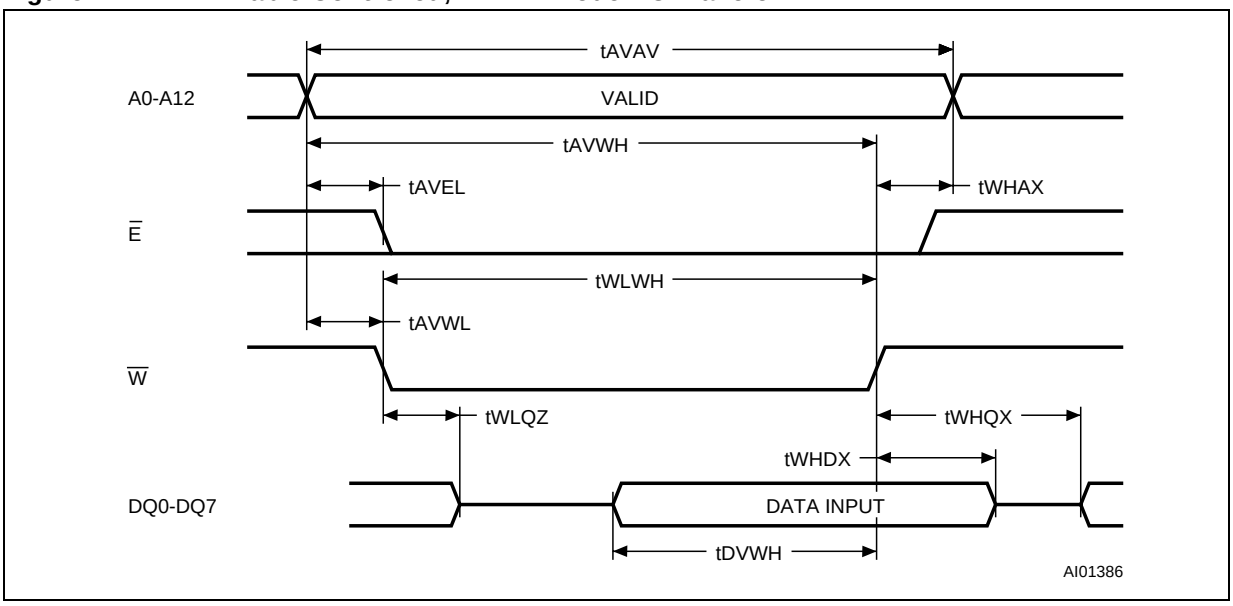


Figure 8. Chip Enable Controlled, WRITE Mode AC Waveforms

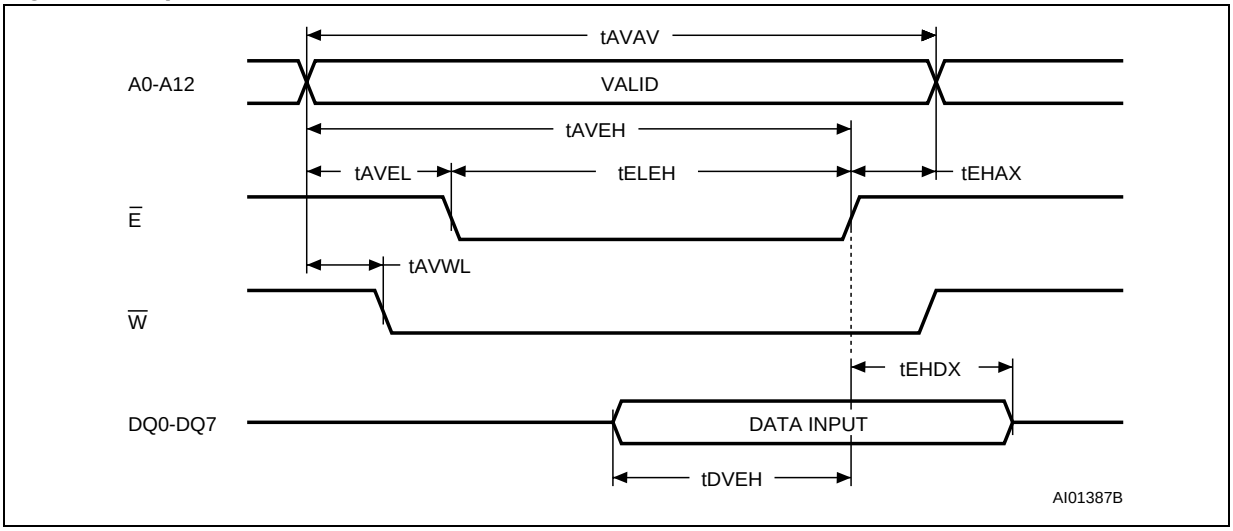


Table 8. WRITE Mode AC Characteristics

Symbol	Parameter[1]	M48Z08/M48Z18		Unit
		Min	Max	
t_{AVAV}	WRITE Cycle Time	100		ns
t_{AVWL}	Address Valid to WRITE Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable 1 Low	0		ns
t_{WLWH}	WRITE Enable Pulse Width	80		ns
t_{ELEH}	Chip Enable Low to Chip Enable 1 High	80		ns
t_{WHAX}	WRITE Enable High to Address Transition	10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		ns
t_{DVWH}	Input Valid to WRITE Enable High	50		ns
t_{DVEH}	Input Valid to Chip Enable 1 High	30		ns
t_{WHDX}	WRITE Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ}[2,3]	WRITE Enable Low to Output Hi-Z		50	ns
t_{AVWH}	Address Valid to WRITE Enable High	80		ns
t_{AVEH}	Address Valid to Chip Enable High	80		ns
t_{WHQX}[2,3]	WRITE Enable High to Output Transition	10		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. C_L = 30pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Data Retention Mode

With valid V_{CC} applied, the M48Z08/18 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

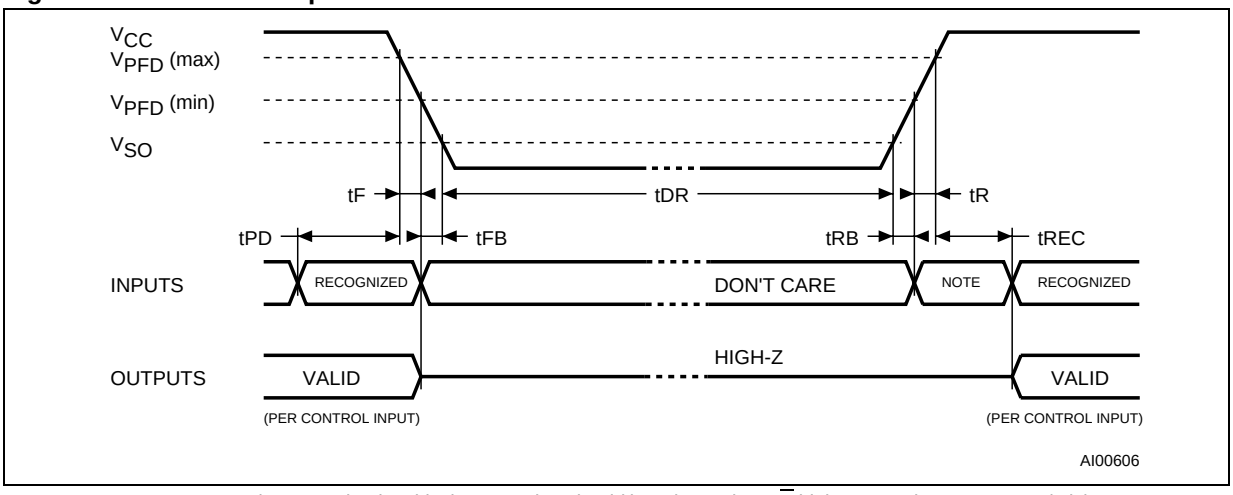
Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z08/18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z08/18 for an accumulated period of at least 11 years when V_{CC} is less than V_{SO}.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{REC} (min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD} (min) to prevent inadvertent write cycles prior to system stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max).

For more information on Battery Storage Life refer to the Application Note AN1012.

Figure 9. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent WRITE cycles after V_{CC} rises above V_{PFD} (min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system is running.

Table 9. Power Down/Up AC Characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} Fall Time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Up	2		ms

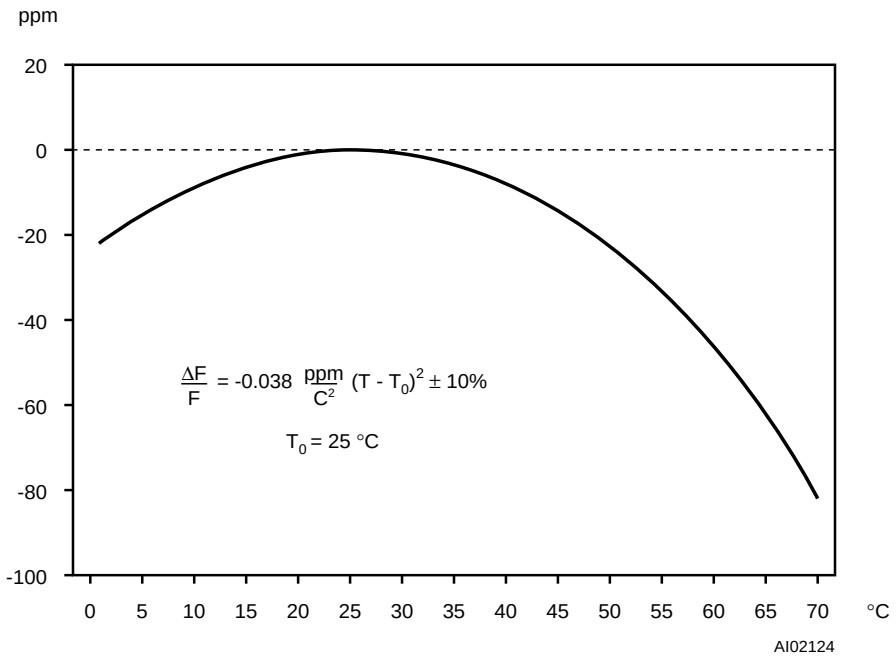
Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than tF may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 10. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter[1,2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	M48Z08	4.5	4.6	4.75	V
		M48Z18	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage			3.0		V
t_{DR}	Expected Data Retention Time		11			YEARS

Note: 1. All voltages referenced to V_{SS}.
2. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5V or 4.5 to 5.5V (except where noted).

Figure 10. Crystal Accuracy Across Temperature

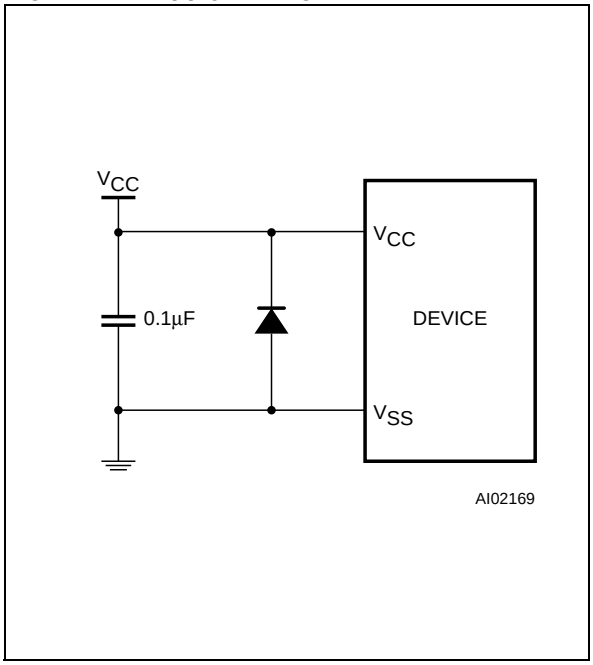


V_{CC} Noise And Negative Going Transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in Figure 11) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 11. Supply Voltage Protection



PART NUMBERING

Table 11. Ordering Information Scheme

Example: M48Z 08 –100 PC 1 TR

Device Type

M48Z

Supply Voltage and Write Protect Voltage

08(1) = V_{CC} = 4.75 to 5.5V; V_{PFD} = 4.5 to 4.75V

18 = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.2 to 4.5V

Speed

–100 = 100ns

Package

PC = PCDIP28

Temperature Range

1 = 0 to 70°C

Shipping Method

blank = Tubes

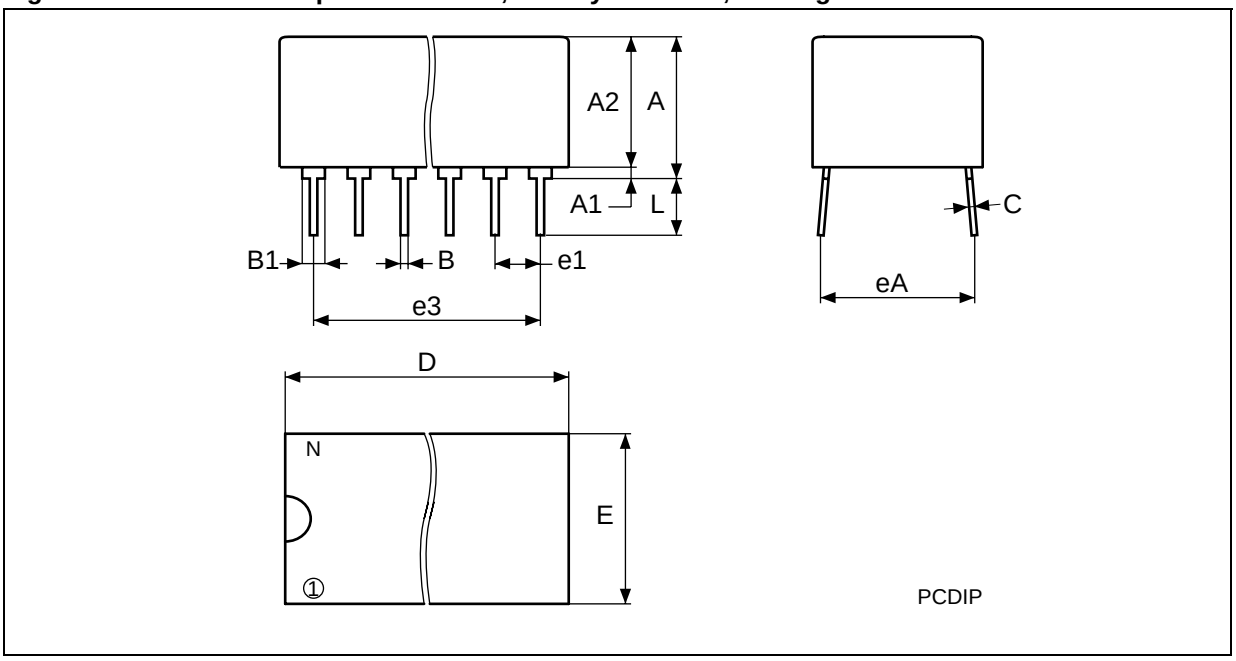
TR = Tape & Reel

Note: 1. The M48Z08/18 part is offered with the PCDIP28 (e.g., CAPHAT™) package only.

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest you.

PACKAGE MECHANICAL INFORMATION

Figure 12. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT, Package Outline



Note: Drawing is not to scale.

Table 12. PCDIP28 – 28-pin Plastic DIP, battery CAPHAT, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

REVISION HISTORY

Table 13. Document Revision History

Date	Rev. #	Revision Details
March 1999	1.0	First issue
07/19/01	2.0	2-socket SOH and 2-pin SH packages removed; reformatted; temperature information added to tables (Table 4, 5, 7, 8, 9, 10)
12/19/01	2.1	Remove all references to “clock”
12/21/01	2.2	Changes to text to reflect addition of M48Z08Y option
05/20/02	2.3	Modify reflow time and temperature footnotes (Table 2)
09/10/02	2.4	Remove all references to “SNAPHAT” and M48Z08Y part (Figure 2; Table 2, 3, 7, 8, 10, 11)