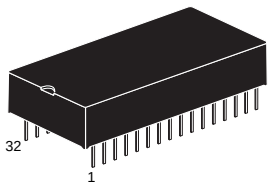
M48Z129Y
M48Z129V

3.3V/5V 1 Mbit (128Kb x8) ZEROPOWER® SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT, and BATTERY
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- MICROPROCESSOR POWER-ON RESET (RESET VALID EVEN DURING BATTERY BACK-UP MODE)
- BATTERY LOW PIN - PROVIDES WARNING OF BATTERY END-OF-LIFE
- WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
  - M48Z129Y: 4.2V ≤ V_{PFD} ≤ 4.5V
  - M48Z129V: 2.7V ≤ V_{PFD} ≤ 3.0V
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS OF DATA RETENTION IN THE ABSENCE OF POWER
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 128Kb x 8 SRAMS
- SELF CONTAINED BATTERY IN DIP PACKAGE



PMDIP32 (PM)
Module

Table 1. Signal Names

A0-A16	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RST}$	Reset Output (Open Drain)
$\overline{BL}$	Battery Low Output (Open Drain)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

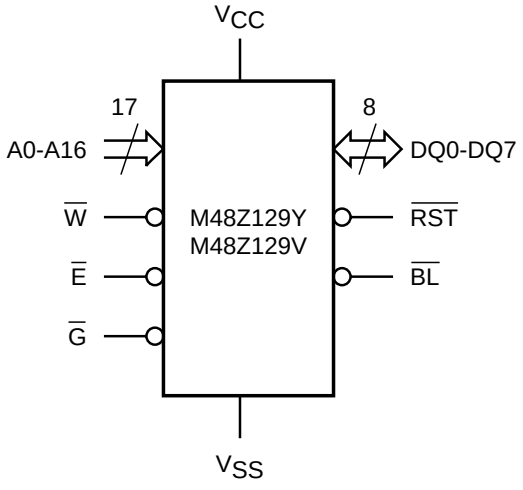


Table 2. Absolute Maximum Ratings (1)

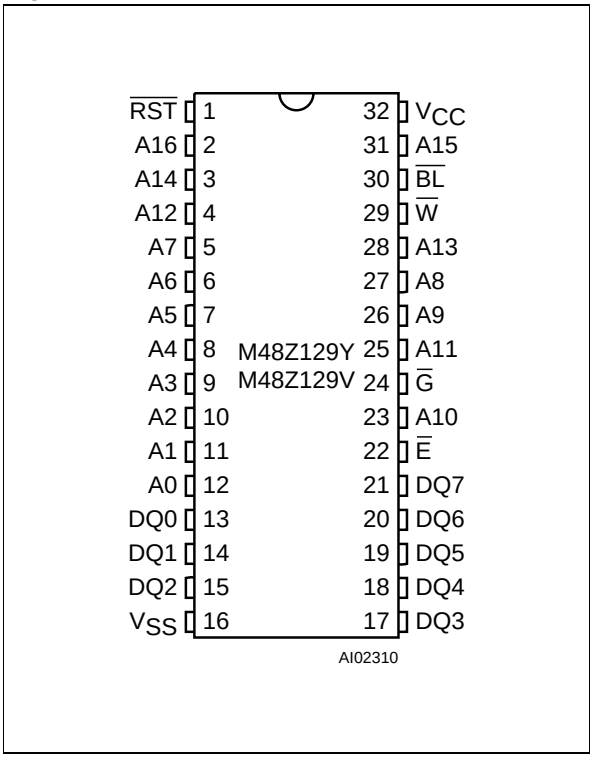
Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)		–40 to 70	°C
T_{BIAS}	Temperature Under Bias		–10 to 70	°C
T_{SLD} (2)	Lead Solder Temperature for 10 seconds		260	°C
V_{IO}	Input or Output Voltages		–0.3 to V_{CC}+0.3	V
V_{CC}	Supply Voltage	M48Z129Y M48Z129V	–0.3 to 7.0 –0.3 to 4.6	V

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

Figure 2A. DIP Pin Connections



DESCRIPTION

The M48Z129Y/V ZEROPOWER SRAM is a 1,048,576 bit non-volatile static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic 32 pin DIP Module. The M48Z129Y/V directly replaces industry standard 128K x 8 SRAM. It also provides the non-volatility of FLASH without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z129Y/V also has its own Power-Fail Detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing data security in the midst of unpredictable system operation. As V_{CC} falls, the control circuitry automatically switches to the battery, maintaining data until valid power is restored.

READ MODE

The M48Z129Y/V is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 17 Address Inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

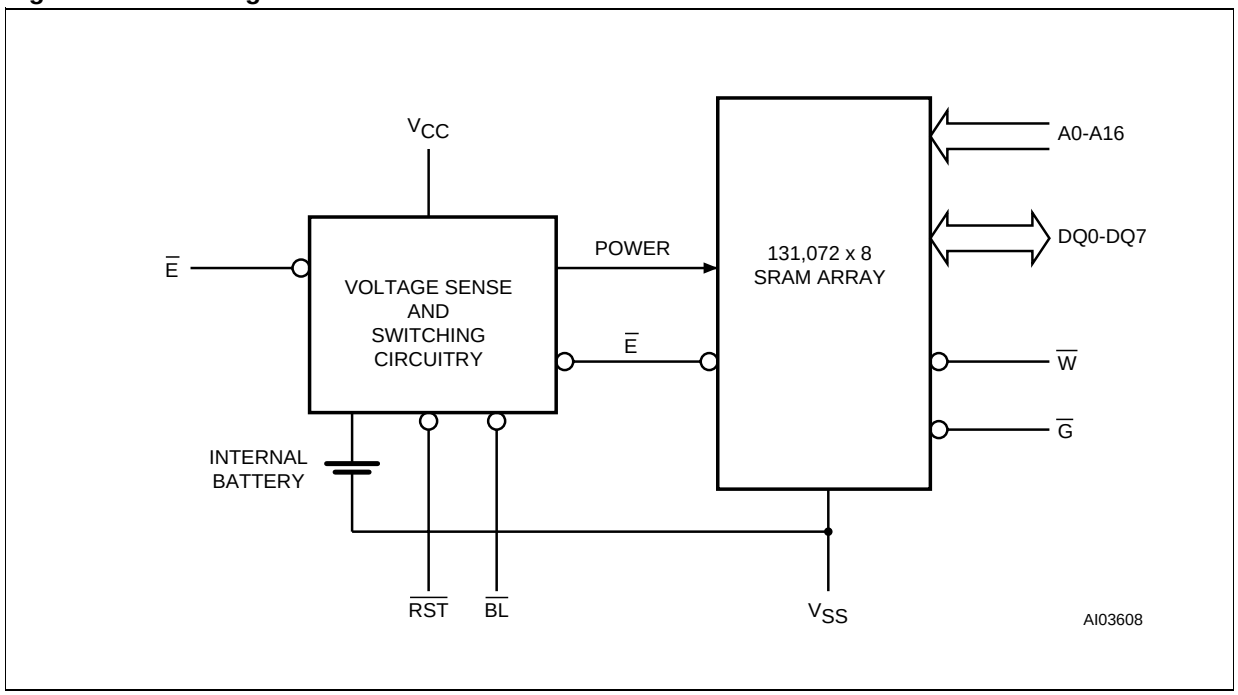
The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V (M48Z129Y) or 3.0V to 3.6V (M48Z129V)	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO} (2)	X	X	X	High Z	Battery Back-up Mode

Note: 1. X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.
2. See Table 7 for details.

Figure 3. Block Diagram



WRITE MODE

The M48Z129Y/V is in the Write Mode whenever $\overline{W}$ (Write Enable) and $\overline{E}$ (Chip Enable) are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z129Y/V operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance and all inputs are treated as “don’t care”.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Note: A power failure during a write cycle may corrupt data at the current addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z129Y/V may respond to transient noise spikes on V_{CC} that cross into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery, preserving data. The internal energy source will maintain data in the M48Z129Y/V for an accumulated period of at least 10 years at room temperature. As system power rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD}(max).

For more information on Battery Storage Life refer to the Application Note AN1012.

POWER-ON RESET OUTPUT

All microprocessors have a reset input which forces them to a known state when starting. The M48Z129Y/V has a reset output ($\overline{RST}$) pin which is guaranteed to be low below V_{PFD}(min). This signal is an open drain configuration. An appropriate pull-up resistor should be chosen to control the rise time. This signal will be valid for all voltage conditions, even when V_{CC} equals V_{SS}. Once V_{CC} exceeds the power failure detect voltage V_{PFD}, an internal timer keeps $\overline{RST}$ low for t_{REC} to allow the power supply to stabilize.

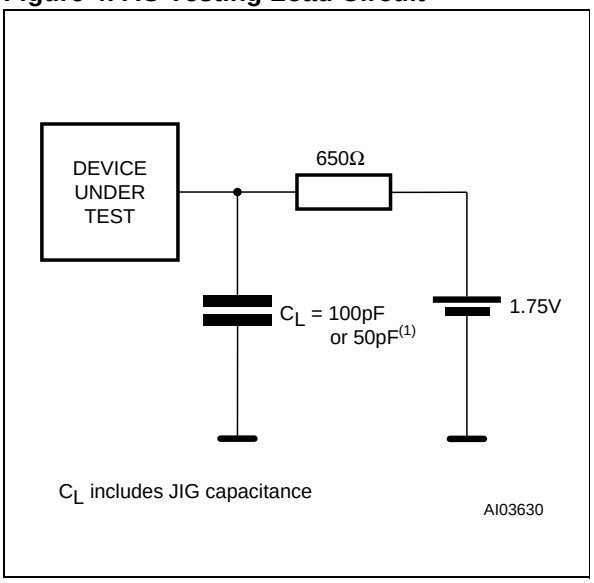
BATTERY LOW PIN

The M48Z129Y/V automatically performs battery voltage monitoring upon power-up, and at factory-programmed time intervals of 24 hours. The Battery Low ($\overline{BL}$) pin will be asserted if the battery voltage is found to be less than approximately 2.5V. If a battery low is generated during a power-up sequence, this indicates that the battery is below 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied.

The M48Z129Y/V only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The $\overline{BL}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control the rise time.

Figure 4. AC Testing Load Circuit



Note: 1. 50pF for M48Z129V (3.3V).

Table 5. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Note: 1. Effective capacitance measured with power supply at 5V.
2. Outputs deselected.

Table 6A. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO} (1)	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply Current	Outputs open		95	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		7	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6B. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 3.0V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO} (1)	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		4	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL}	Input Low Voltage		–0.3	0.6	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.2		V

Note: 1. Outputs deselected.

Table 7. Power Down/Up Trip Points DC Characteristics (1)
(T_A = 0 to 70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z129Y)	4.2	4.35	4.5	V
	Power-fail Deselect Voltage (M48Z129V)	2.7	2.9	3.0	
V_{SO}	Battery Back-up Switchover Voltage (M48Z129Y)		3.0		V
	Battery Back-up Switchover Voltage (M48Z129V)		2.45		
t_{DR} (2)	Expected Data Retention Time	10			YEARS

Note: 1. All voltages referenced to V_{SS}.
2. At 25 °C.

Table 8. Power Down/Up AC Characteristics
(T_A = 0 to 70 °C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SS} V_{CC} Fall Time (M48Z129Y)	10		µs
	V_{PFD} (min) to V_{SS} V_{CC} Fall Time (M48Z129V)	150		
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{WPT}	Write Protect Time (M48Z129Y)	40	150	µs
	Write Protect Time (M48Z129V)	40	250	
t_{REC}	V_{PFD} (max) to $\overline{RST}$ High	40	200	ms

Note: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

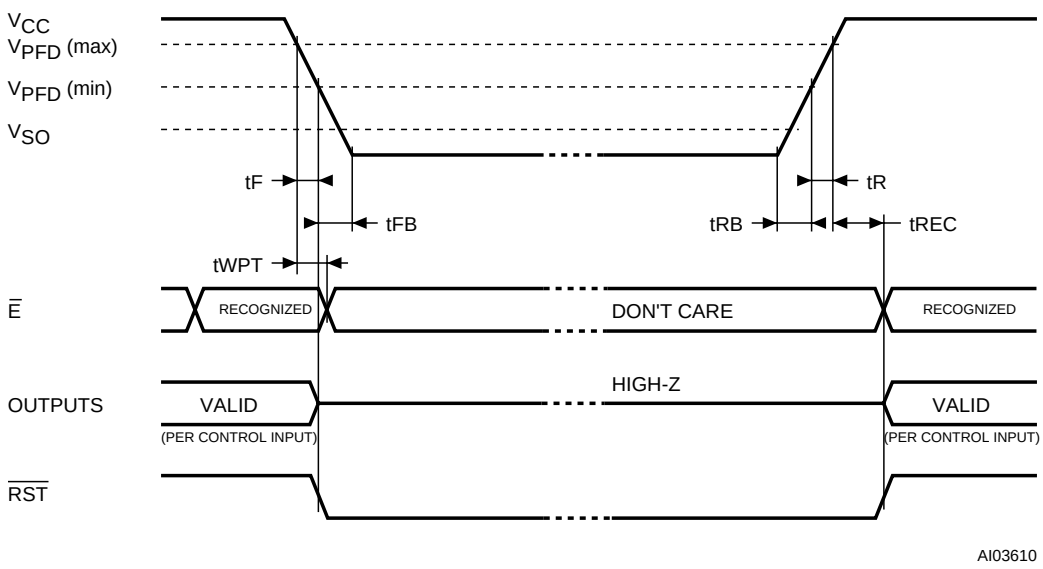
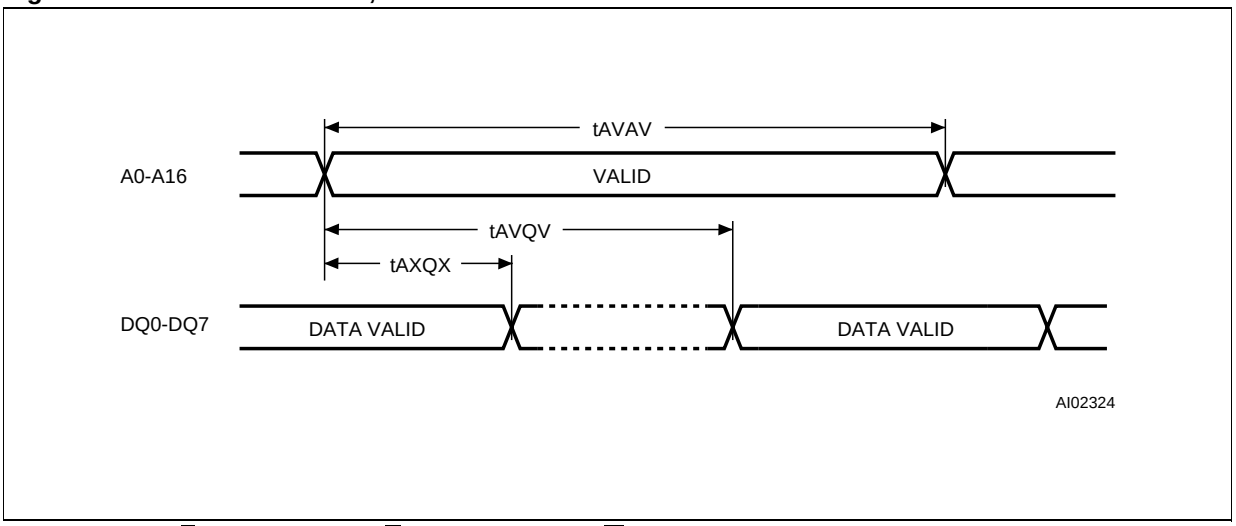


Table 9. Read Mode AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.5V to 5.5V or 3.0V to 3.6V)

Symbol	Parameter	M48Z129Y		M48Z129V		Unit
		-70		-85		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	70		85		ns
t_{AVQV} (1)	Address Valid to Output Valid		70		85	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70		85	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35		45	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	3		5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		30		40	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		20		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	5		5		ns

Note: 1. C_L = 100pF or 50pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Address Controlled, Read Mode AC Waveforms.



Note: Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) = Low, Write Enable ($\overline{W}$) = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveform

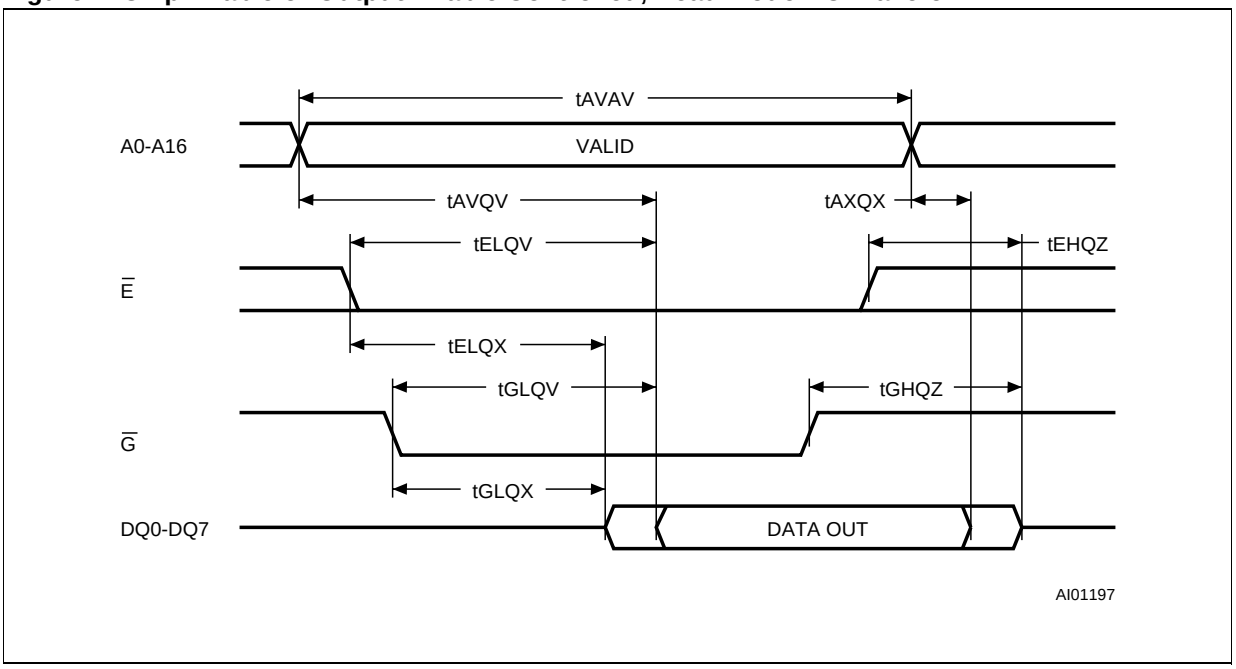


Table 10. Write Mode AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.5V to 5.5V or 3.0V to 3.6V)

Symbol	Parameter	M48Z129Y		M48Z129V		Unit
		-70		-85		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	70		85		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	55		65		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		75		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	30		35		ns
t_{DVEH}	Input Valid to Chip Enable High	30		35		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		15		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25		30	ns
t_{AVWH}	Address Valid to Write Enable High	65		75		ns
t_{AVEH}	Address Valid to Chip Enable High	65		75		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		5		ns

Note: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms

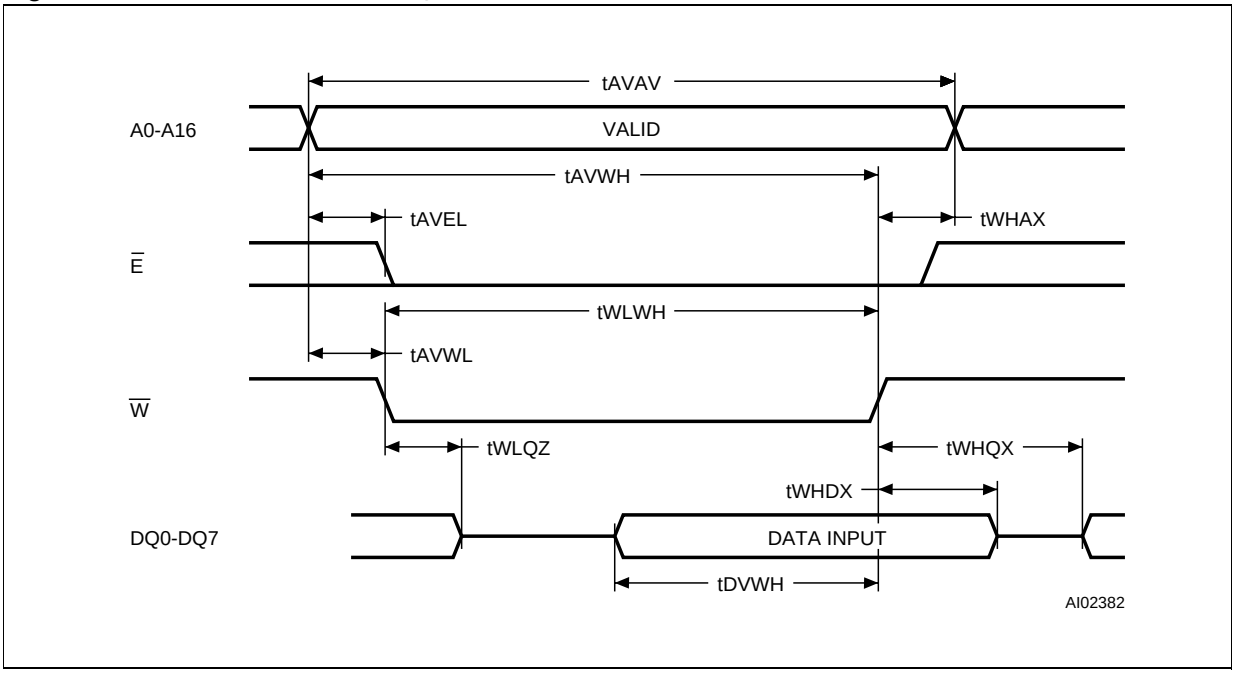


Figure 9. Chip Enable Controlled, Write AC Waveforms

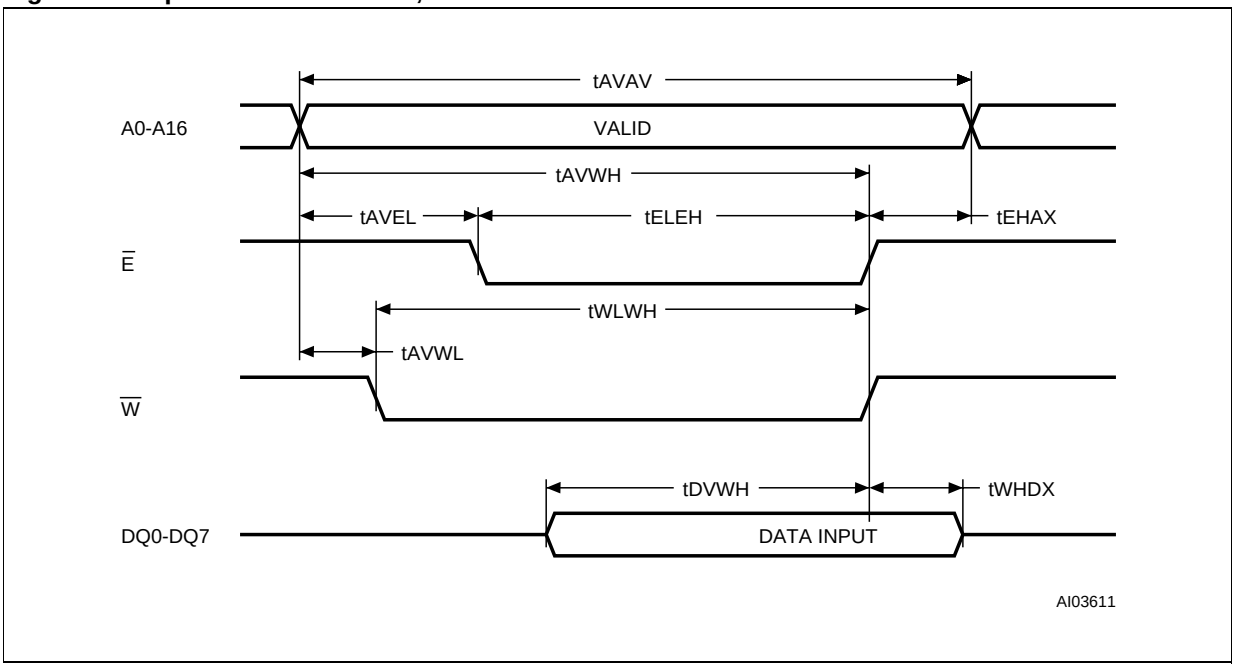
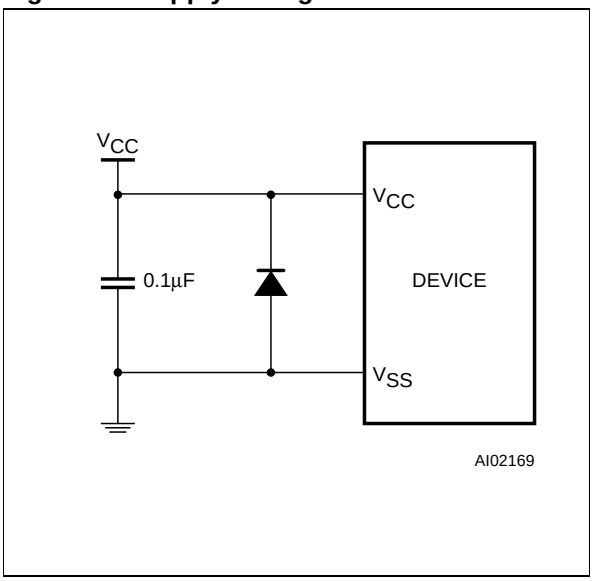


Figure 10. Supply Voltage Protection



POWER SUPPLY DECOUPLING AND UNDERSHOOT PROTECTION

Icc transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 microfarad is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below Vss by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from V_{CC} to Vss (cathode connected to V_{CC}, anode to Vss). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount).

Table 11. Ordering Information Scheme

Example: M48Z129Y -70 PM 1

Supply Voltage and Write Protect Voltage

129Y = V_{CC} = 4.5V to 5.5V; V_{PFD} = 4.2V to 4.5V

129V = V_{CC} = 3.0V to 3.6V; V_{PFD} = 2.7V to 3.0V

Speed

-70 = 70ns (M48Z129Y)

-85 = 85ns (M48Z129V)

Package

PM = PMDIP32

Temperature Range

1 = 0 to 70 °C

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

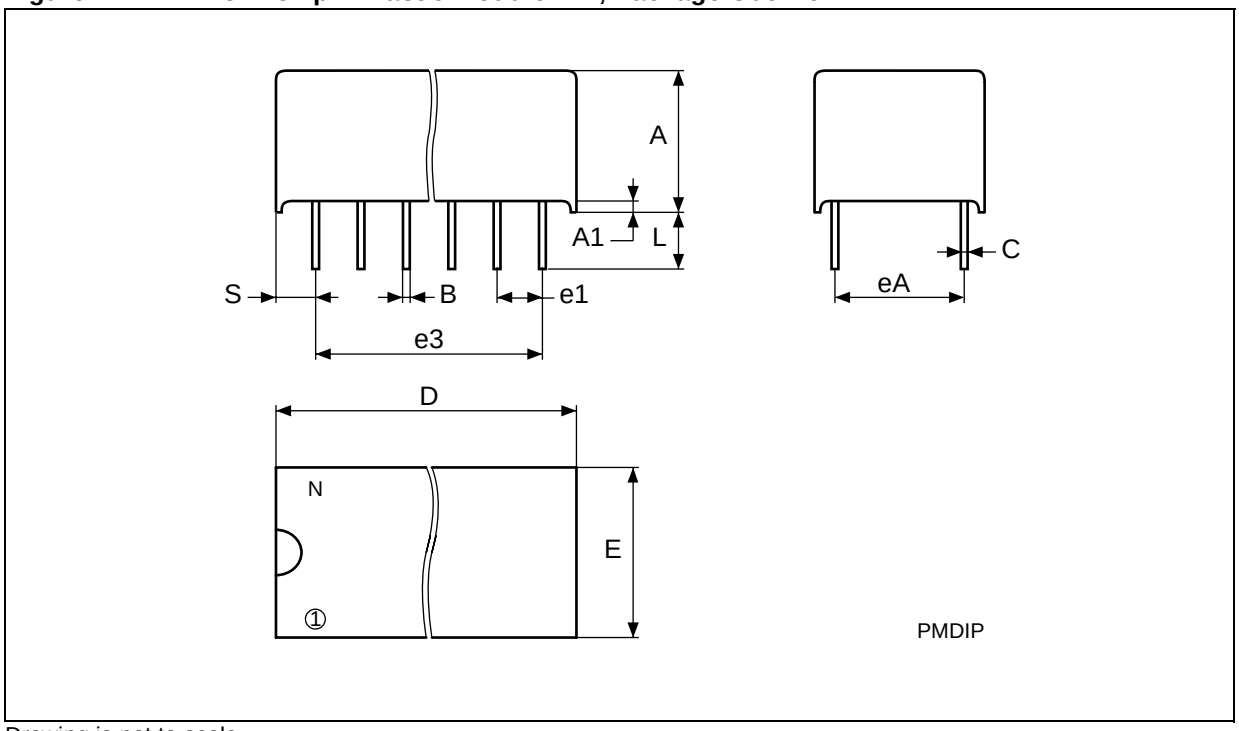
Table 12. Revision History

Date	Revision Details
December 1999	First Issue
03/30/00	From Preliminary Data to Data Sheet
06/20/00	t_{GLQX} changed for M48Z129Y (Table 9)

Table 13. PMDIP32 - 32 pin Plastic Module DIP, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

Figure 11. PMDIP32 - 32 pin Plastic Module DIP, Package Outline



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