



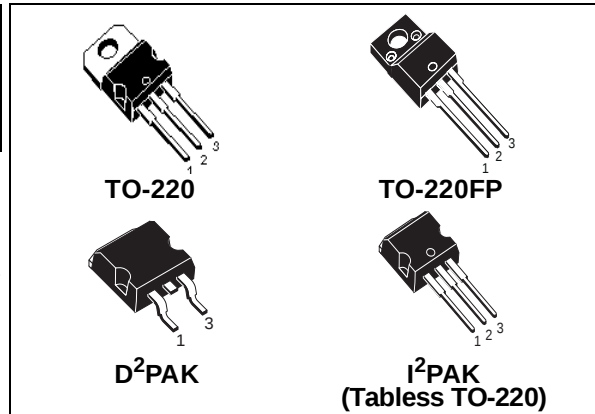
STP12NM50 - STP12NM50FP STB12NM50 - STB12NM50-1

N-CHANNEL 500V - 0.30Ω - 12A TO-220/FP/D²PAK/I²PAK

MDmesh™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP12NM50/FP	500V	<0.35Ω	12 A
STB12NM50	500V	<0.35Ω	12 A
STB12NM50-1	500V	<0.35Ω	12 A

- TYPICAL R_{DS(on)} = 0.30Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

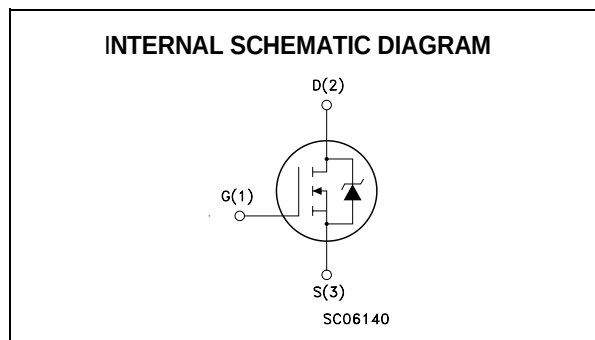


DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP(B)12NM50(-1)	STP12NM50FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500		V
V _{GS}	Gate- source Voltage	±30		V
I _D	Drain Current (continuous) at T _C = 25°C	12	12(*)	A
I _D	Drain Current (continuous) at T _C = 100°C	7.5	7.5(*)	A
I _{DM} (●)	Drain Current (pulsed)	48	48(*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	160	35	W
	Derating Factor	1.28	0.28	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	15		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	--	2500	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(●) Pulse width limited by safe operating area
October 2002

(1) I_{SD} ≤ 12 A, di/dt ≤ 400 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

STP12NM50 - STP12NM50FP - STB12NM50 - STB12NM50-1**THERMAL DATA**

		TO-220 /D ² PAK/ I ² PAK	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case	Max	0.78	3.57
R _{thj-amb} T _I	Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose	Max	62.5 300	°C/W °C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	6	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	400	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)
OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 µA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 6 A		0.30	0.35	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 6A		5.2		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1000		pF
C _{oss}	Output Capacitance			180		pF
C _{rss}	Reverse Transfer Capacitance			25		pF
C _{oss eq.} (2)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 400V		90		pF
R _g	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

STP12NM50 - STP12NM50FP - STB12NM50 - STB12NM50-1

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250\text{ V}$, $I_D = 6\text{ A}$		20		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		10		ns
Q_g	Total Gate Charge	$V_{DD} = 400\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$		28		nC
Q_{gs}	Gate-Source Charge			8		nC
Q_{gd}	Gate-Drain Charge			15		nC

SWITCHING OFF

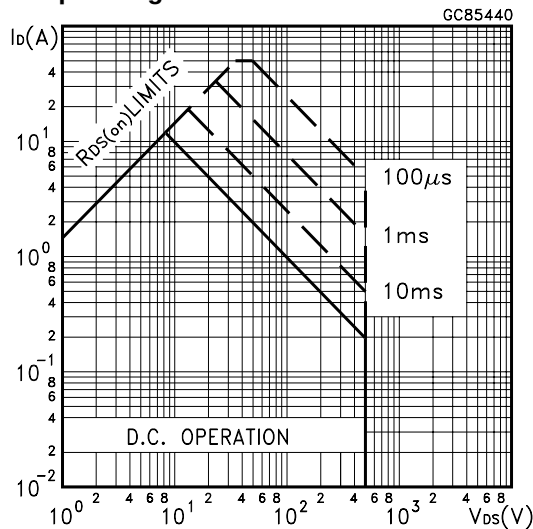
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_r(V_{off})$	Off-voltage Rise Time	$V_{DD} = 400\text{ V}$, $I_D = 12\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		19		ns
t_f	Fall Time			8		ns
t_c	Cross-over Time			18		ns

SOURCE DRAIN DIODE

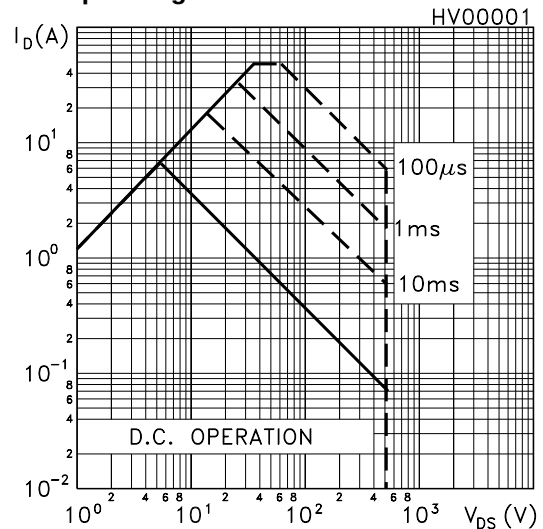
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				12	A
$I_{SDM}(2)$	Source-drain Current (pulsed)				48	A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 25^\circ\text{C}$ (see test circuit, Figure 5)		270		ns
Q_{rr}	Reverse Recovery Charge			2.23		μC
I_{RRM}	Reverse Recovery Current			16.5		A
t_{rr}	Reverse Recovery Time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		340		ns
Q_{rr}	Reverse Recovery Charge			3		μC
I_{RRM}	Reverse Recovery Current			18		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

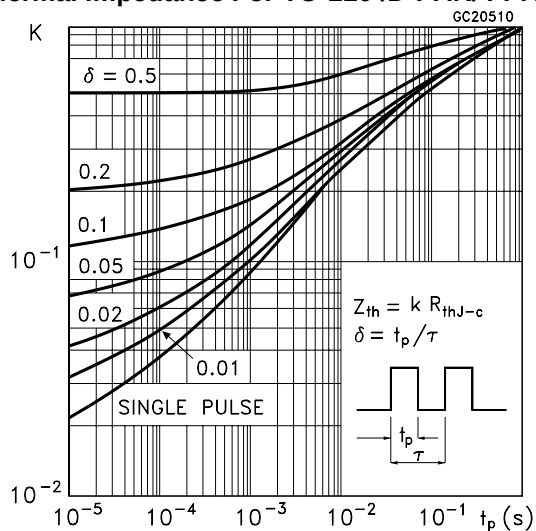
Safe Operating Area For TO-220 / D²PAK/I²PAK



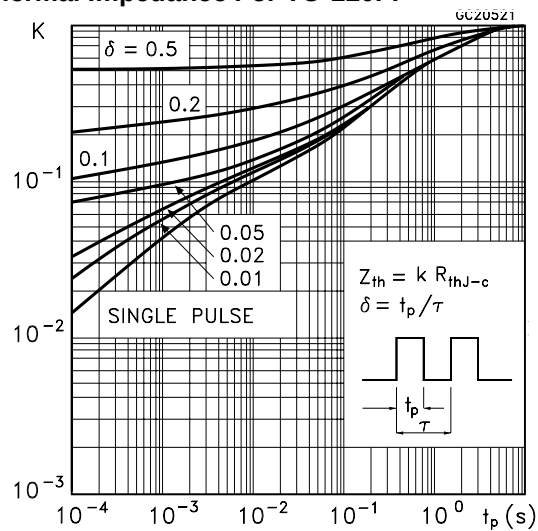
Safe Operating Area For TO-220FP



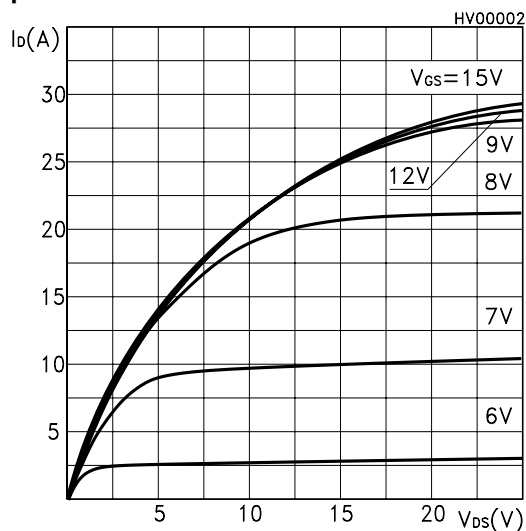
Thermal Impedance For TO-220 /D²PAK/ I²PAK



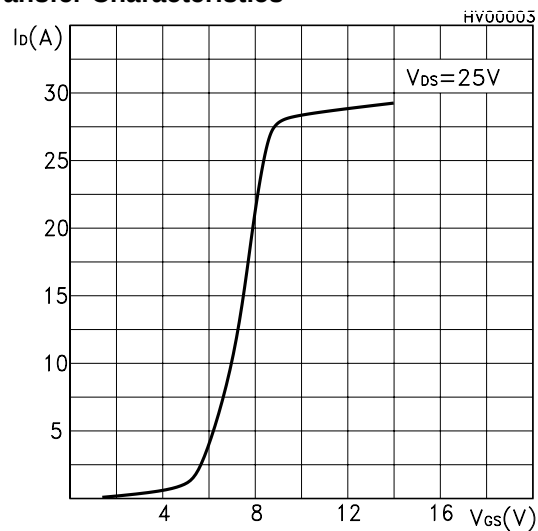
Thermal Impedance For TO-220FP



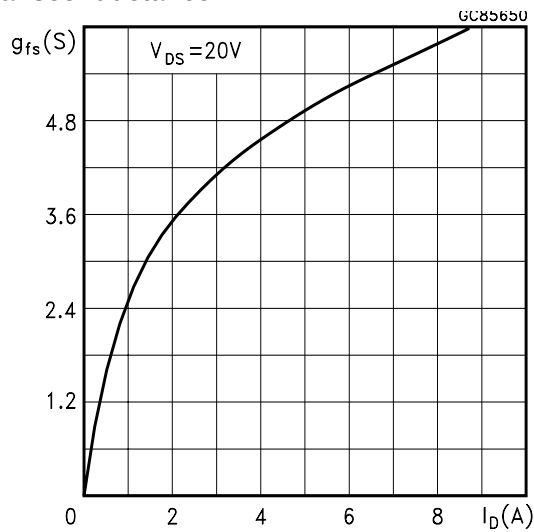
Output Characteristics



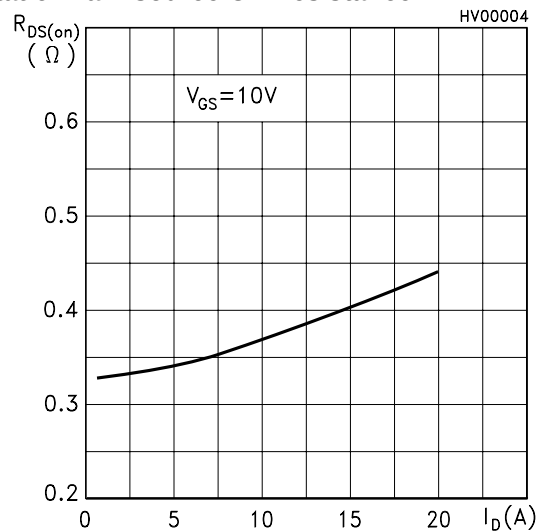
Transfer Characteristics



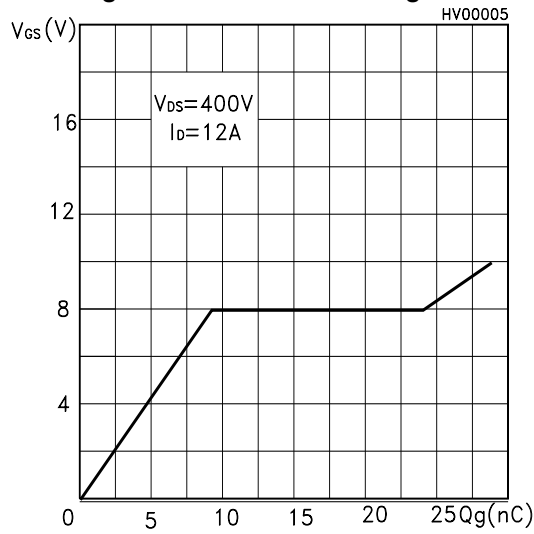
Transconductance



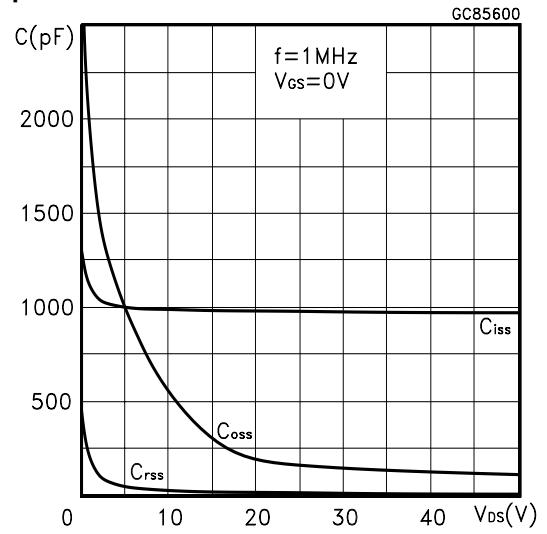
Static Drain-source On Resistance



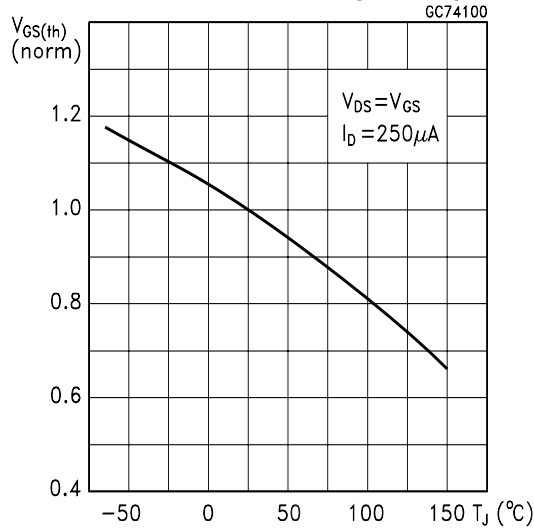
Gate Charge vs Gate-source Voltage



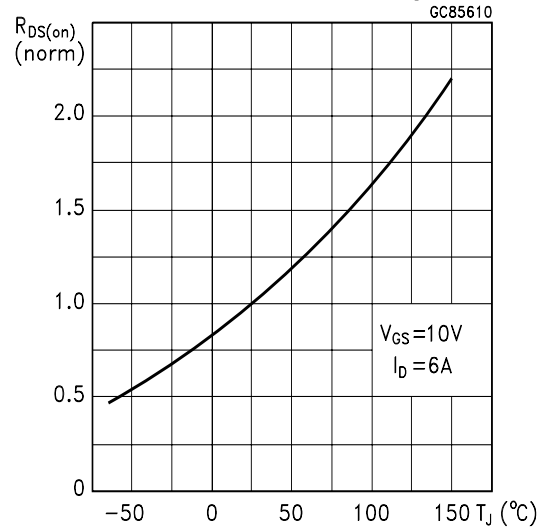
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

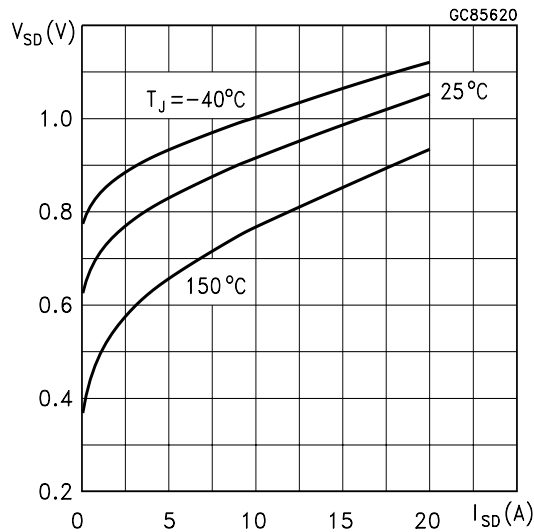


Fig. 1: Unclamped Inductive Load Test Circuit

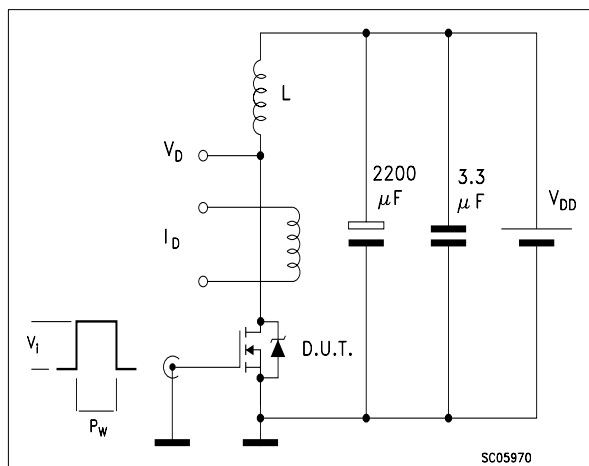


Fig. 2: Unclamped Inductive Waveform

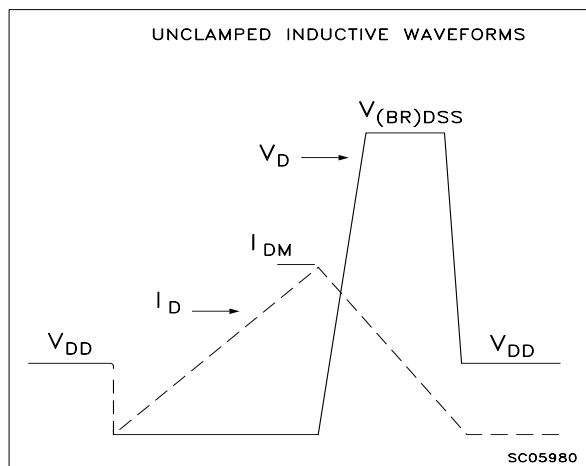


Fig. 3: Switching Times Test Circuits For Resistive Load

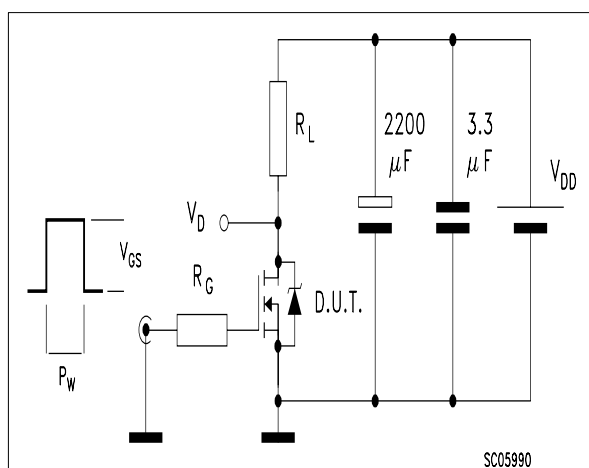


Fig. 4: Gate Charge test Circuit

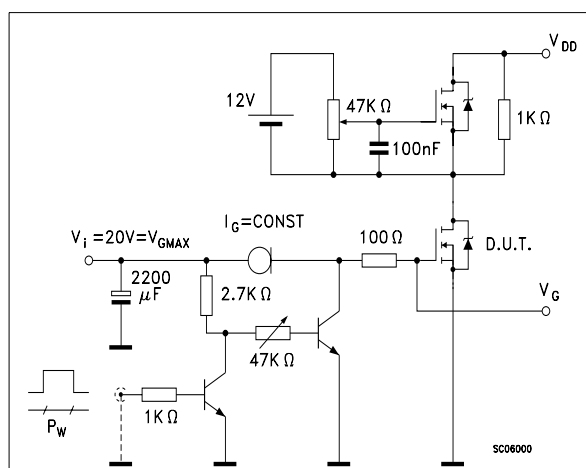
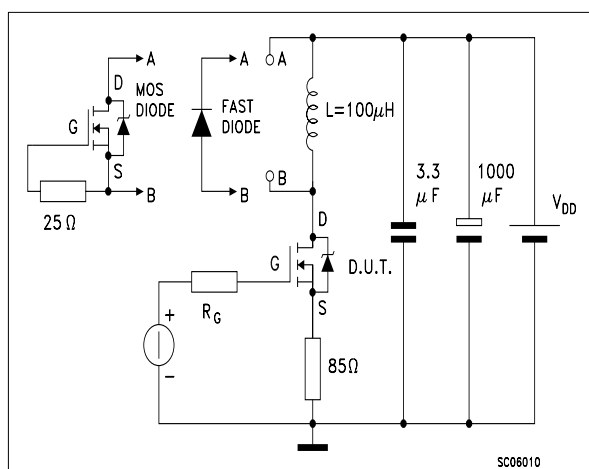
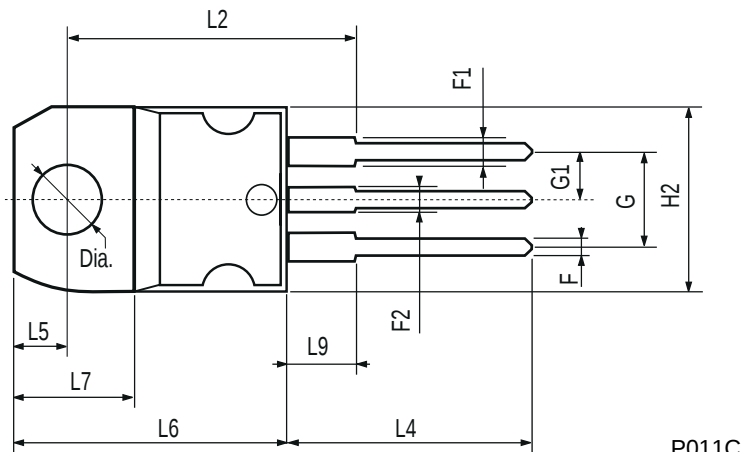
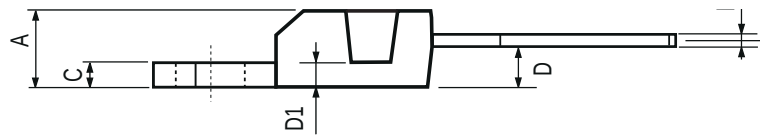


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

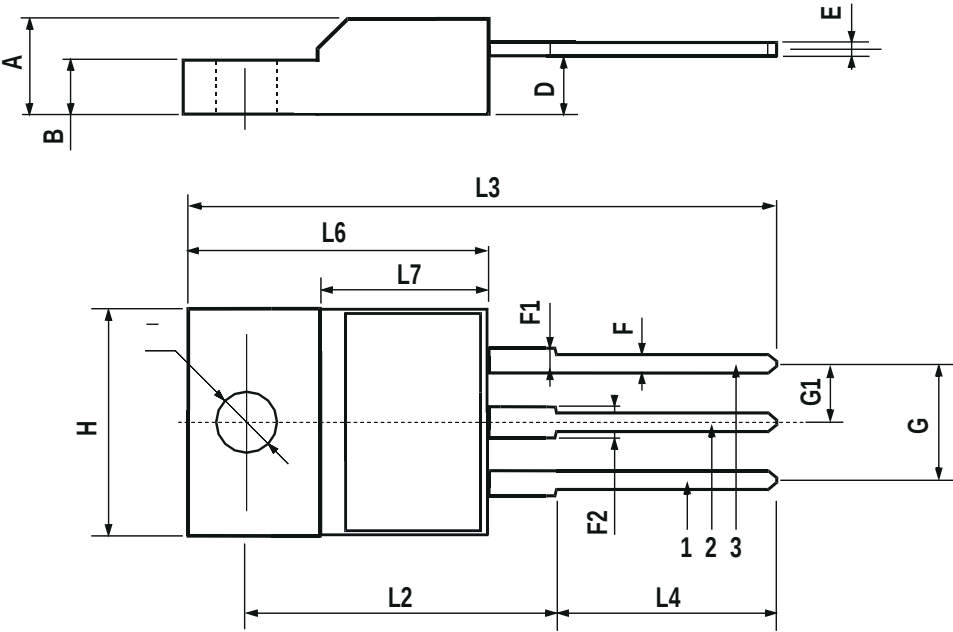
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



P011C

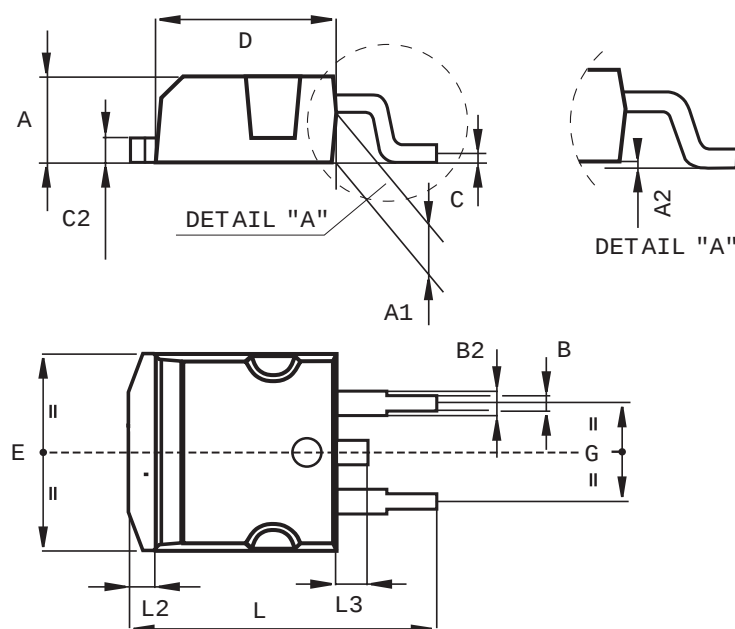
TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-263 (D²PAK) MECHANICAL DATA

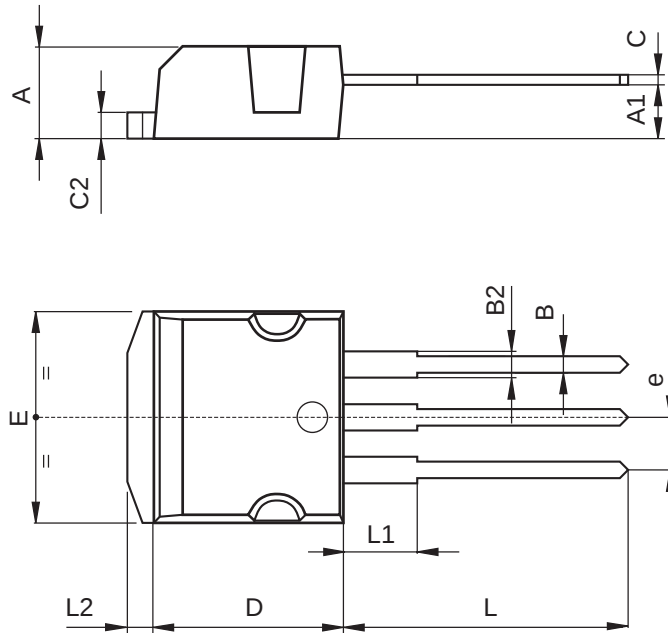
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



P011P6/E

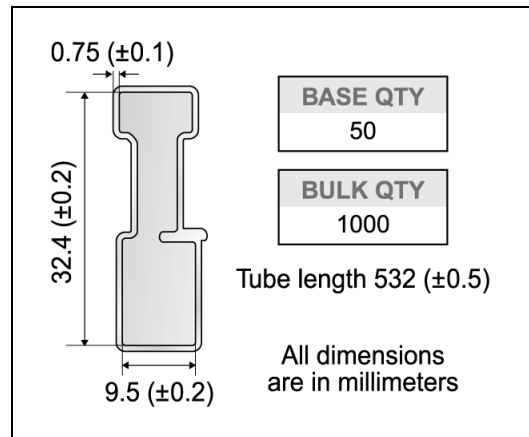
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



P011P5/E

TUBE SHIPMENT (no suffix)*



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