



STB40NF10

N-CHANNEL 100V - 0.025Ω - 50A - D²PAK LOW GATE CHARGE STripFET™II MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB40NF10T4	100 V	< 0.028 Ω	50 A

- TYPICAL R_{DS(on)} = 0.025Ω
- EXCEPTIONAL dv/dt CAPABILITY
- LOW GATE CHARGE AT 100°C
- APPLICATION ORIENTED CHARACTERIZATION
- 100% AVALANCHE TESTED

DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- AUTOMOTIVE ENVIRONMENT

Figure 1: Package

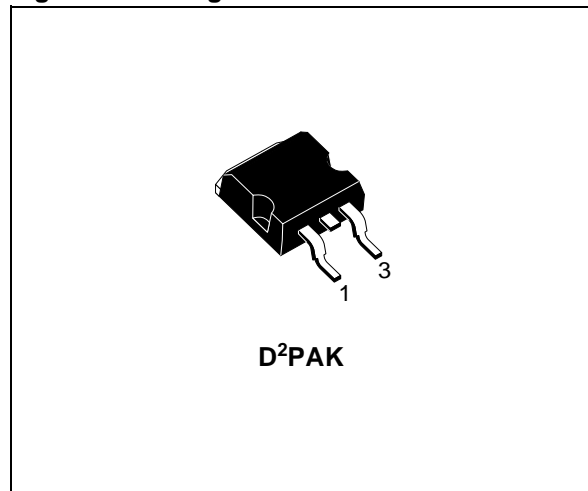


Figure 2: Internal Schematic Diagram

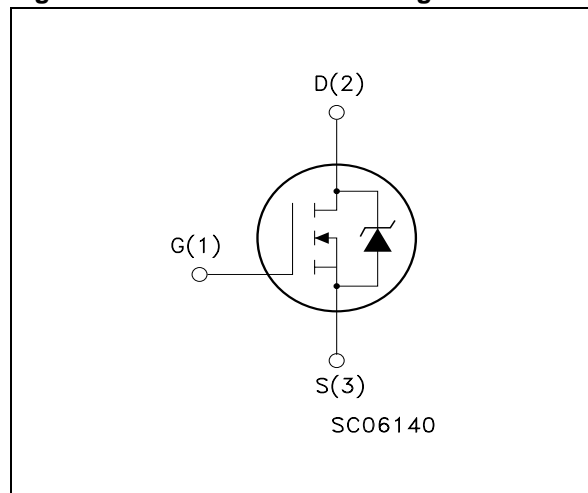


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB40NF10T4	B40NF10	D ² PAK	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	100	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	100	V
V_{GS}	Gate- source Voltage	± 20	V
$I_{D(*)}$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	50	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	35	A
$I_{DM(*)}$	Drain Current (pulsed)	200	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	150	W
	Derating Factor	1	W/ $^\circ\text{C}$
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	150	mJ
T_{stg}	Storage Temperature	- 55 to 175	$^\circ\text{C}$
T_j	Operating Junction Temperature		

(•) Pulse width limited by safe operating area

(*) Limited by Package

(1) $I_{SD} \leq 50\text{A}$, $di/dt \leq 600 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(2) Starting $T_j = 25^\circ\text{C}$, $I_D = 50\text{A}$, $V_{DD} = 25\text{V}$

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	1	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

Table 5: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage	$V_{DS} = \text{Max Rating}$			1	μA
	Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			10	μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2	2.8	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 25 \text{ A}$		0.024	0.028	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 25V, I_D = 25 A$		20		S
C_{iss}	Input Capacitance	$V_{DS} = 25V, f = 1 MHz, V_{GS} = 0$		1780		pF
C_{oss}	Output Capacitance			265		pF
C_{rss}	Reverse Transfer Capacitance			112		pF

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50 V, I_D = 25 A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		28		ns
t_r	Rise Time			63		ns
Q_g	Total Gate Charge	$V_{DD} = 80V, I_D = 50A, V_{GS} = 10V$		60.6	80	nC
Q_{gs}	Gate-Source Charge			9.6		nC
Q_{gd}	Gate-Drain Charge			22.8		nC

Table 8: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 50 V, I_D = 25 A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		84		ns
t_f	Fall Time			28		ns

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				50	A
I_{SDM} (2)	Source-drain Current (pulsed)				200	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 50 A, V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50 A, di/dt = 100A/\mu s, V_{DD} = 25V, T_j = 150^\circ C$ (see test circuit, Figure 5)		114		ns
Q_{rr}	Reverse Recovery Charge			456		nC
I_{RRM}	Reverse Recovery Current			8		A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

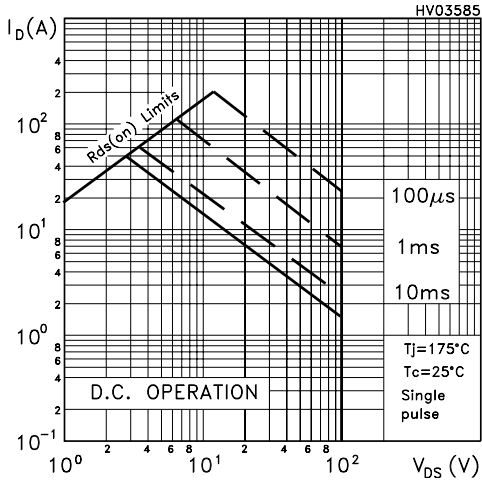


Figure 4: Output Characteristics

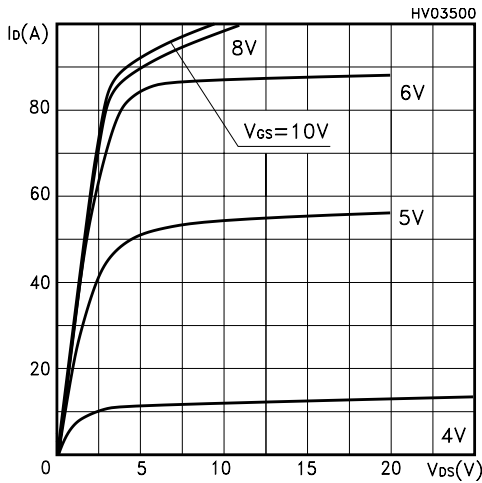


Figure 5: Transconductance

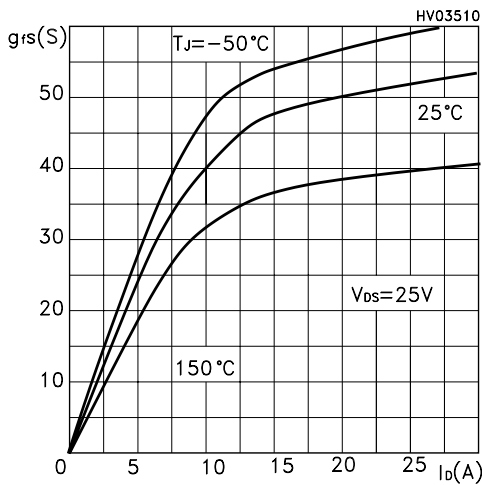


Figure 6: Thermal Impedance

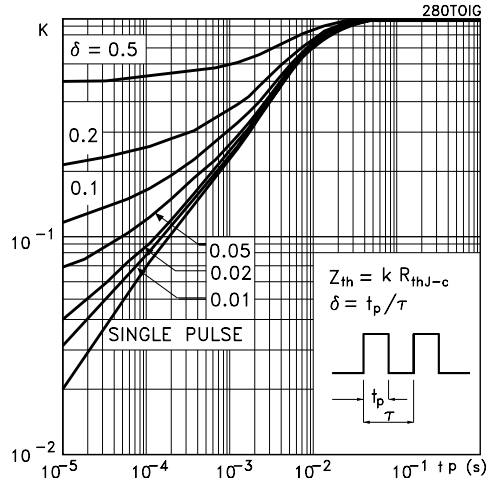


Figure 7: Transfer Characteristics

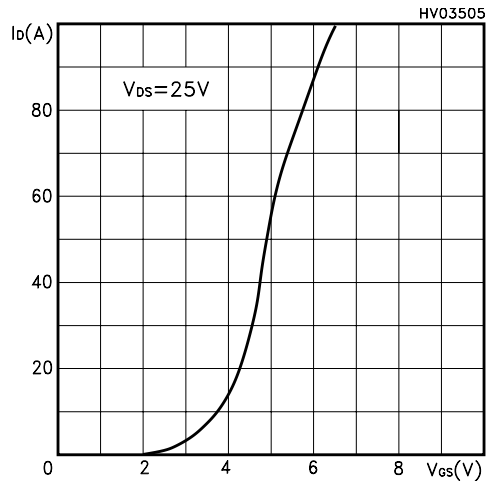


Figure 8: Static Drain-source On Resistance

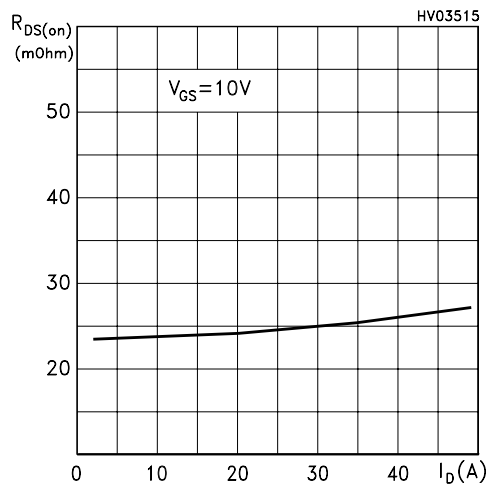


Figure 9: Gate Charge vs Gate-source Voltage

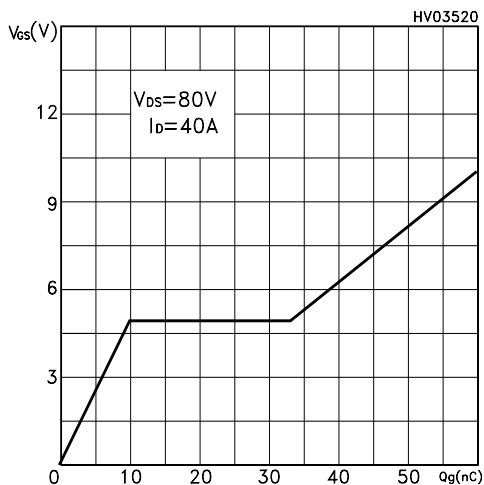


Figure 10: Normalized Gate Threshold Voltage vs Temperature

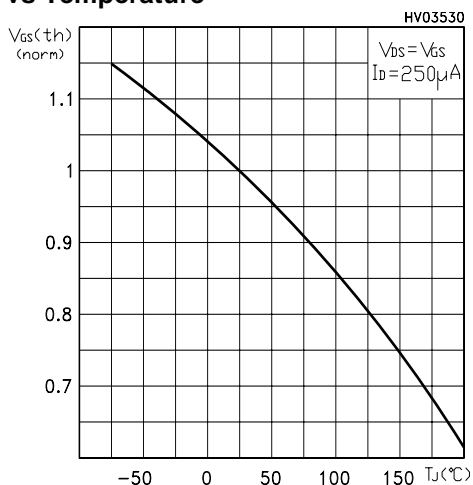


Figure 11: Source-Drain Diode Forward Characteristics

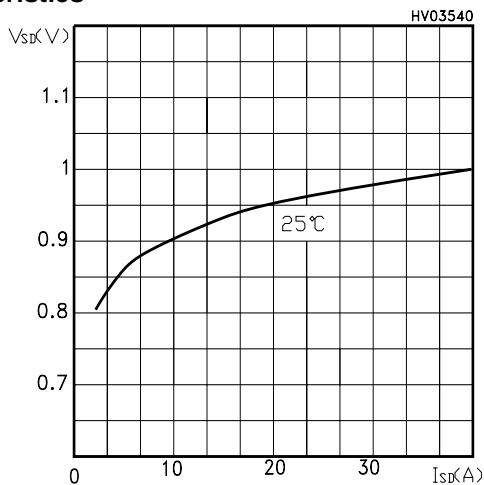


Figure 12: Capacitance Variations

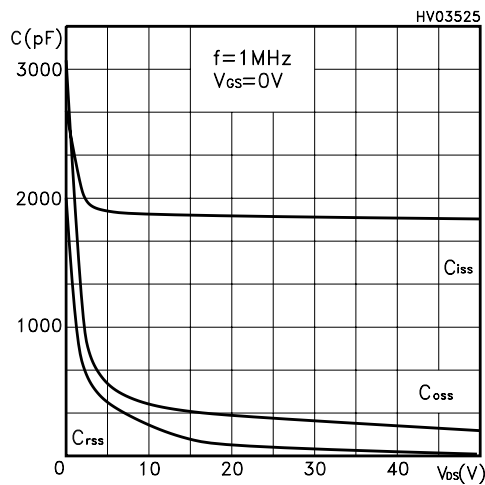


Figure 13: Normalized On Resistance vs Temperature

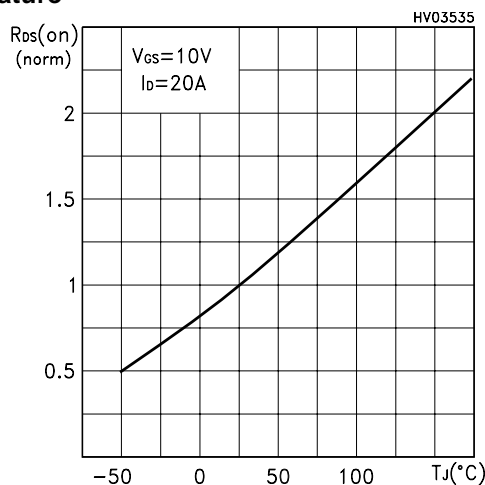


Figure 14: Normalized Breakdown Voltage vs Temperature

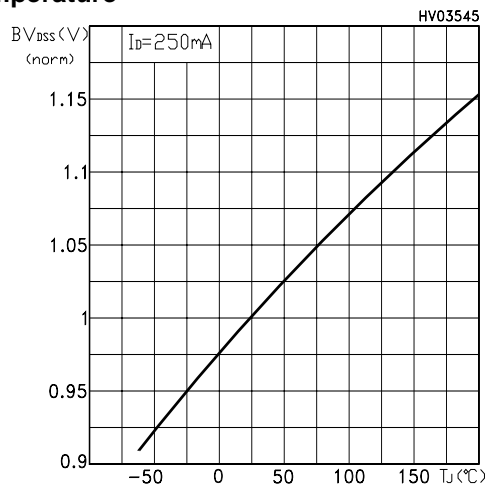


Figure 15: Unclamped Inductive Load Test Circuit

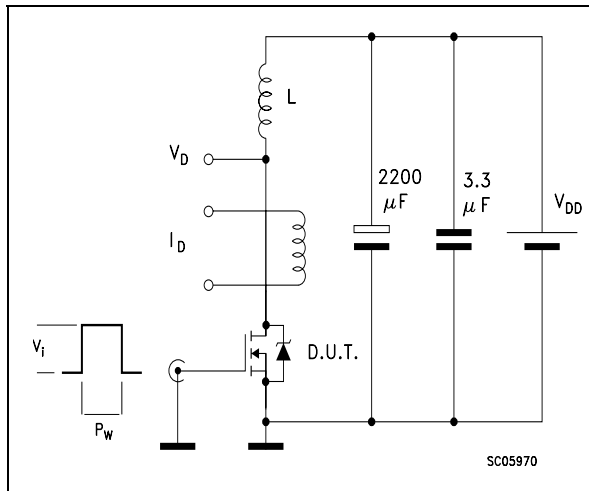


Figure 16: Switching Times Test Circuit For Resistive Load

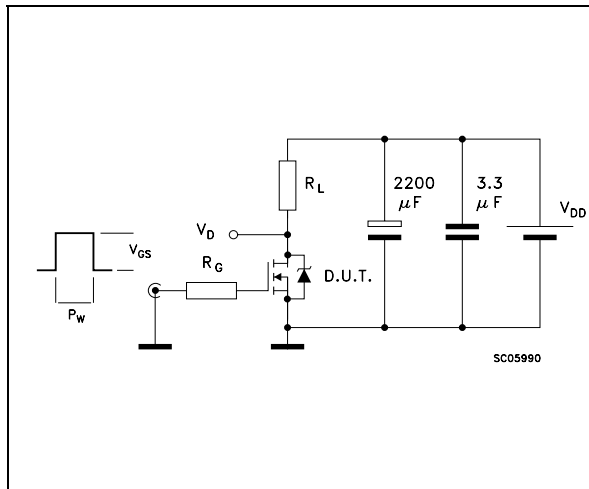


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

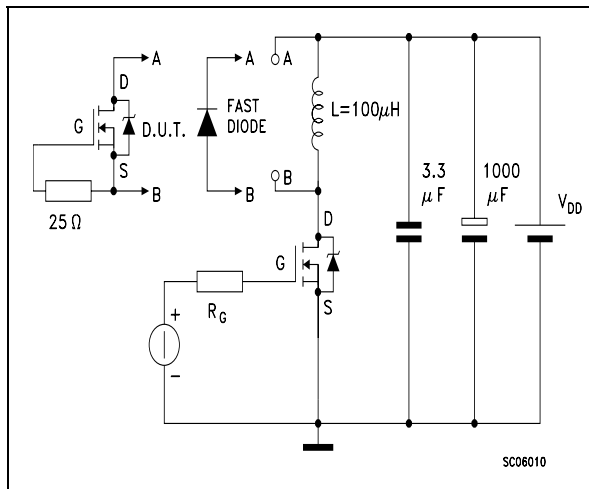


Figure 18: Unclamped Inductive Waferform

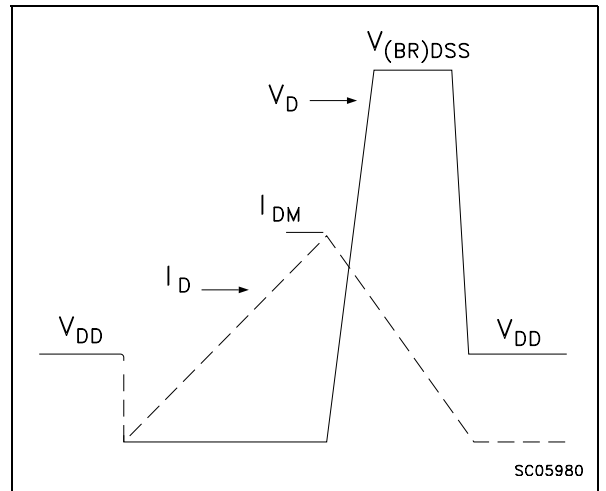
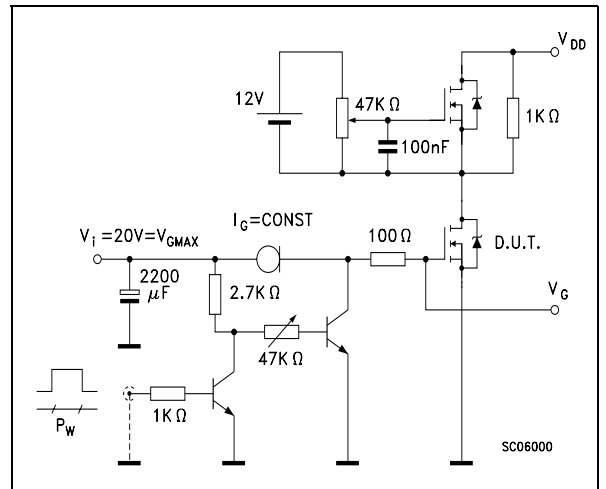
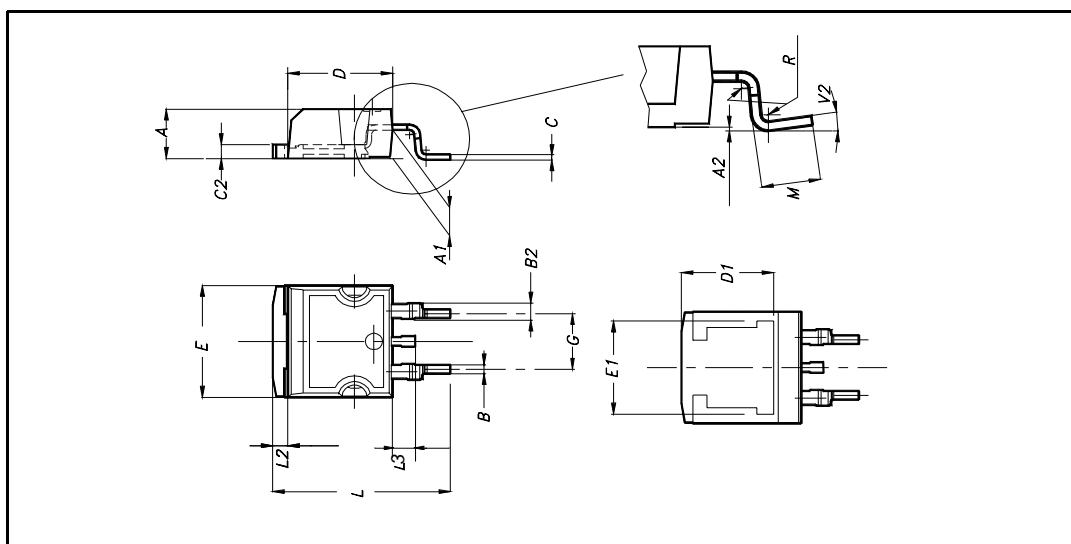


Figure 19: Gate Charge Test Circuit

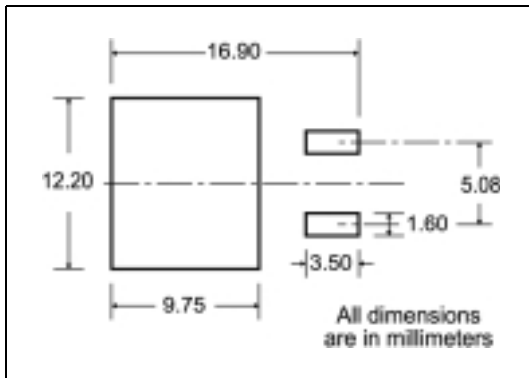


D²PAK MECHANICAL DATA

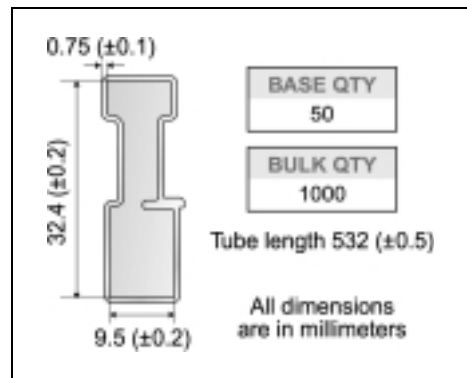
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

* on sales type

Table 10: Revision History

Date	Revision	Description of Changes
14-Dec-2004	2	New Stylesheet

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America