



STB45N10L

N-CHANNEL 100V - 0.028 Ω - 45A I²PAK/D²PAK POWER MOS TRANSISTOR

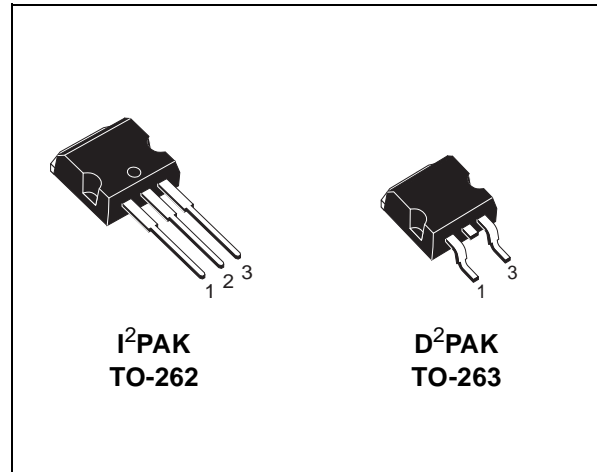
PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB45N10L	100 V	< 0.036 Ω	45 A

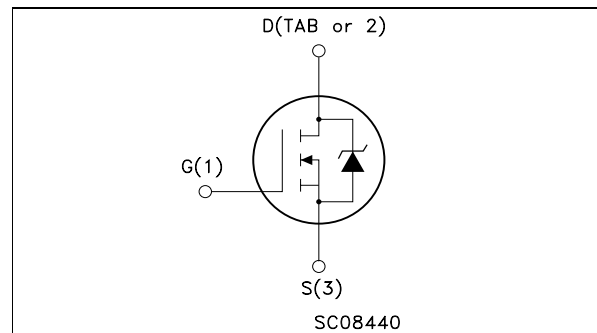
- TYPICAL R_{DS(on)} = 0.028 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100oC
- LOW INPUT CAPACITANCE
- LOW GATE CHARGE
- LOW LEAKAGE CURRENT
- APPLICATION ORIENTED CHARACTERIZATION
- THROUGH-HOLE I²PAK (TO-262) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TUBE (NO SUFFIX) OR IN TAPE & REEL (SUFFIX "T4")

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLY (SMPS)
- CONSUMER AND INDUSTRIAL LIGHTING
- DC-AC CONVERTER FOR WELDING EQUIPMENT AND UNINTERRUPTABLE POWER SUPPLY (UPS)



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate- source Voltage	±15	V
I _D	Drain Current (continuous) at T _C = 25°C	45	A
I _D	Drain Current (continuous) at T _C = 100°C	32	A
I _{DM} (●)	Drain Current (pulsed)	180	A
P _{tot}	Total Dissipation at T _C = 25°C	150	W
	Derating Factor	1	W/°C
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●)Pulse width limited by safe operating area

STB45N10L

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	1	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W
$R_{thc-sink}$	Thermal Resistance Junction-ambient	Typ	0.5	°C/W
T_j	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	45	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	400	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ °C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_C = 125\text{ °C}$			250 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 15\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 5\text{ V}$ $I_D = 22.5\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 22.5\text{ A}$ $T_C = 100\text{ °C}$ $V_{GS} = 10\text{ V}$ $I_D = 22.5\text{ A}$ $V_{GS} = 10\text{ V}$ $I_D = 22.5\text{ A}$ $T_C = 100\text{ °C}$		0.028 0.024	0.036 0.072 0.032 0.064	Ω Ω Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	45			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(*)}$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 22.5\text{ A}$	20	43		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		3700	4700	pF
C_{oss}	Output Capacitance			600	800	pF
C_{rss}	Reverse Transfer Capacitance			170	230	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 22.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (see test circuit, Figure 3)		25 100	35 140	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 80\text{ V}$ $I_D = 45\text{ A}$ $R_G = 47\ \Omega$ $V_{GS} = 5\text{ V}$ (see test circuit, Figure 5)		130		A/ μ s
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 80\text{ V}$ $I_D = 45\text{ A}$ $V_{GS} = 5\text{ V}$		70 15 35	100	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{clamp} = 80\text{ V}$ $I_D = 45\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (see test circuit, Figure 5)		40 90 130	60 130 190	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				45 180	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 45\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 45\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_R = 30\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, Figure 5)		165 0.1 12		ns μ C A

(*) Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %.

(\bullet) Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

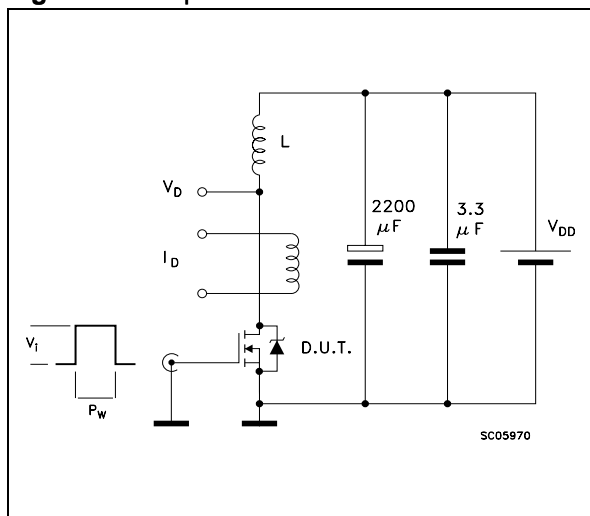


Fig. 2: Unclamped Inductive Waveform

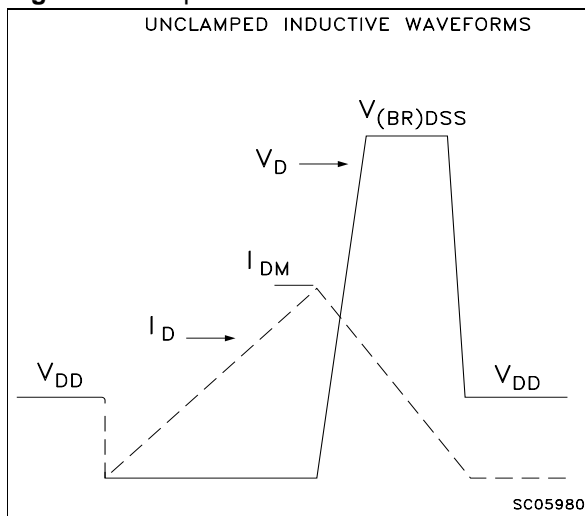


Fig. 3: Switching Times Test Circuits For Resistive Load

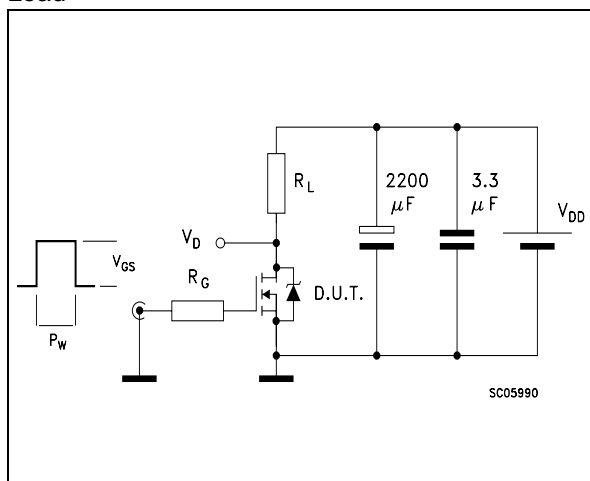


Fig. 4: Gate Charge test Circuit

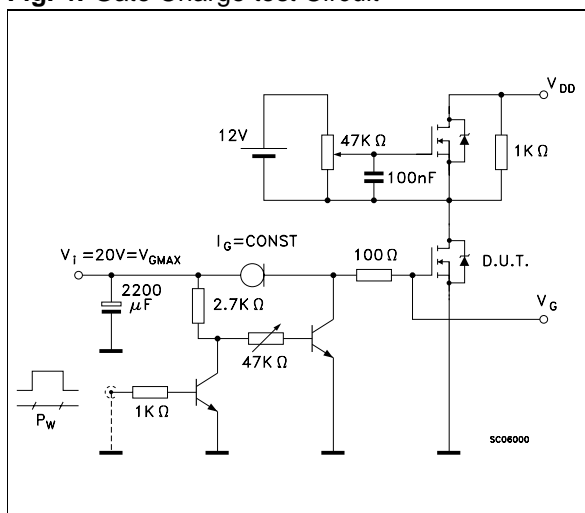
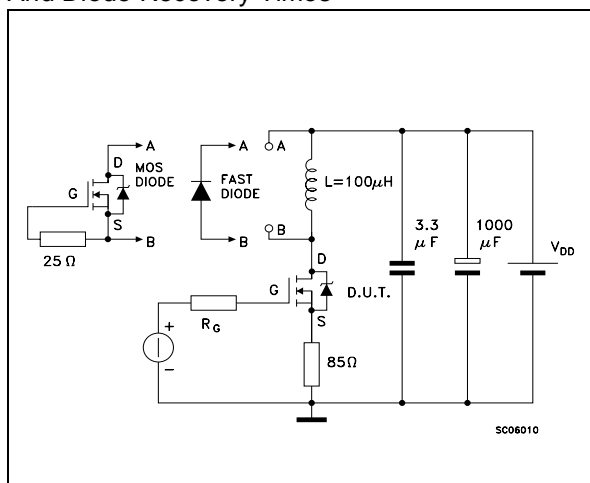
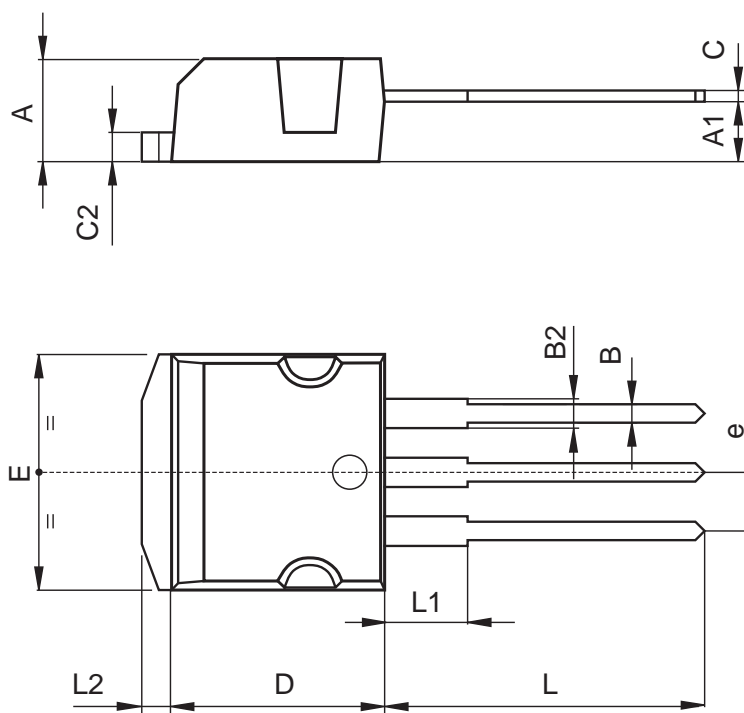


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-262 (I²PAK) MECHANICAL DATA

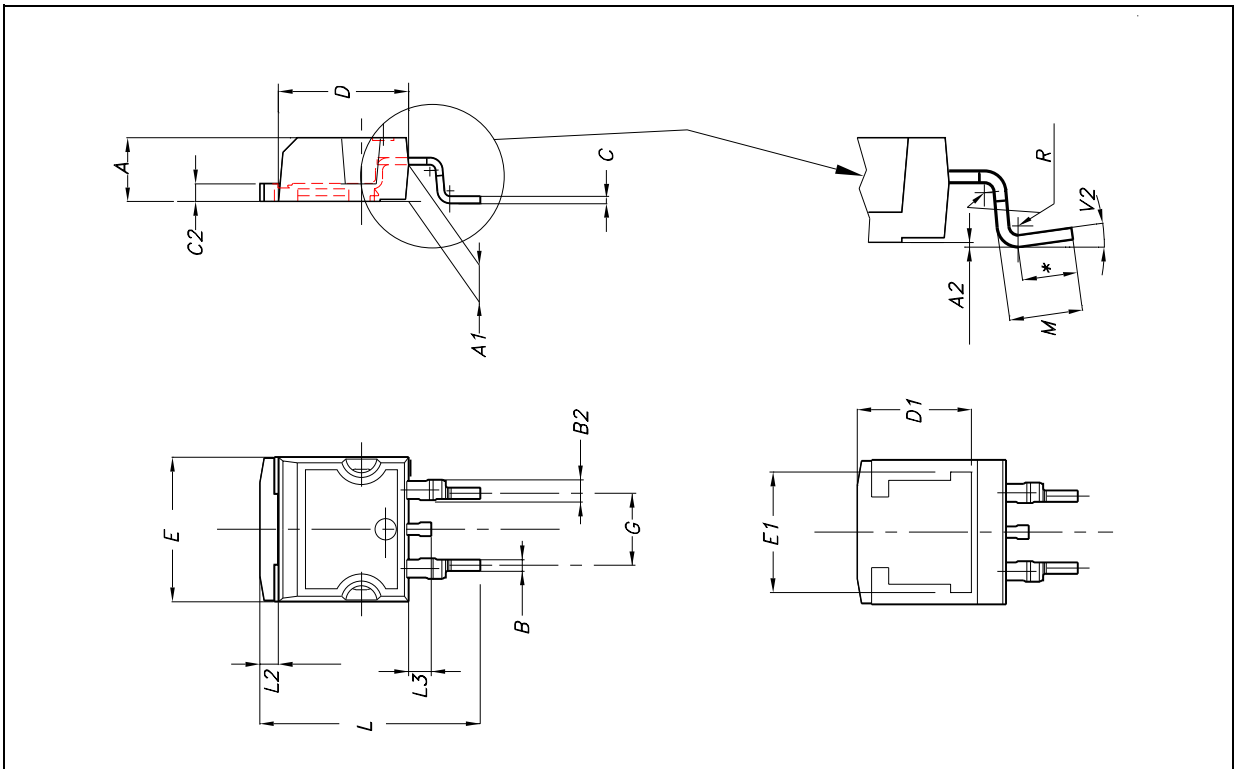
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



P011P5/E

D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
© 2000 STMicroelectronics - All Rights Reserved

All other names are the property of their respective owners.

STMicroelectronics GROUP OF COMPANIES
Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>