STB7NB40

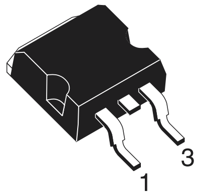
N-CHANNEL 400V - 0.75 Ω - 7.0A D²PAK
PowerMESH™ MOSFET

PRELIMINARY DATA

Table 1. General Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB7NB40	400 V	< 0.9 Ω	7.0 A

Figure 1. Package



D²PAK
TO-263

FEATURES SUMMARY

- TYPICAL $R_{DS(on)}$ = 0.75 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

DESCRIPTION

Using the latest high voltage technology, STMicroelectronics has designed an advanced family of power Mosfets with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area,exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

Figure 2. Internal Schematic Diagram

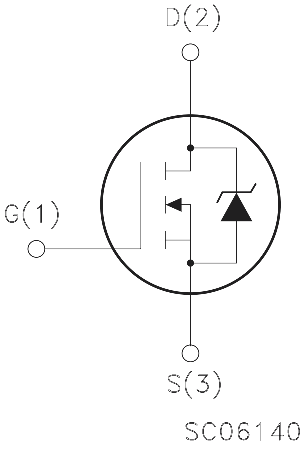


Table 2. Order Codes

Part Number	Marking	Package	Packaging
STB7NB40T4	B7NB40	D²PAK	TAPE & REEL

REV. 2

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	400	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	400	V
V_{GS}	Gate-source Voltage	± 30	V
I_D	Drain Current (cont.) at T_C = 25 °C	7	A
I_D	Drain Current (cont.) at T_C = 100 °C	4.4	A
I_{DM} (1)	Drain Current (pulsed)	28	A
P_{tot}	Total Dissipation at T_C = 25 °C	100	W
	Derating Factor	0.8	W°/C
dv/dt (2)	Peak Diode Recovery voltage slope	4.5	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

Note: 1. Pulse width limited by safe operating area
2. $I_{SD} \leq 7A$, $di/dt \leq 200$ A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	1.25	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5. Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, δ < 1%)	7	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C; $I_D = I_{AR}$; V_{DD} = 50 V)	300	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Table 6. Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA; V_{GS} = 0	400			V
I_{DSS}	Zero Gate Voltage	V_{DS} = Max Rating			1	µA
	Drain Current (V_{GS} = 0)	V_{DS} = Max Rating Tc = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30 V			± 100	nA

Table 7. On (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}; I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V; I_D = 3.5 A		0.75	0.9	Ω

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Table 8. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$; I_D = 3.5 A	2.5	4.2		S
C_{iss}	Input Capacitance	V_{DS} = 25 V; f = 1 MHz; V_{GS} = 0		705	720	pF
C_{oss}	Output Capacitance			132	175	pF
C_{rss}	Reverse Transfer Capacitance			17	25	pF

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Table 9. Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
td(on)	Turn-on Time	V_{DD} = 200 V; I_D = 3.5 A; R_G = 4.7 Ω		11.5	16	ns
tr	Rise Time	V_{GS} = 10 V (see test circuit, Figure 5)		7.5	11	ns
Q_g	Total Gate Charge	V_{DD} = 320 V; I_D = 7 A; V_{GS} = 10 V		21	30	nC
Q_{gs}	Gate-Source Charge			7.3		nC
Q_{gd}	Gate-Drain Charge			8.5		nC

Table 10. Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 320 V; I_D = 7 A; R_G = 4.7 Ω		9.5	15	ns
t_f	Fall Time	V_{GS} = 10 V (see test circuit, Figure 7)		9	14	ns
t_c	Cross-over Time			16.5	25	ns

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				7	A
I_{SDM} (1)	Source-drain Current (pulsed)				28	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 7 A; V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 7 A; di/dt = 100 A/µs V_{DD} = 100 V; T_j = 150 °C (see test circuit, Figure 7)		300		ns
Q_{rr}	Reverse RecoveryCharge			2		µC
I_{RRAM}	Reverse RecoveryCharge			13.7		A

Note: 1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Figure 3. Unclamped Inductive Load Test Circuit

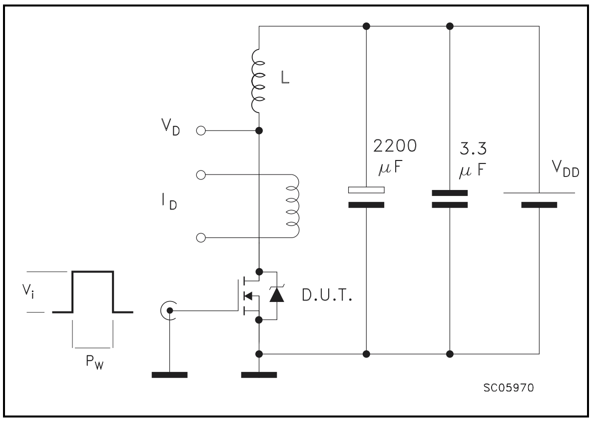


Figure 4. Unclamped Inductive Waveforms

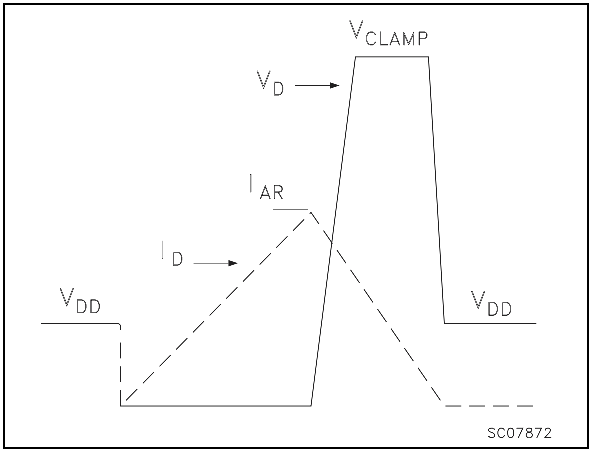


Figure 5. Switching Times Test Circuits For Resistive Load

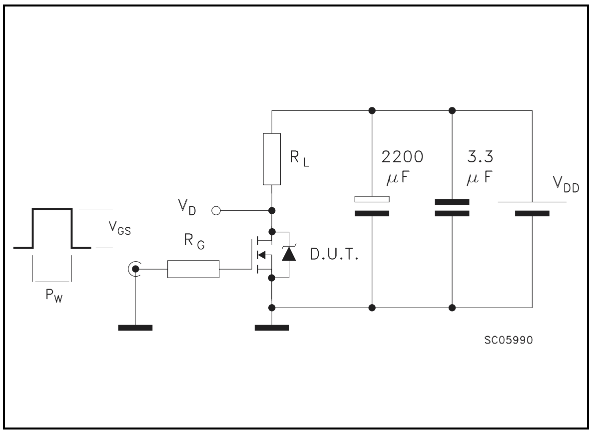


Figure 6. Gate Charge Test Circuit

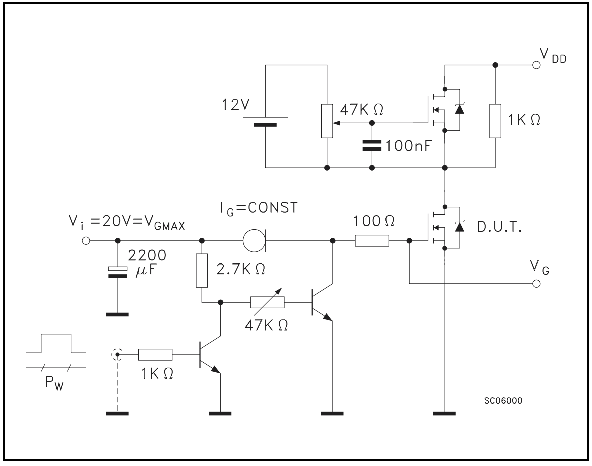
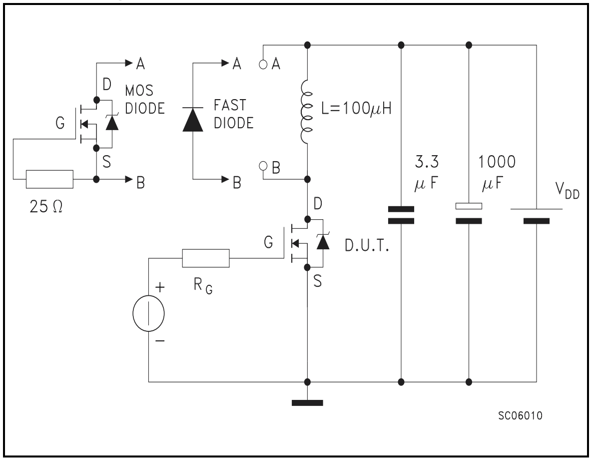


Figure 7. Test Circuit For Inductive Load Switching And Diode Recovery Times

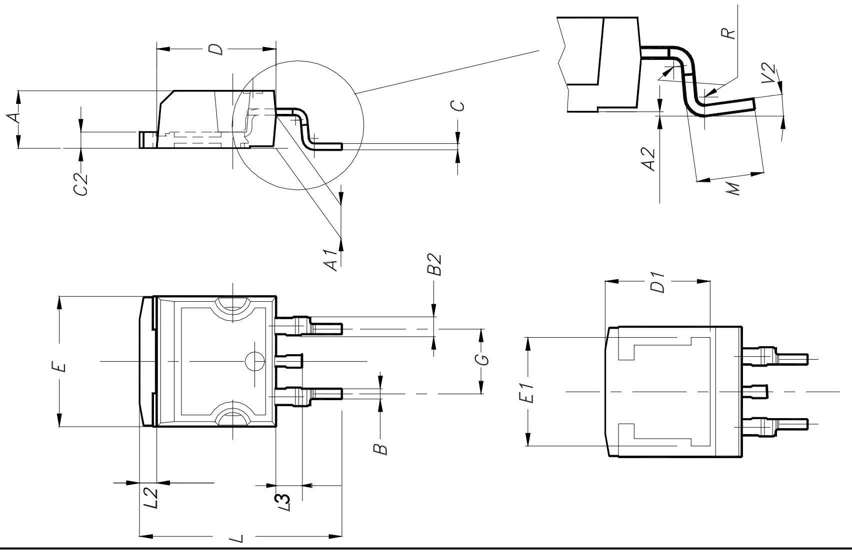


PACKAGE MECHANICAL

Table 12. D^{2}PAK Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			

Figure 8. D^{2}PAK Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY

Table 13. Revision History

Date	Revision	Description of Changes
October-1997	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.

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