

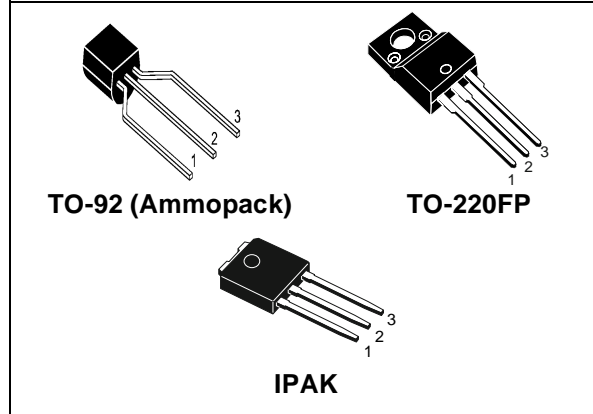


STQ2HNK60ZR-AP STF2HNK60Z - STD2HNK60Z-1

N-CHANNEL 600V - 4.4Ω - 2.0A TO-92/TO-220FP/IPAK
Zener-Protected SuperMESH™ MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _W
STQ2HNK60ZR-AP	600 V	< 4.8 Ω	0.5 A	3 W
STD2HNK60Z-1	600 V	< 4.8 Ω	2.0 A	45 W
STF2HNK60Z	600 V	< 4.8 Ω	2.0 A	20 W

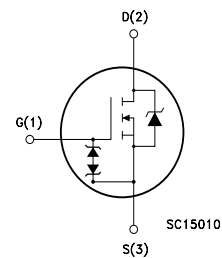
- TYPICAL R_{DS(on)} = 4.4Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITCH MODE POWER SUPPLIES (SMPS)

ORDER CODES

PART NUMBER	MARKING	PACKAGE	PACKAGING
STD2HNK60Z-1	D2HNK60Z	IPAK	TUBE
STQ2HNK60ZR-AP	Q2HNK60ZR	TO-92	AMMOPAK
STF2HNK60Z	F2HNK60Z	TO-220FP	TUBE

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		IPAK	TO-220FP	TO-92	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600			V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600			V
V _{GS}	Gate- source Voltage	± 30			V
I _D	Drain Current (continuous) at T _C = 25°C	2.0	2.0 (*)	0.5	A
I _D	Drain Current (continuous) at T _C = 100°C	1.26	1.26 (*)	0.32	A
I _{DM} (•)	Drain Current (pulsed)	8	8 (*)	2	A
P _{TOT}	Total Dissipation at T _C = 25°C	45	20	3	W
	Derating Factor	0.36	0.16	0.025	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000			V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	--	2500	--	V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 2 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Current Limited by package

THERMAL DATA

		IPAK	TO-220FP	TO-92	
R _{thj-case}	Thermal Resistance Junction-case Max	2.77	6.25	--	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	100	62.5	120	°C/W
R _{thj-lead}	Thermal Resistance Junction-lead Max	--	--	40	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	300	260	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	2	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	120	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} =± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

STQ2Hnk60ZR-AP - STF2Hnk60Z - STD2Hnk60Z-1

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 1.0 A		4.4	4.8	Ω

DYNAMIC

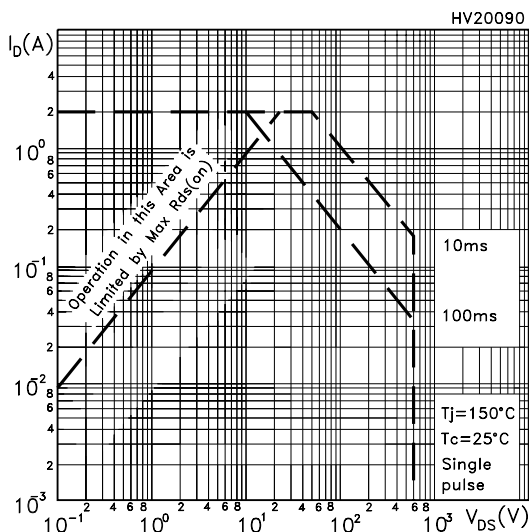
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 1.0 A		1.5		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		280 38 7		pF pF pF
C _{oss eq.} (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 480V		30		pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V _{DD} = 300 V, I _D = 1.0 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		10 30 23 50		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 480V, I _D = 2.0 A, V _{GS} = 10V		11 2.25 6	15	nC nC nC

SOURCE DRAIN DIODE

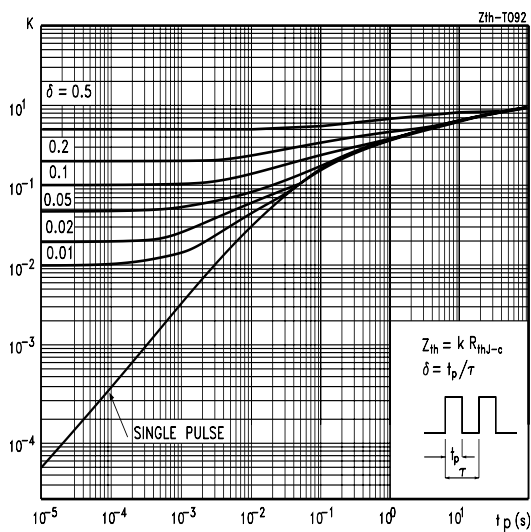
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				2.0 8.0	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 2.0 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{Rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 2.0 A, di/dt = 100 A/μs V _{DD} = 20 V, T _j = 25°C (see test circuit, Figure 5)		178 445 5		ns nC A
t _{rr} Q _{rr} I _{Rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 13 A, di/dt = 100 A/μs V _{DD} = 20 V, T _j = 150°C (see test circuit, Figure 5)		200 500 5		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.
 3. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

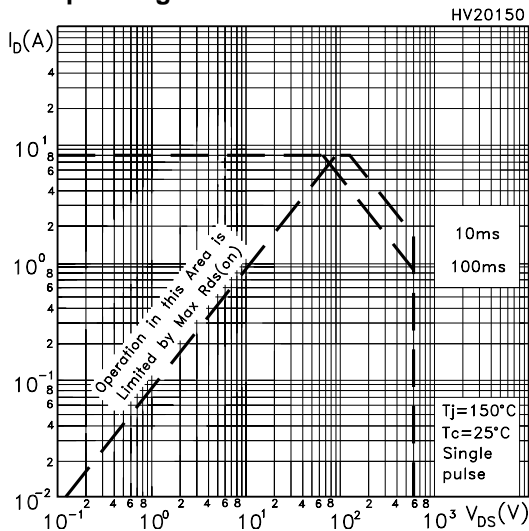
Safe Operating Area for TO-92



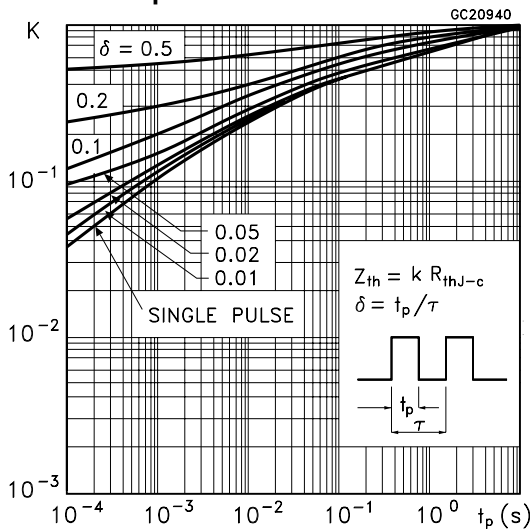
Thermal Impedance for TO-92



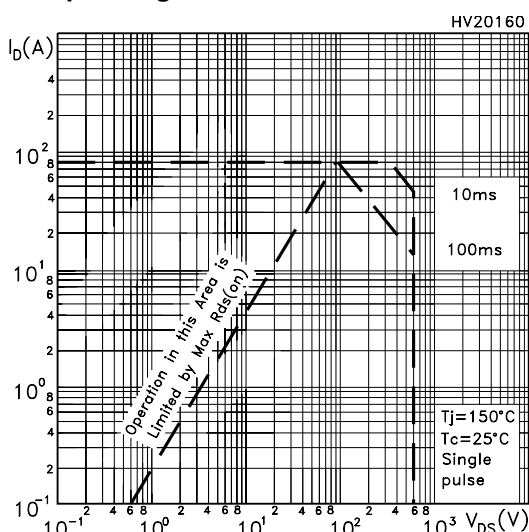
Safe Operating Area for TO-220FP



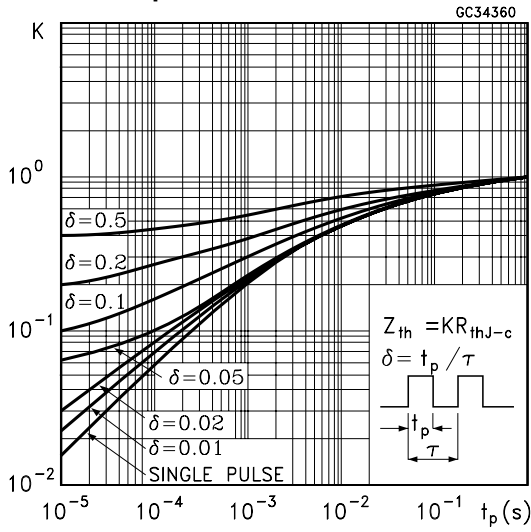
Thermal Impedance for TO-220FP



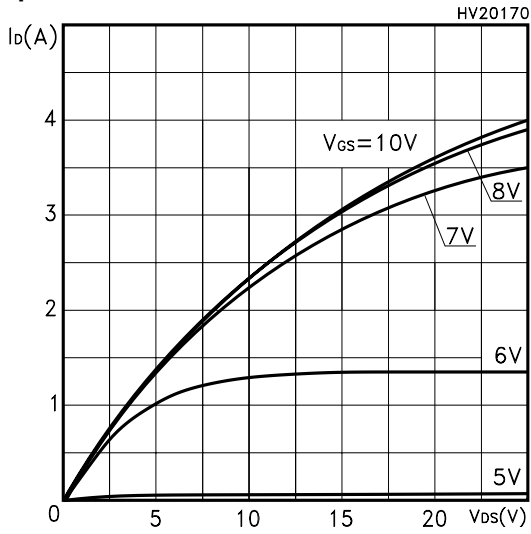
Safe Operating Area for IPAK



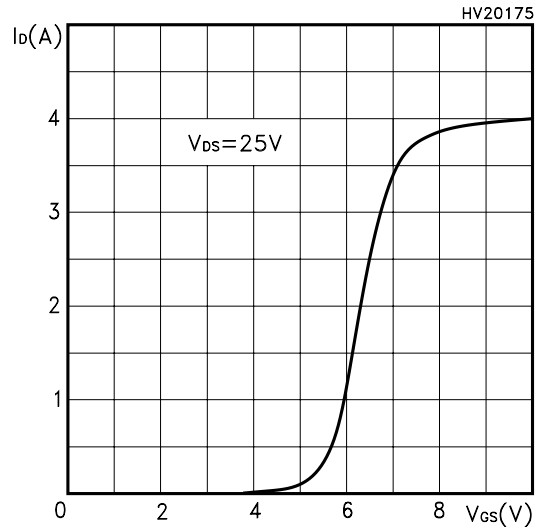
Thermal Impedance for IPAK



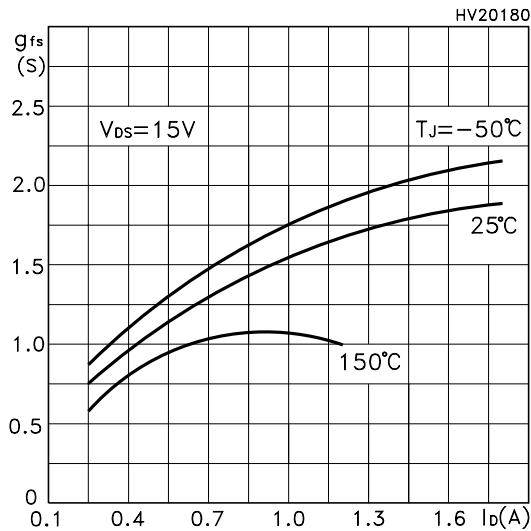
Output Characteristics



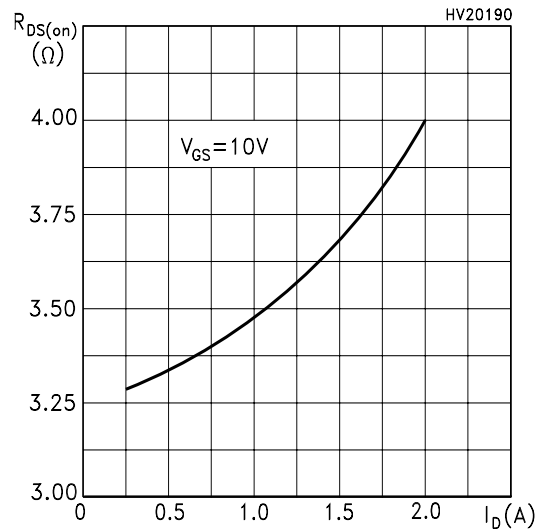
Transfer Characteristics



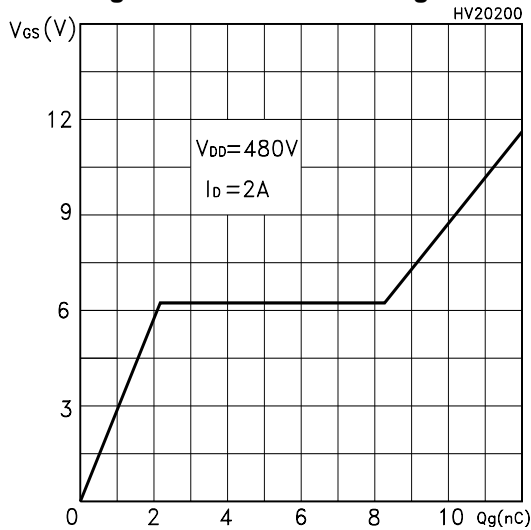
Transconductance



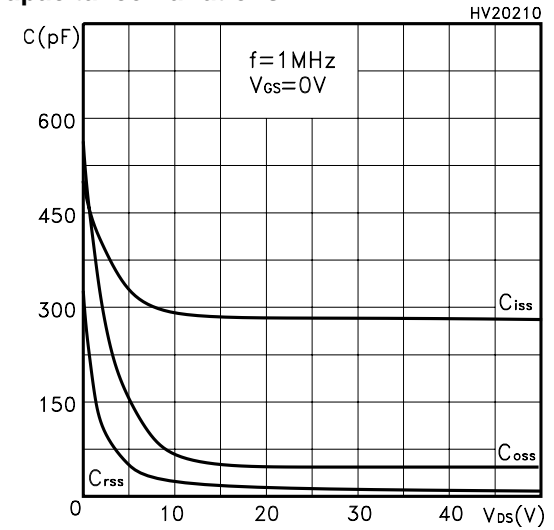
Static Drain-source On Resistance



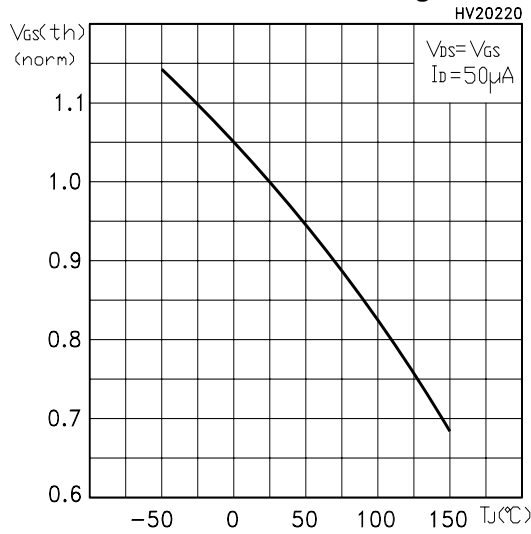
Gate Charge vs Gate-source Voltage



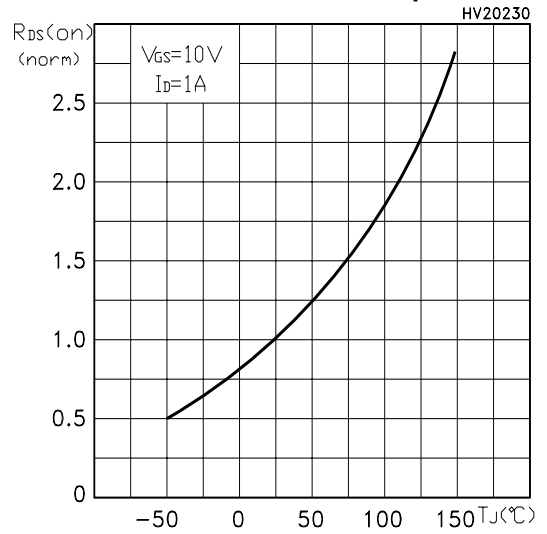
Capacitance Variations



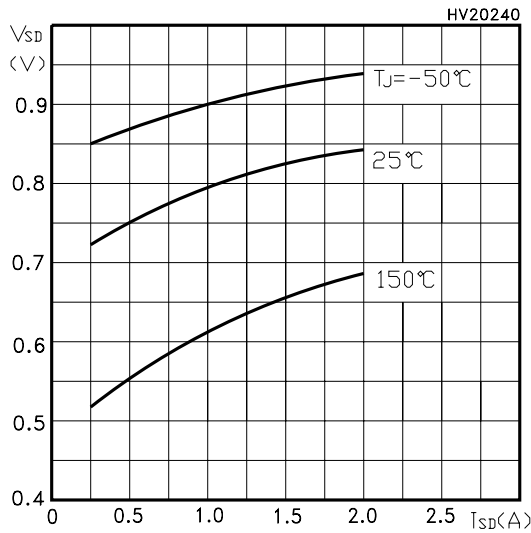
Normalized Gate Threshold Voltage vs Temp.



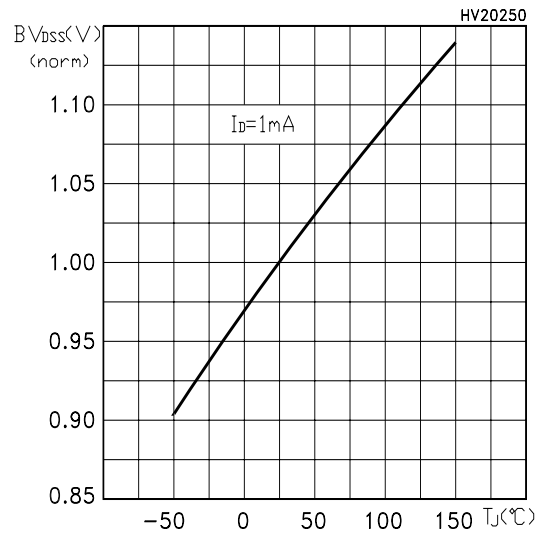
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

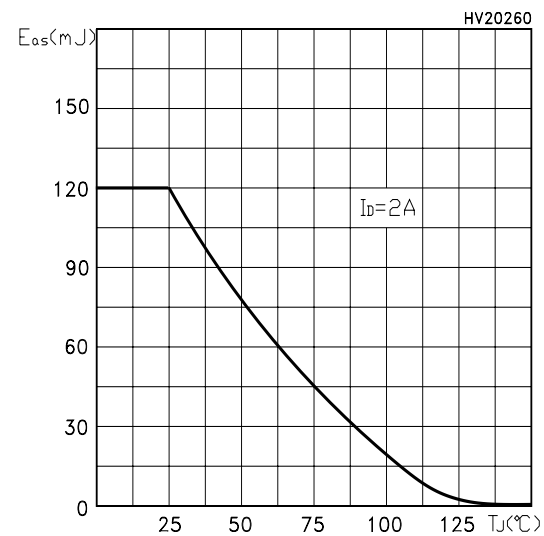


Fig. 1: Unclamped Inductive Load Test Circuit

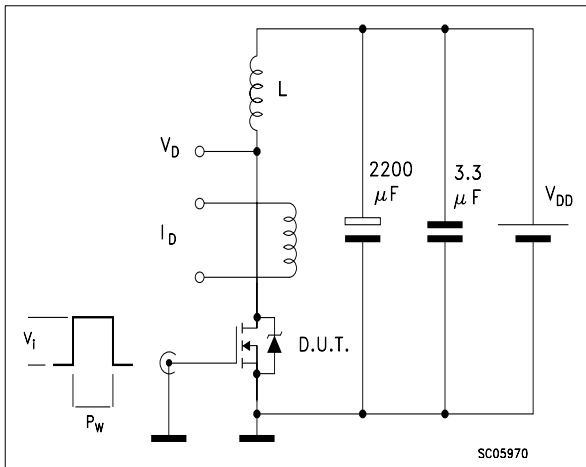


Fig. 2: Unclamped Inductive Waveform

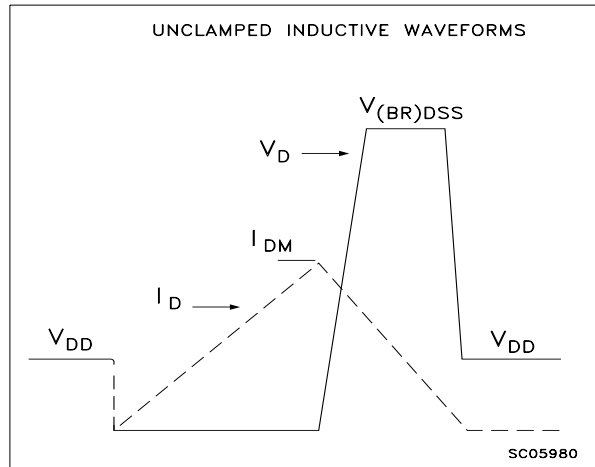


Fig. 3: Switching Times Test Circuit For Resistive Load

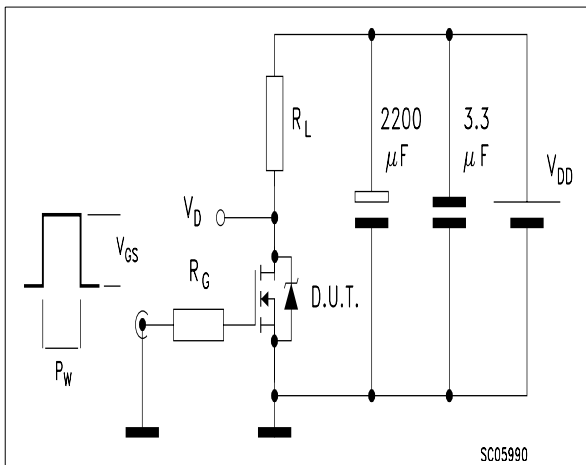


Fig. 4: Gate Charge test Circuit

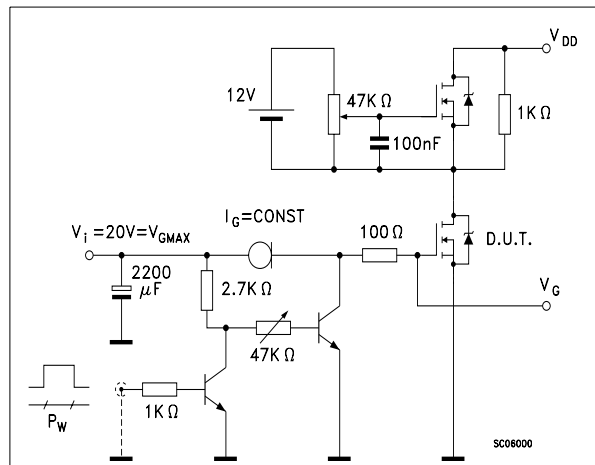
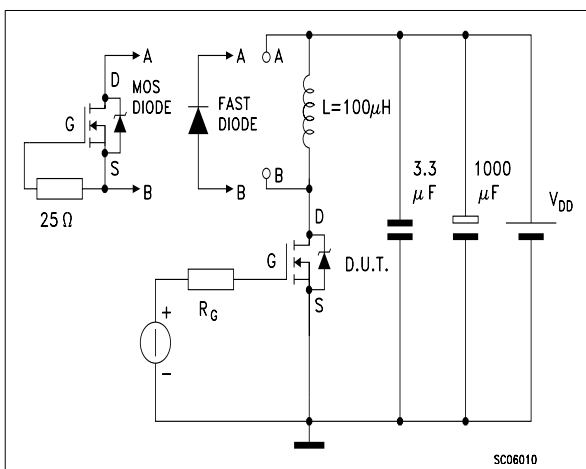
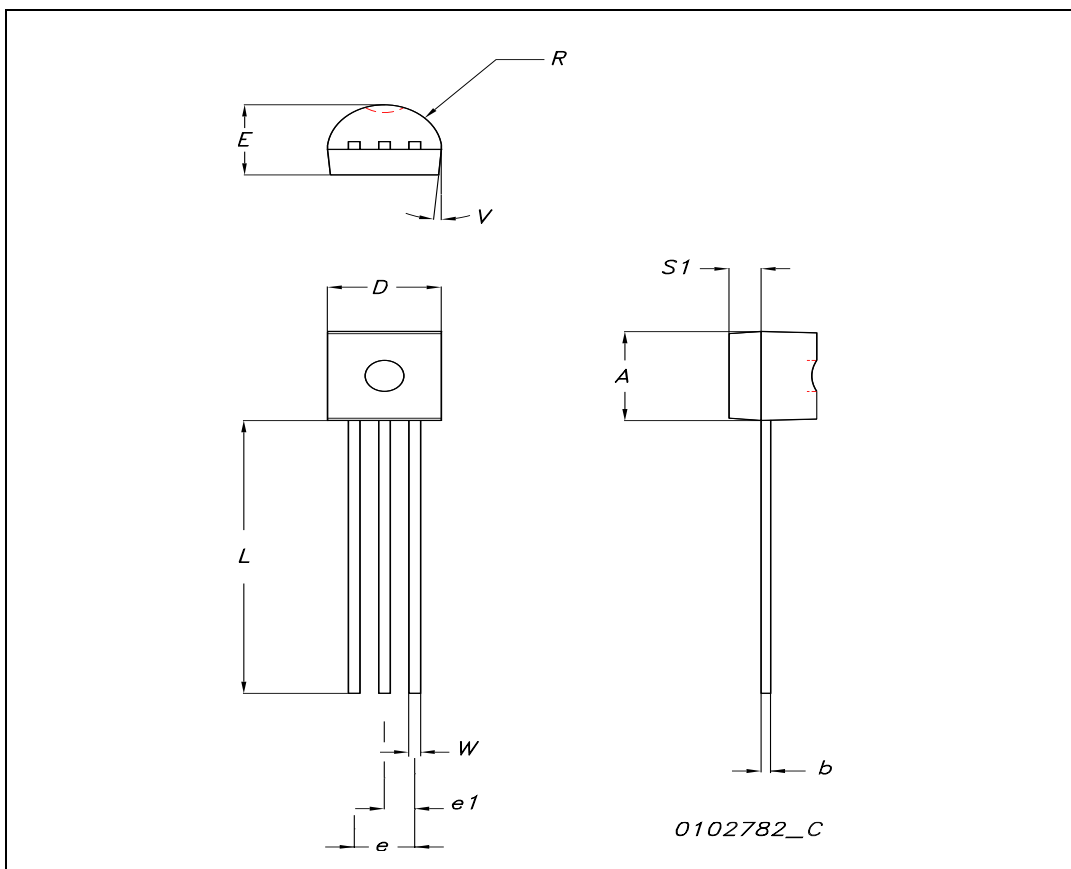


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



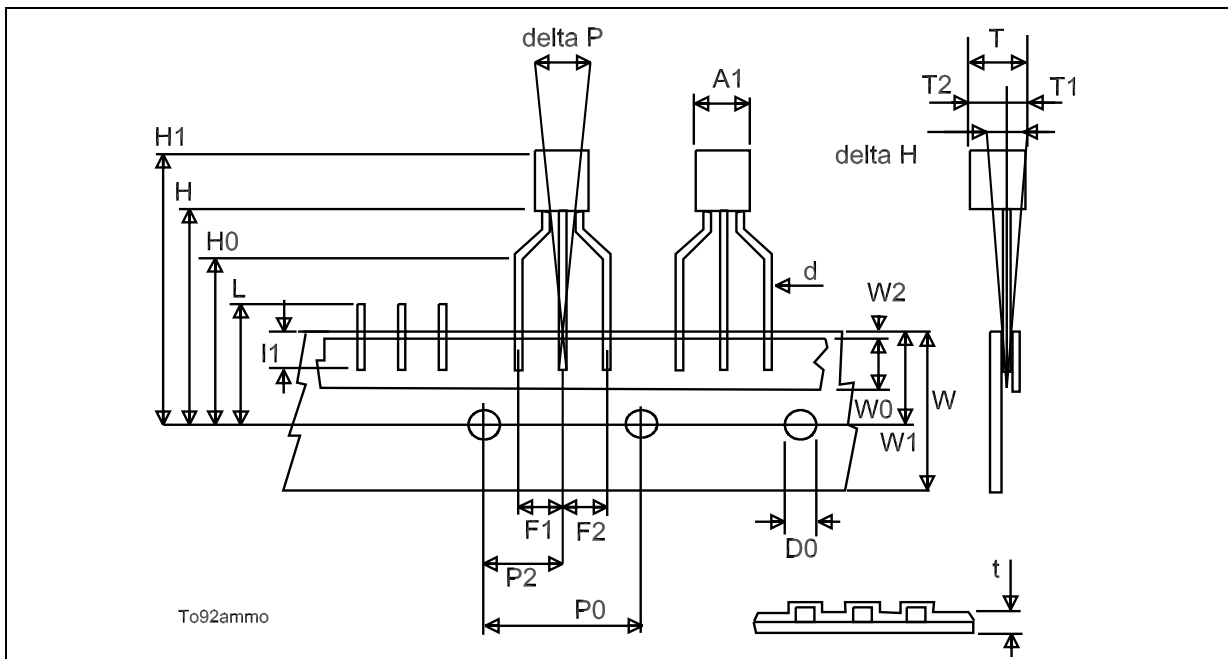
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



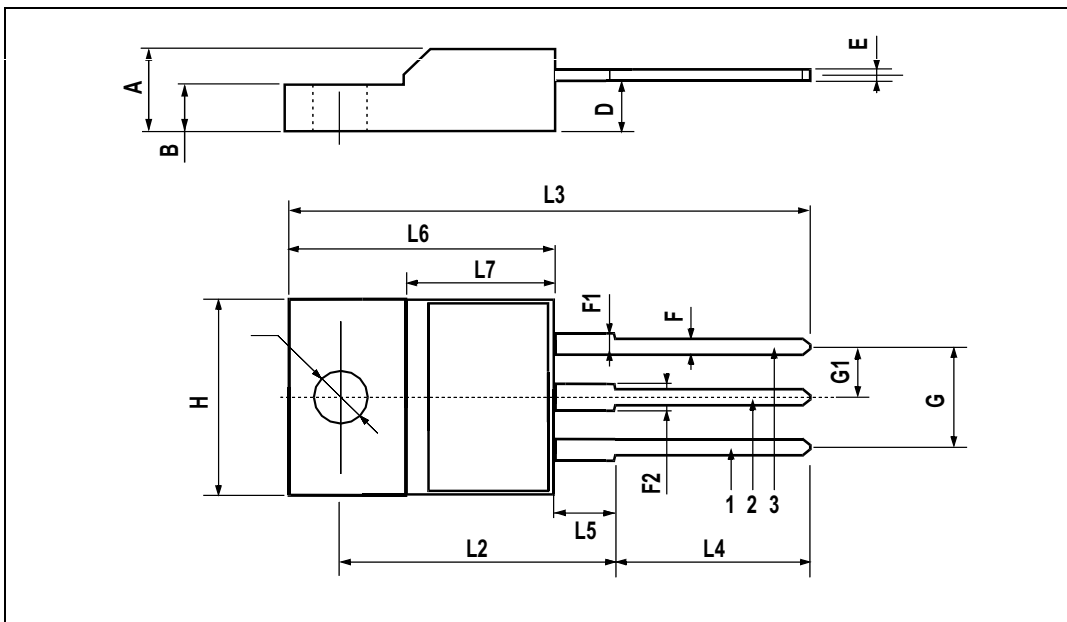
TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
l1	3			0.11		
delta P	-1		1	-0.04		0.04



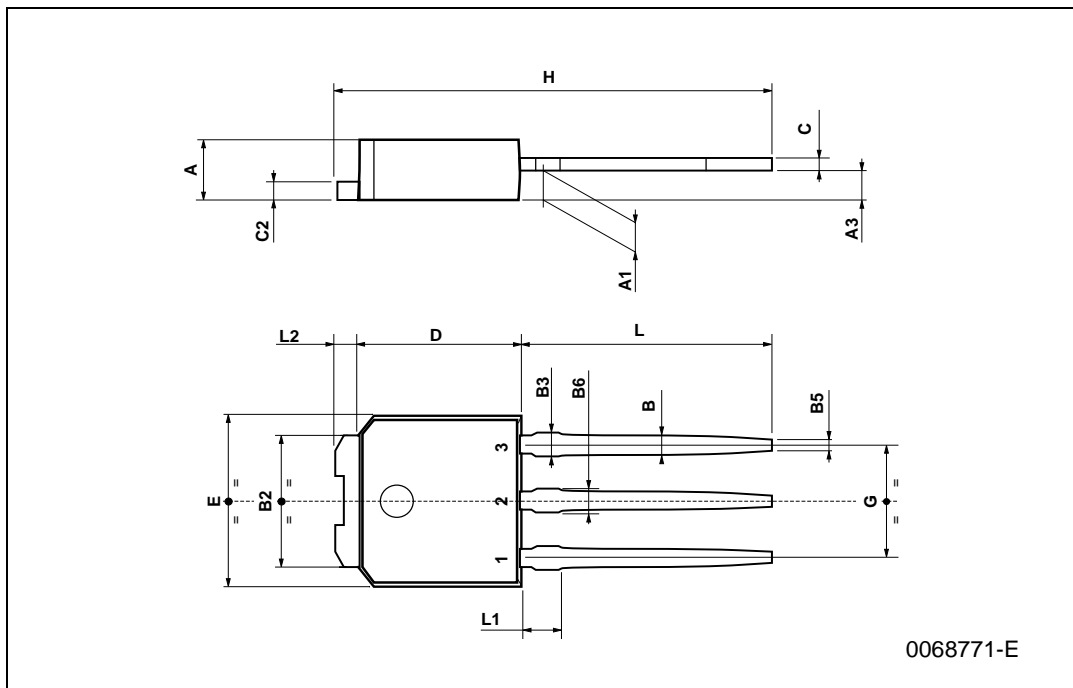
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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