



STD40NF3LL

N-CHANNEL 30V - 0.009 Ω - 40A DPAK LOW GATE CHARGE STripFET™II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD40NF3LL	30 V	<0.011 Ω	40 A

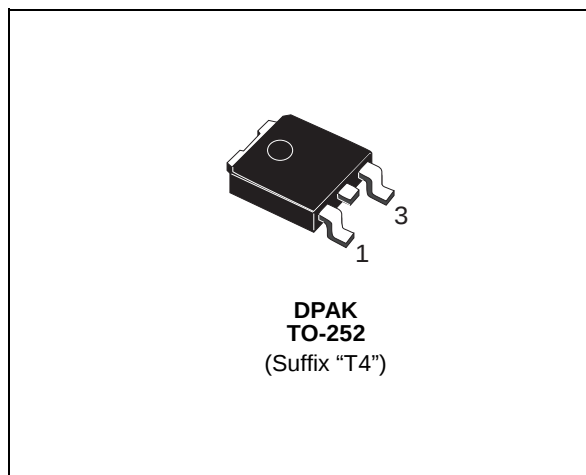
- TYPICAL R_{DS(on)} = 0.009 Ω @ 10V
- OPTIMAL R_{DS(on)} x Q_g TRADE-OFF
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- SURFACE-MOUNTING DPAK (TO-252)
POWER PACKAGE IN TAPE & REEL
(SUFFIX "T4")

DESCRIPTION

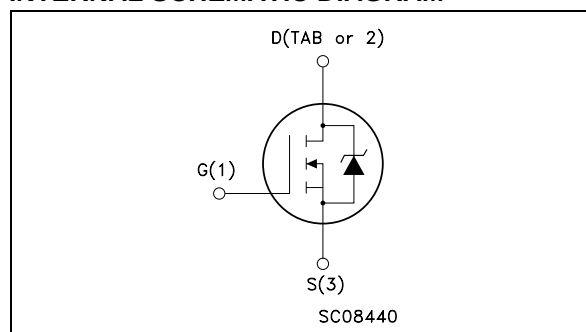
This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS
- AUTOMOTIVE SWITCHING APPLICATIONS



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD40NF3LLT4	D40NF3LL@	TO-252	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	30	V
V _{GS}	Gate- source Voltage	± 16	V
I _D (●)	Drain Current (continuous) at T _C = 25°C	40	A
I _D	Drain Current (continuous) at T _C = 100°C	28	A
I _{DM} (●●)	Drain Current (pulsed)	160	A
P _{tot}	Total Dissipation at T _C = 25°C	80	W
	Derating Factor	0.53	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	5.5	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	850	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(●) Current limited by the package

(●●) Pulse width limited by safe operating area.

(1) I_{SD} $\leq$ 40A, di/dt $\leq$ 350A/ μ s, V_{DD} $\leq$ V_{(BR)DSS}, T_j $\leq$ T_{JMAX}

(2) Starting T_j = 25 °C, I_D = 20A, V_{DD} = 25V

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THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	1.88	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	100	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 µA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 20 A V _{GS} = 4.5 V I _D = 10 A		0.0090 0.0115	0.0110 0.0135	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 20 A		23		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1650 540 130		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		23 156		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=15\text{ V}$ $I_D=40\text{ A}$ $V_{GS}=4.5\text{ V}$		24 8.5 12	33	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		27 28		ns ns

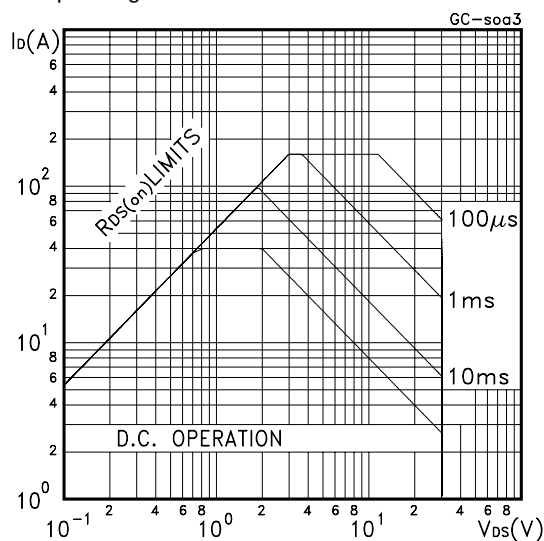
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				40 160	A A
$V_{SD}^(*)$	Forward On Voltage	$I_{SD} = 40\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		40 50 2.5		ns nC A

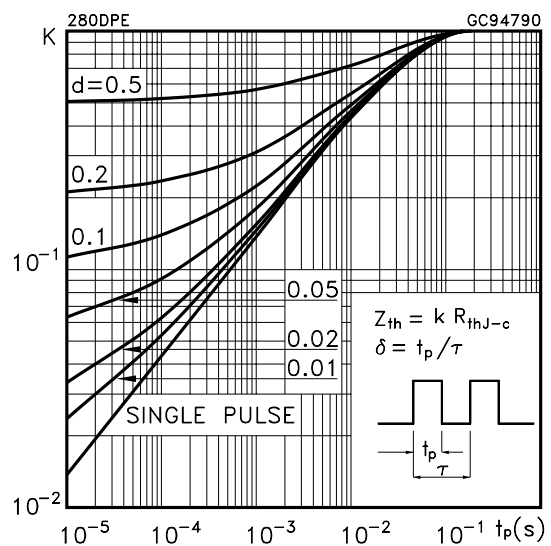
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(•) Pulse width limited by safe operating area.

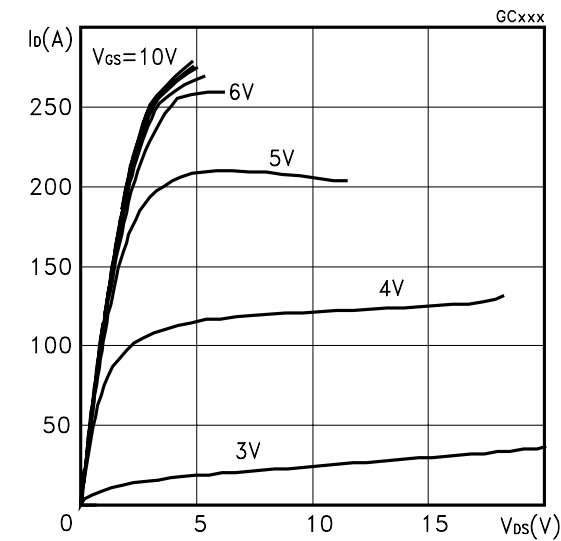
Safe Operating Area



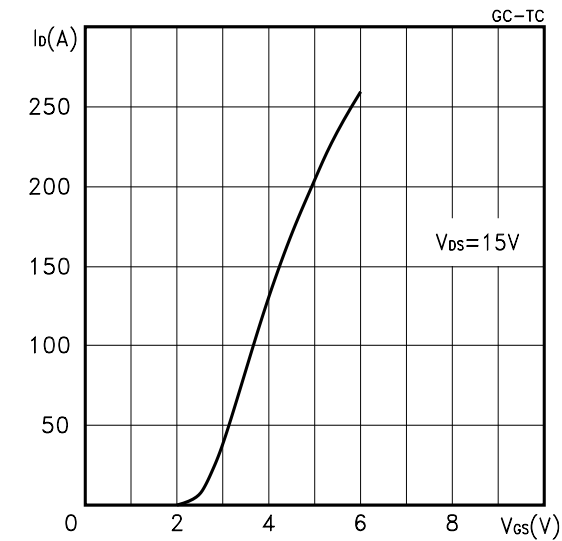
Thermal Impedance



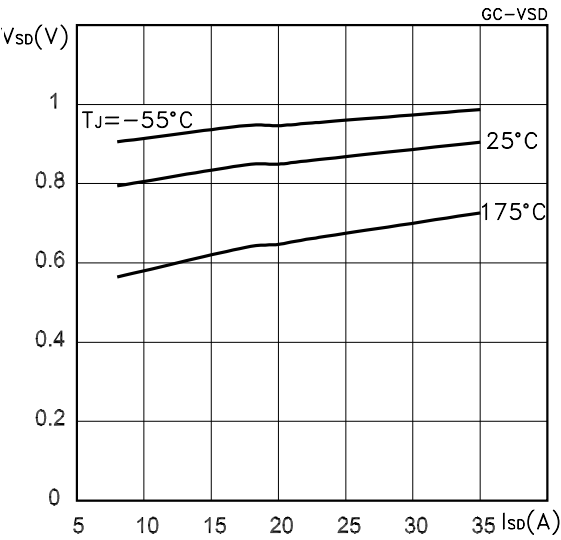
Output Characteristics



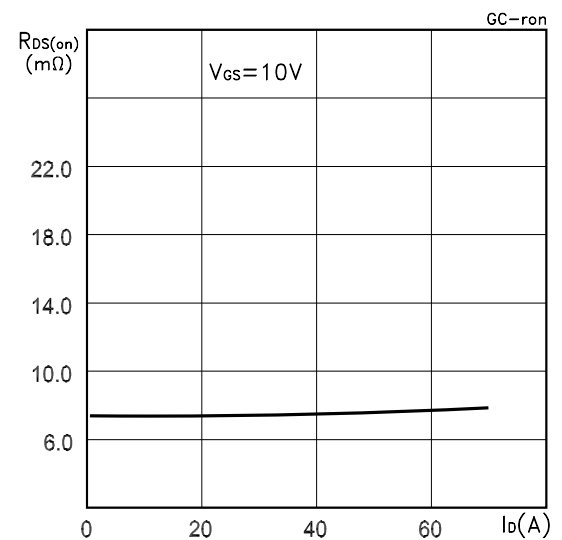
Transfer Characteristics



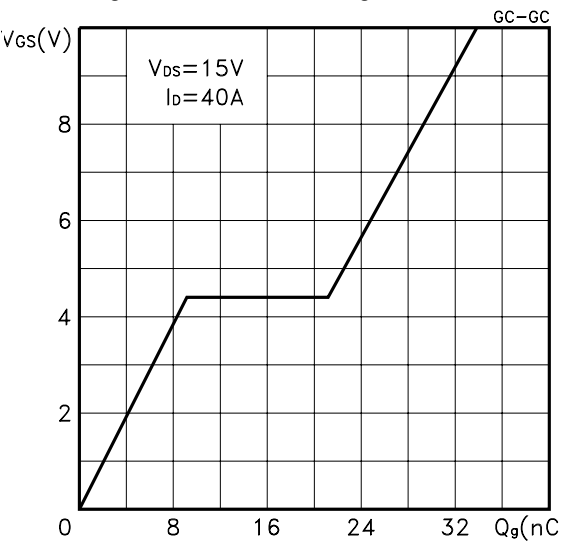
Source-drain Diode Forward Characteristics



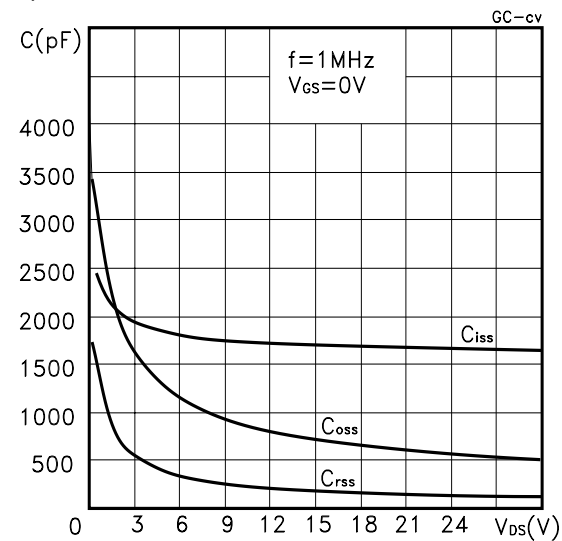
Static Drain-source On Resistance



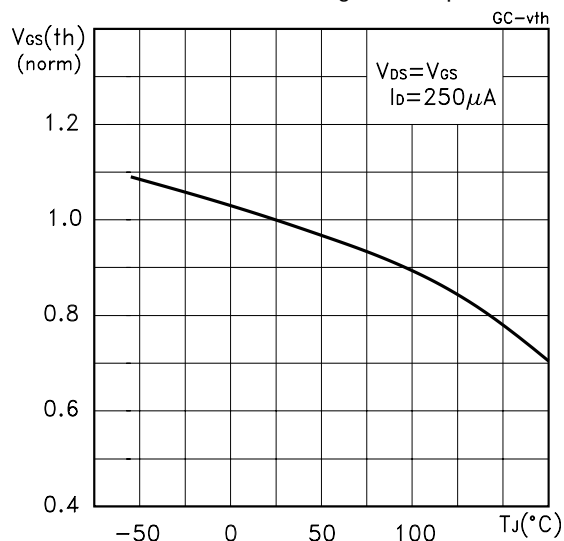
Gate Charge vs Gate-source Voltage



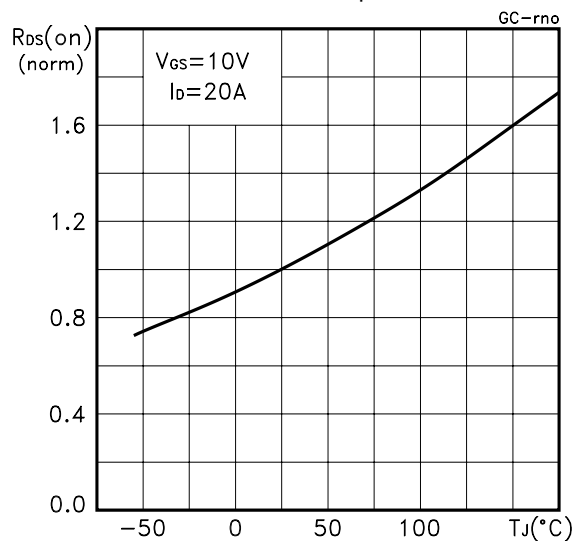
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Normalized Breakdown Voltage vs Temperature.

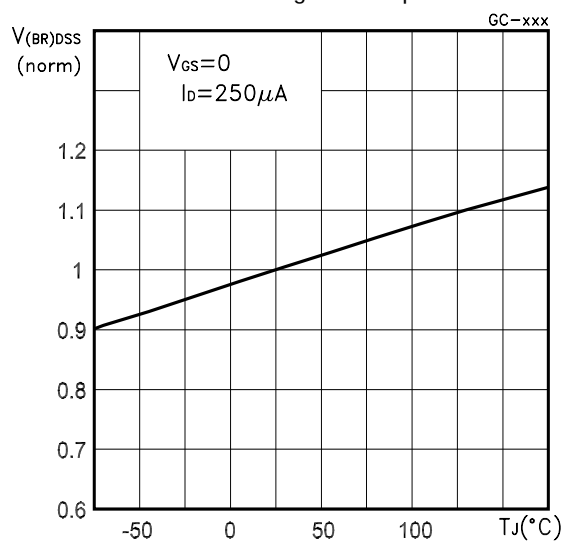


Fig. 1: Unclamped Inductive Load Test Circuit

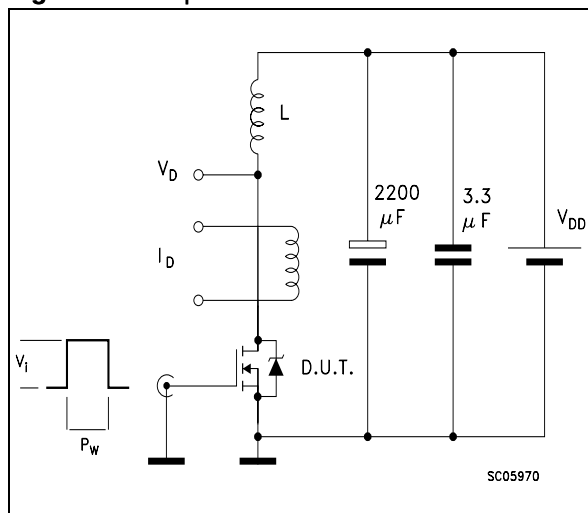


Fig. 2: Unclamped Inductive Waveform

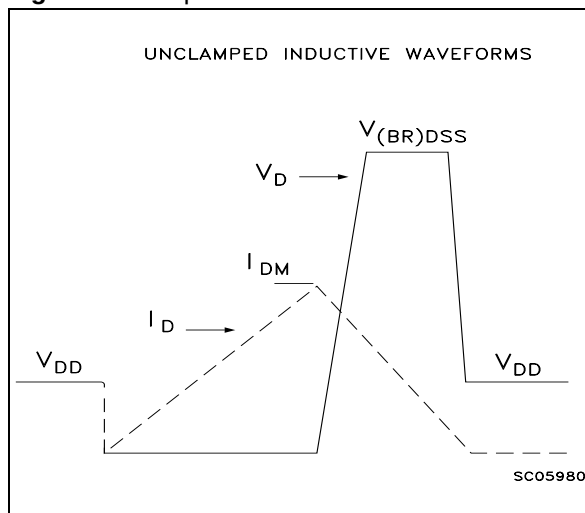


Fig. 3: Switching Times Test Circuits For Resistive Load

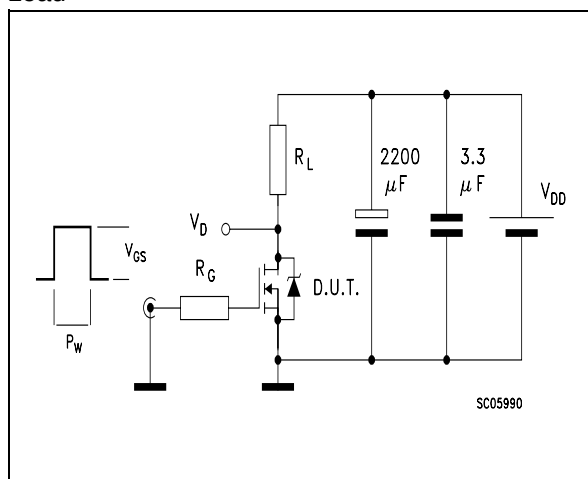


Fig. 4: Gate Charge test Circuit

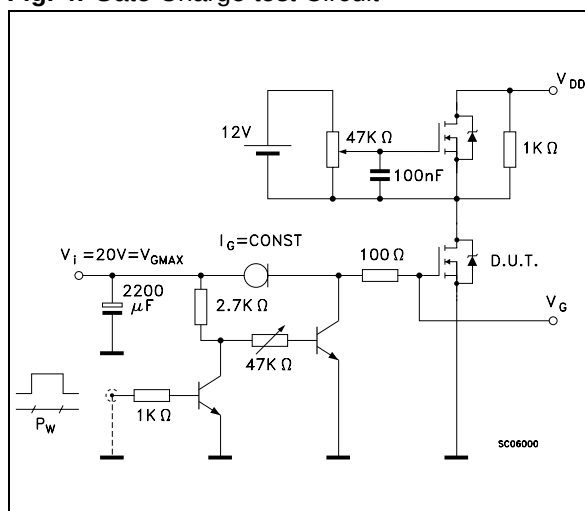
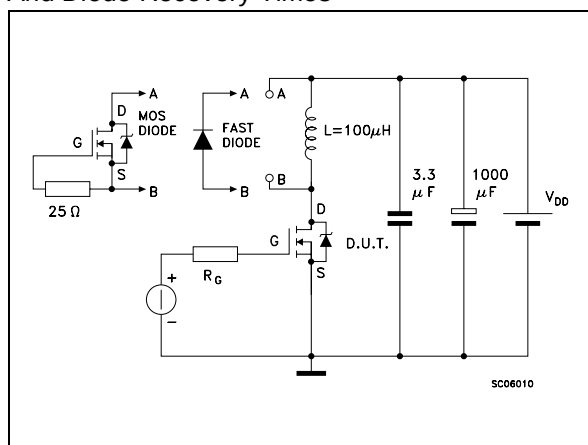
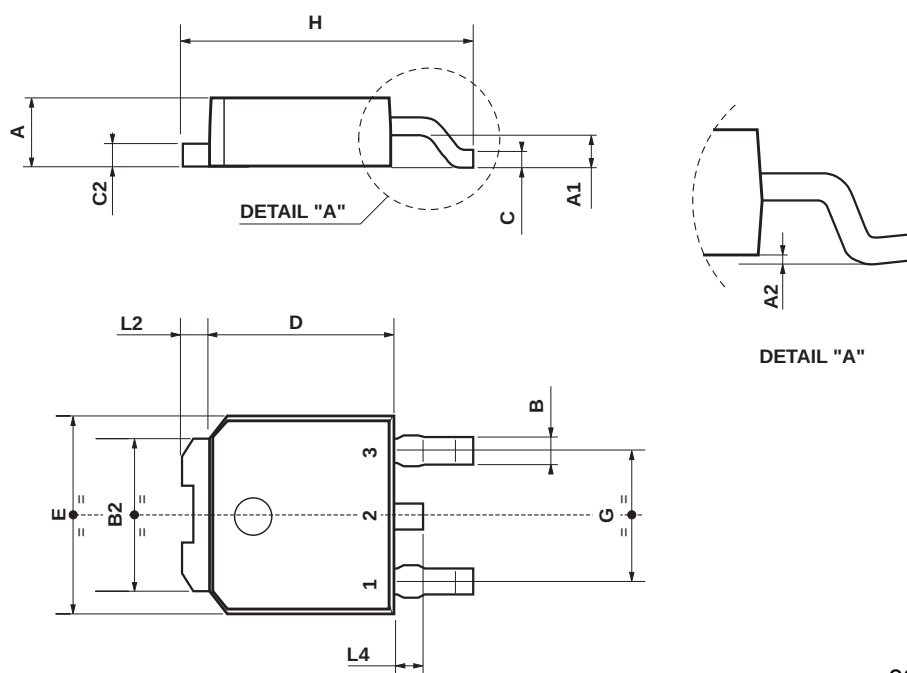


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



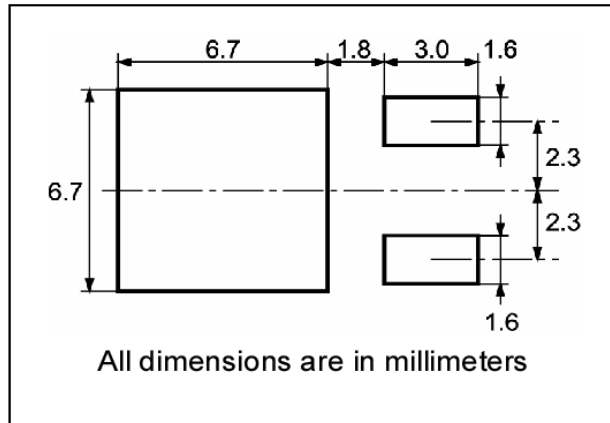
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039

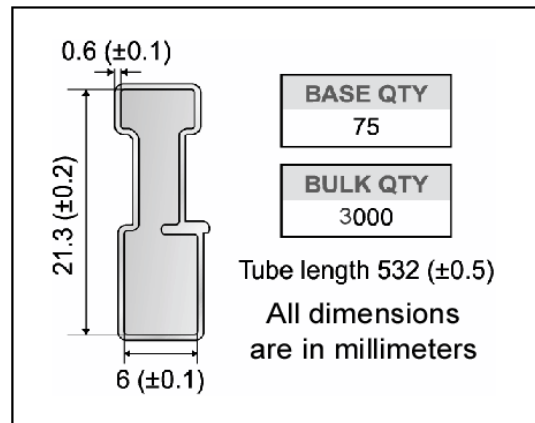


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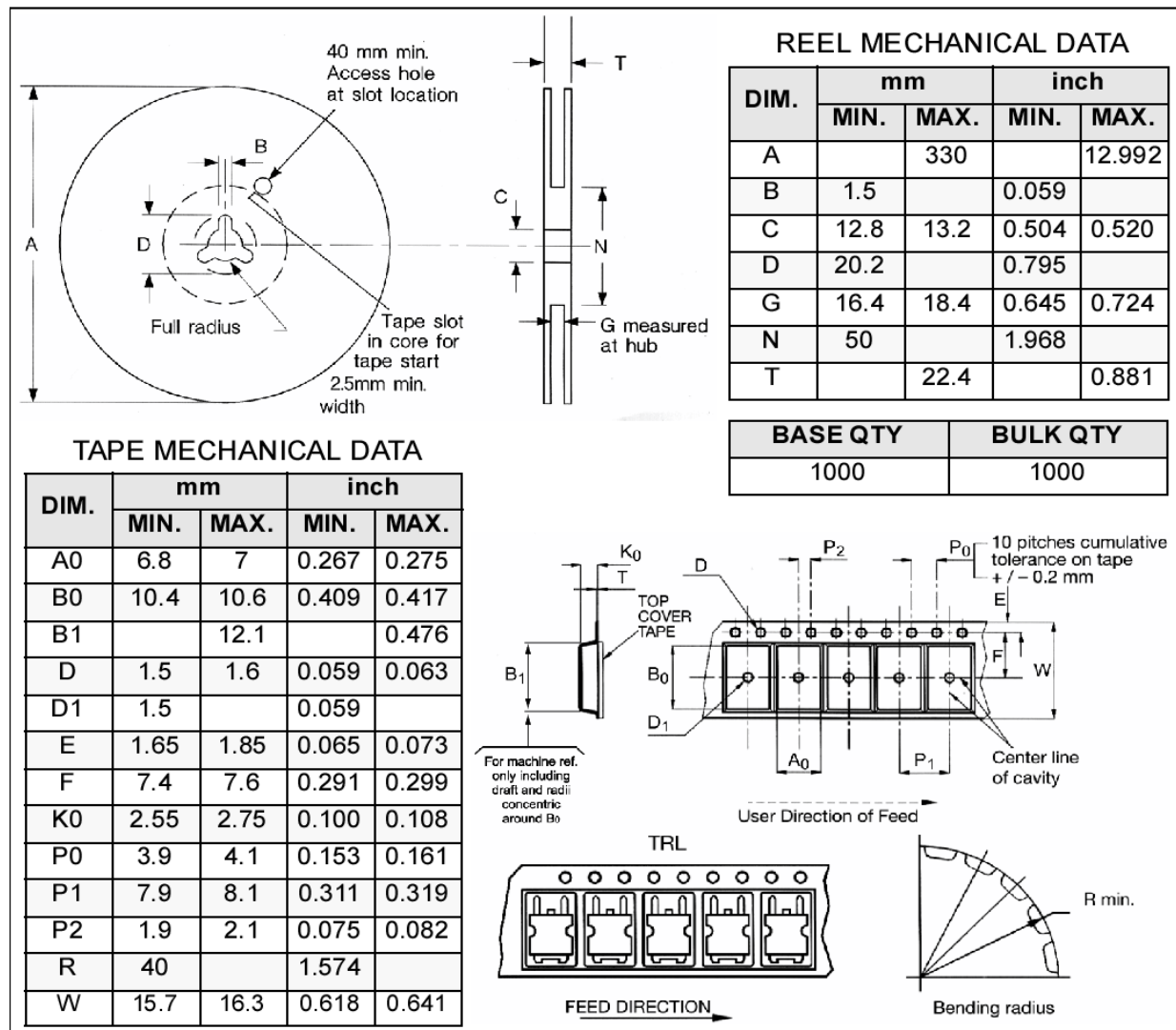
DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



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