



# STD95NH02L

## N-CHANNEL 24V - 0.0039Ω - 80A DPAK ULTRA LOW GATE CHARGE STripFET™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD95NH02L	24 V	< 0.005Ω	80(*) A

- TYPICAL R<sub>DS(on)</sub> = 0.0039Ω @ 10 V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

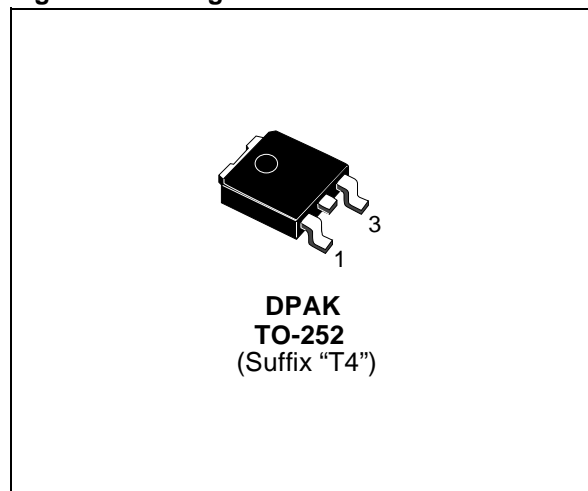
### DESCRIPTION

The **STD95NH02L** is based on the latest generation of ST's proprietary STripFET™ technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements in high-frequency DC-DC converters. It's therefore ideal for high-density converters in Telecom and Computer applications.

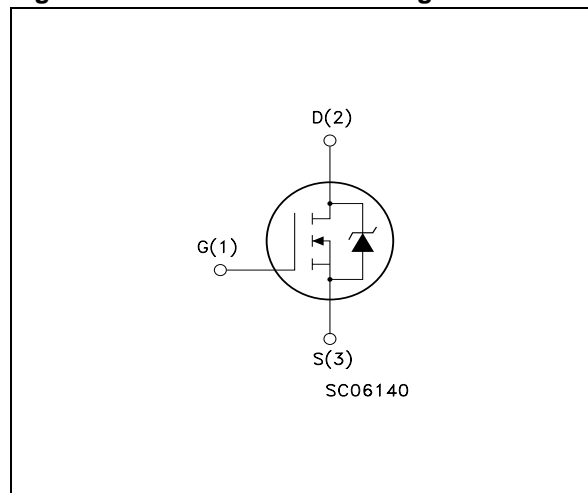
### APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

PART NUMBER	MARKING	PACKAGE	PACKAGING
STD95NH02LT4	D95NH02L	DPAK	TAPE & REEL

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>spike</sub> (1)	Drain-source Voltage Rating	30	V
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	24	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	24	V
V <sub>GS</sub>	Gate- source Voltage	± 20	V
I <sub>D</sub> (*)	Drain Current (continuous) at T <sub>C</sub> = 25°C	80	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	68	A
I <sub>DM</sub> (2)	Drain Current (pulsed)	320	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	100	W
	Derating Factor	0.67	W/°C
E <sub>AS</sub> (3)	Single Pulse Avalanche Energy	600	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

(1) Garanted when external R<sub>g</sub> = 4.7 Ω and t<sub>f</sub> < t<sub>f</sub> max.

(2) Pulse width limited by safe operating area.

(3) Starting T<sub>j</sub> = 25°C, I<sub>D</sub> = 40A, V<sub>DD</sub> = 22V

(\*) Value limited by wires

**Table 4: Thermal Data**

R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.5	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	100	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	275	°C

**ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> =25°C UNLESS OTHERWISE SPECIFIED)**

**Table 5: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	24			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A V <sub>GS</sub> = 5 V, I <sub>D</sub> =40 A		0.0039 0.0055	0.005 0.009	Ω Ω

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (4)	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 10\text{ A}$		30		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 15\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		2070 990 90		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 12\text{ V}$ , $I_D = 40\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 16)		20 110 47 20		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 12\text{ V}$ , $I_D = 80\text{ A}$ , $V_{GS} = 5\text{ V}$ (see Figure 19)		17 7.6 6.8		nC nC nC
$Q_{oss}$ (5)	Output Charge	$V_{DS} = 19\text{ V}$ , $V_{GS} = 0\text{ V}$		22.6		nC
$Q_{gls}$ (6)	Third-Quadrant Gate Charge	$V_{DS} < 0\text{ V}$ , $V_{GS} = 5\text{ V}$		15		nC
$R_G$	Gate Input Resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.8		$\Omega$

Table 7: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				80	A
$I_{SDM}$	Source-drain Current (pulsed)				320	A
$V_{SD}$ (4)	Forward On Voltage	$I_{SD} = 40\text{ A}$ , $V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 80\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 20\text{ V}$ , $T_j = 150^\circ\text{C}$ (see Figure 16)		42 50.4 2.4		ns nC A

(4). Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

(5).  $Q_{oss} = C_{oss} \cdot \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{ds}$ . See Appendix A.

(6). Gate charge for Synchronous Operation.

Figure 3: Safe Operating Area

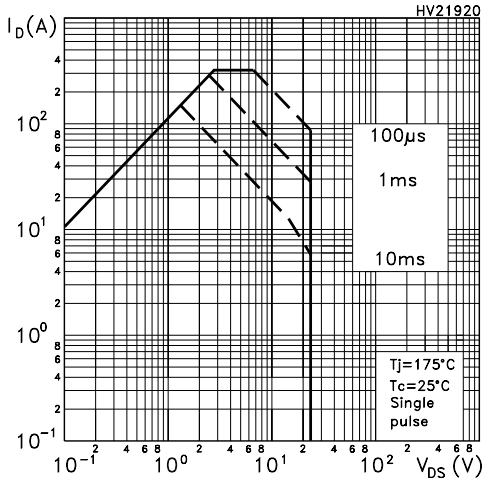


Figure 4: Output Characteristics

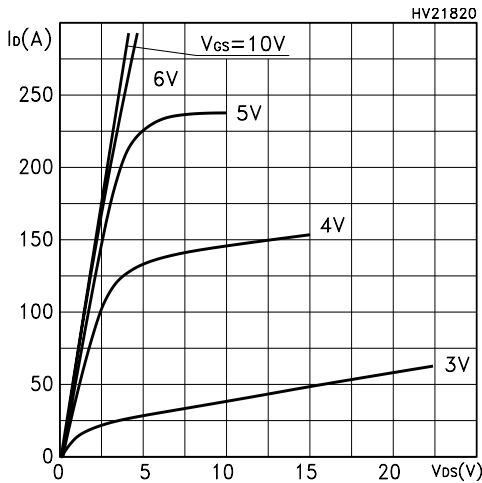


Figure 5: Transconductance

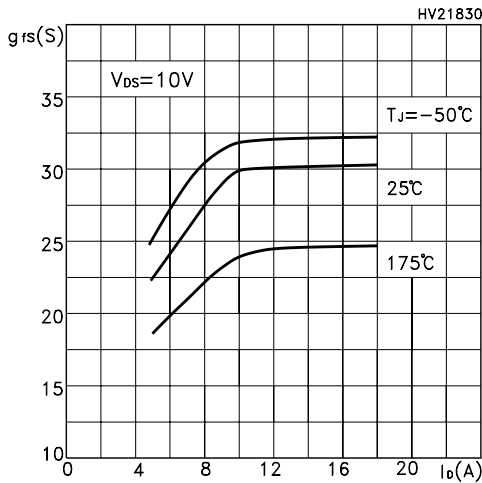


Figure 6: Thermal Impedance

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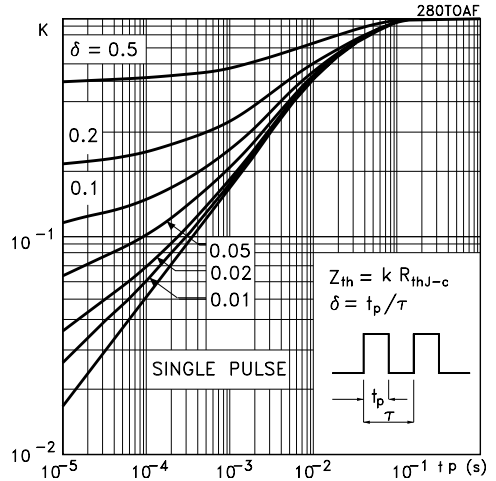


Figure 7: Transfer Characteristics

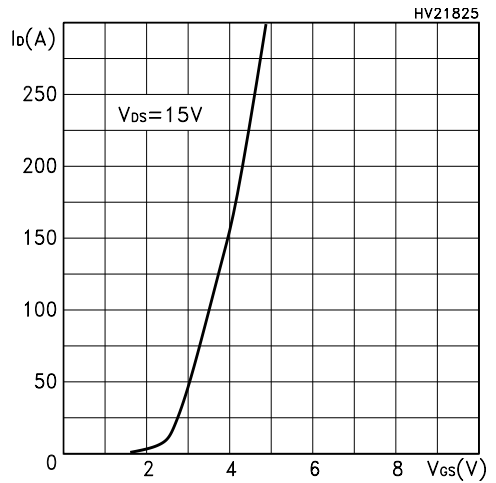


Figure 8: Static Drain-source On Resistance

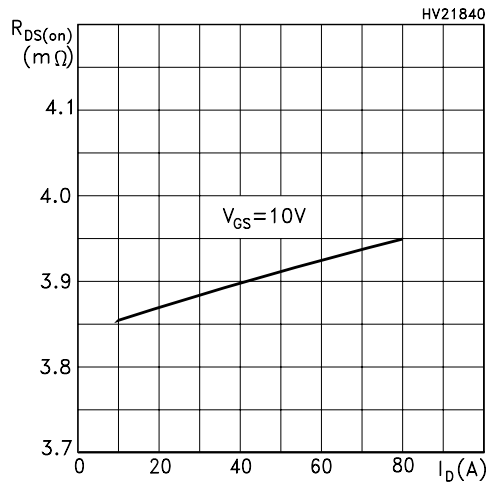


Figure 9: Gate Charge vs Gate-source Voltage

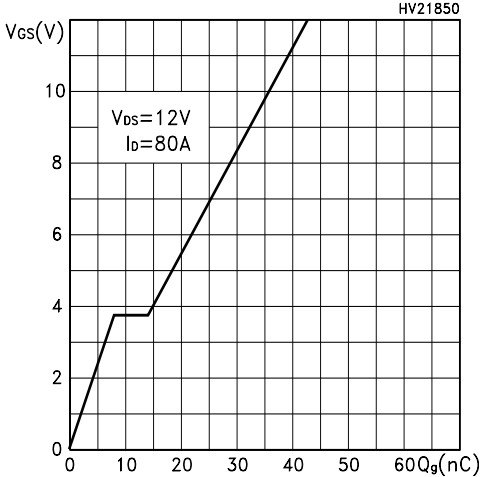


Figure 10: Normalized Gate Threshold Voltage vs Temperature

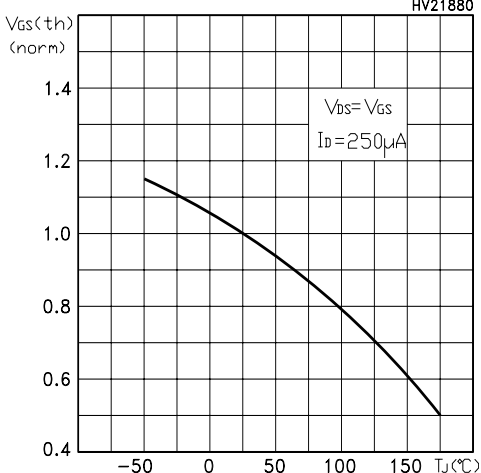


Figure 11: Dource-Drain Diode Forward Characteristics

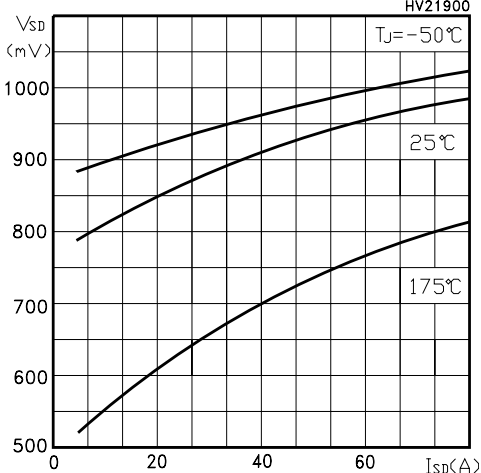


Figure 12: Capacitance Variations

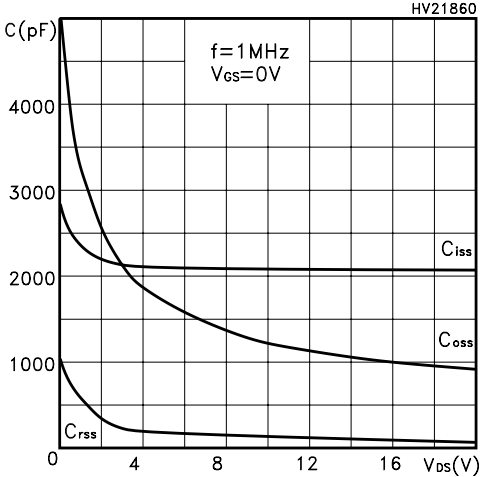


Figure 13: Normalized On Resistance vs Temperature

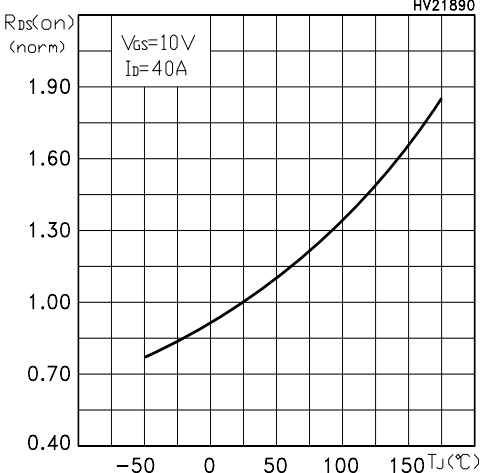


Figure 14: Normalized Breakdown Voltage vs Temperature

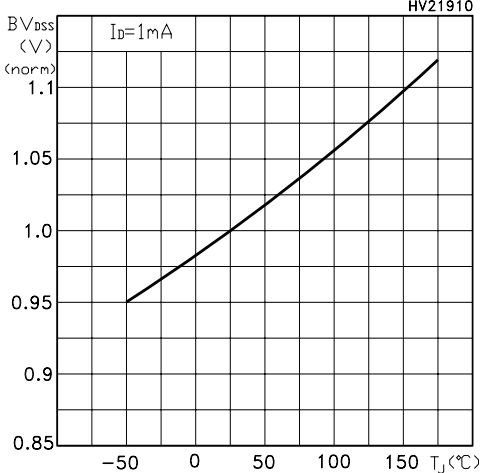


Figure 15: Unclamped Inductive Load Test Circuit

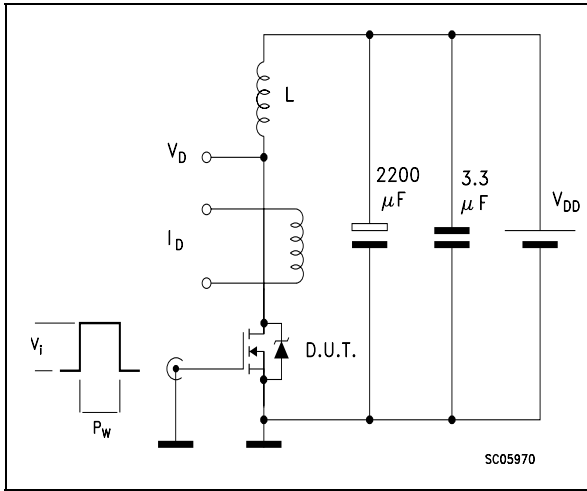


Figure 16: Switching Times Test Circuit For Resistive Load

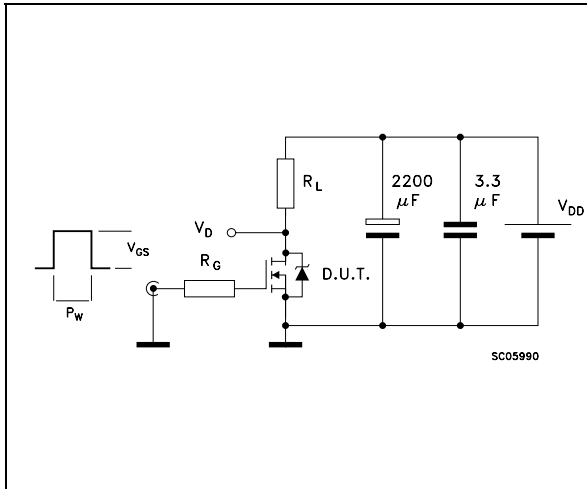


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

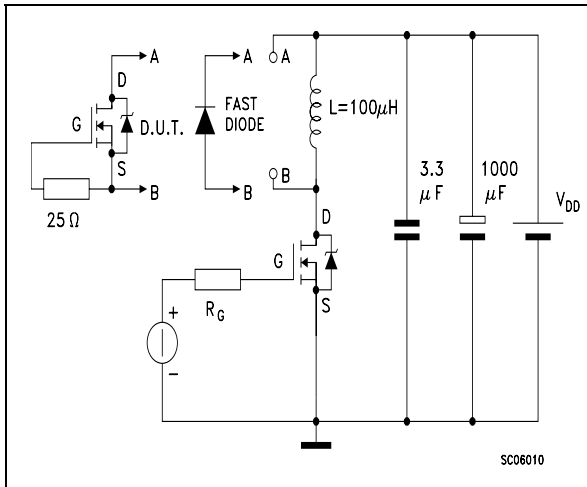


Figure 18: Unclamped Inductive Waferform

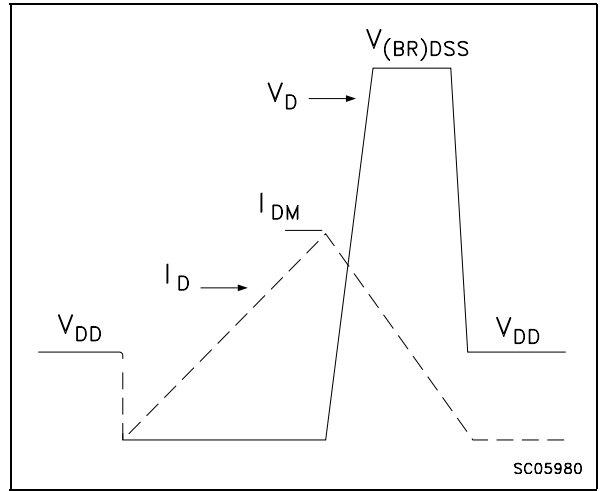
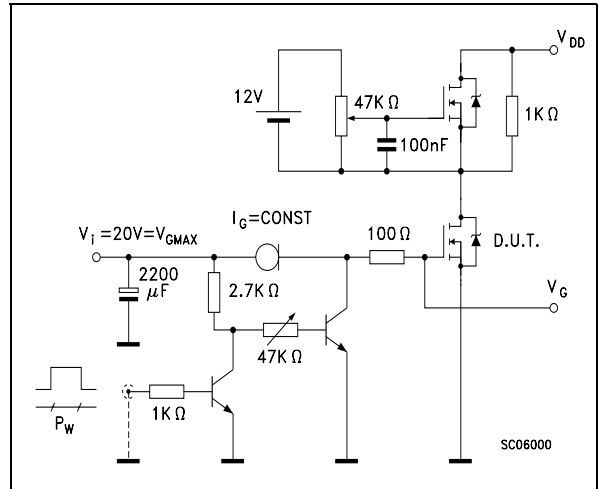
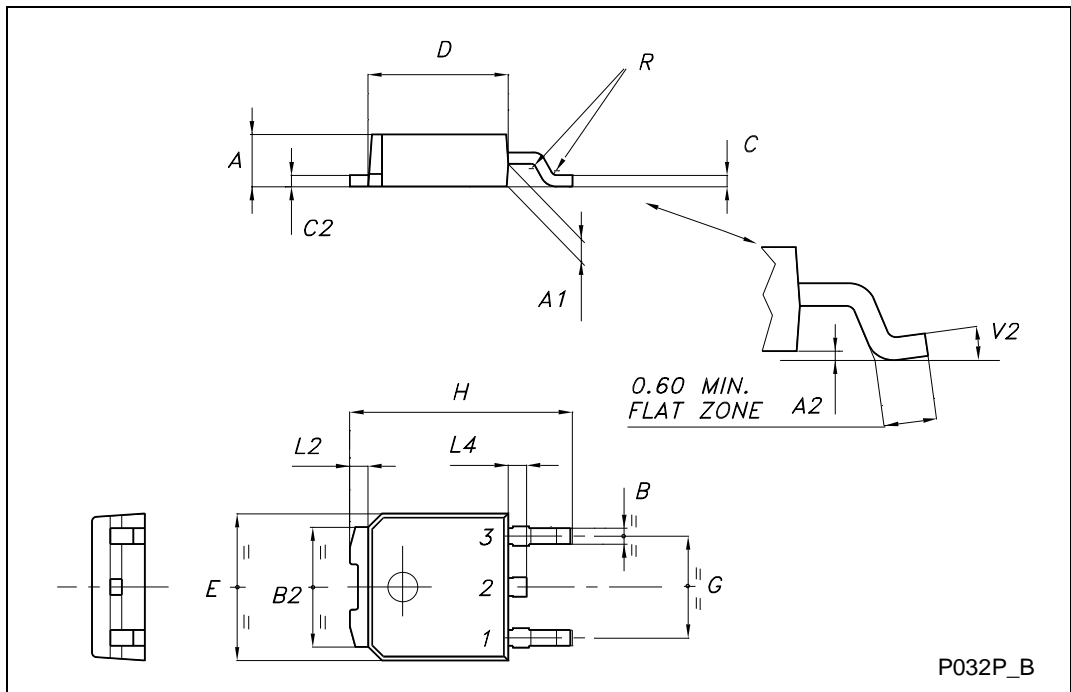


Figure 19: Gate Charge Test Circuit



**TO-252 (DPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°

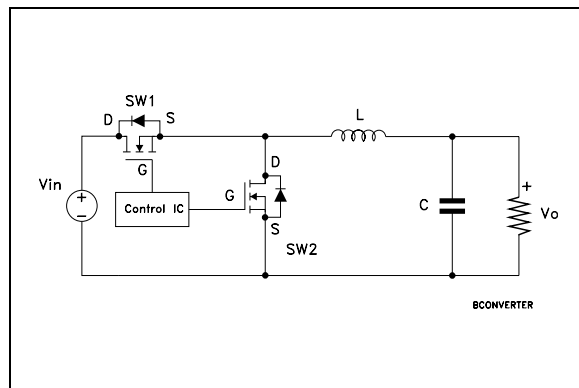




## Appendix A: Buck Converter Power Losses Estimation

### DESCRIPTION

The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.



#### The low side (SW2) device requires:

- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gls}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW1 during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{GG}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon

#### The high side (SW1) device requires:

- Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
- Low  $R_{DS(on)}$  to reduce the conduction losses

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gs(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
$P_{diode}$	Recovery	Not Applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{r(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q)}$		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gs(SW2)} * V_{gg} * f$
$P_{Qoss}$		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
$\delta$	Duty-Cycle
$Q_{gsth}$	Post Threshold Gate Charge
$Q_{gls}$	Third Quadrant Gate Charge
$P_{conduction}$	On State Losses
$P_{switching}$	On-off Transition Losses
$P_{diode}$	Conduction and Reverse Recovery Diode Losses
$P_{diode}$	Gate Drive Losses
$P_{Qoss}$	Output Capacitance Losses

**Table 8: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
27-Aug-2004	1	First Release.
10-Sep-2004	2	Values changed in table 7

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